

# Upgrade of End-cap TOF Trigger system on BESIII

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**Abstract**—In the ETOF(End-cap TOF) upgrade of BESIII, MRPC(Multi-gap Resistive Plate Chamber) detectors are used. ETOF is designed with 72 MRPCs. 24 channels signal are read out from each MRPC, in which 6 neighbouring channels OR together in Front-End Electronic(FEE) side. So 288 channel hit signals are sent to ETOF trigger system for trigger logic. The MRPC hit signal is about 30 ns width after FEE. Hit signals are stretched and trigger data are stored by TDPP (Trigger Data Pre-Processor) and then sent to ETOFT (End-cap TOF Trigger) through 10 high speed optical fiber links. Trigger data are aligned and stored in FIFO in ETOFT. Trigger logic in the center FPGA counts hit signals and finds Back to Back (BtB) events and give out three ETOF trigger conditions: NETOF.GE.1, NETOF.GE.2 and ETOF.BB. ETOF trigger conditions are integrated with other detector trigger signals by SIF2(Signal Integrate and Fan-out Version2) to Global Trigger to generate L1. ETOF trigger system was installed on BESIII in Sept.2015 and has run stable for half year.

**Index Terms**—BESIII, ETOF, MRPC, trigger.

## I. INTRODUCTION

**B**EIJING Spectrometer III (BESIII) is the main detector on Beijing Electron-Positron Collider II (BEPCII) which designed luminosity is  $10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ [1]. TOF (Time of Flight) consisted of Barrel TOF(BTOF) and End-Cap TOF(ETOF) is one sub-detector on BESIII[1]. With high time resolution, its trigger condition is used as timing reference for BESIII Data Acquisition (DAQ) system. In 2008, plastic scintillator was used as TOF detector(both for BTOF and ETOF) with intrinsic time resolution up to 80-90ps[2]. In order to improve the performance of End Cap TOF, MRPC(Multi-gap Resistive Plate Chamber) detectors are used, instead of Plastic scintillators in ETOF detector from 2015. Now its intrinsic time resolution is better than 60 ps and detection efficiency is better than 96%. With the upgrade of ETOF detector, FEE, trigger and DAQ system are all new designed.

ETOF is designed with 72 MRPCs, 36 MRPCs on each side, as shown in Fig.1. MRPC are staggered in two layers to make sure its effective detection area is more than 99%

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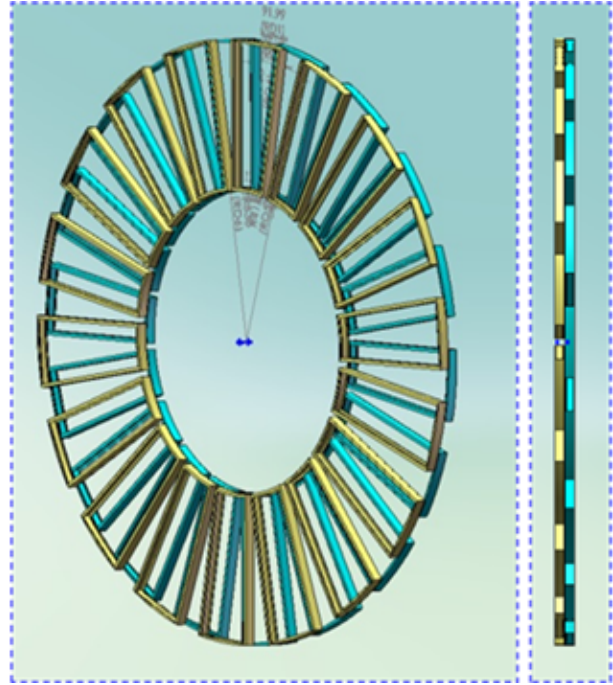


Fig. 1. ETOF MRPC detector model.

of detector covering area. There are 12 MRPC pads in one MRPC. And pad signals are double-end readout by Front-End Electronic(FEE). Totally, 24 channels signal are read out from each MRPC, in which 6 neighbouring channels OR together in side and sent to trigger system, as shown in Fig.2. So 288 channel hit signals are sent to ETOF trigger system for trigger logic. The width of MRPC hit signal is about 30 ns after FEE OR logic. In ETOF trigger system, the 288 channel hit signals are used to generate the hit trigger condition NETOF.GE.1, NETOF.GE.2 and relative location trigger condition ETOF.BB[3].

## II. ETOF TRIGGER SYSTEM

On ETOF FEE side, CTTT boards send out 288 channels hit signal to ETOF trigger system. Hit signals are pre-processed near detector in BESIII hall by Trigger Data Pre-Processing (TDPP) board and then sent to ETOF Trigger(ETOFT) board by 10 high speed fiber links at 2.5Gbps line rate. Data alignment protocol are used to compensate different hardware delay in 10 channels. ETOFT generate same trigger conditions as old one. NETOF.GE.1, NETOF.GE.2, ETOF.BB trigger conditions then are sent to Global Trigger Logic(GTL) system by Signal Integrate and Fan out Version2(SIF2), as shown in Fig.3.

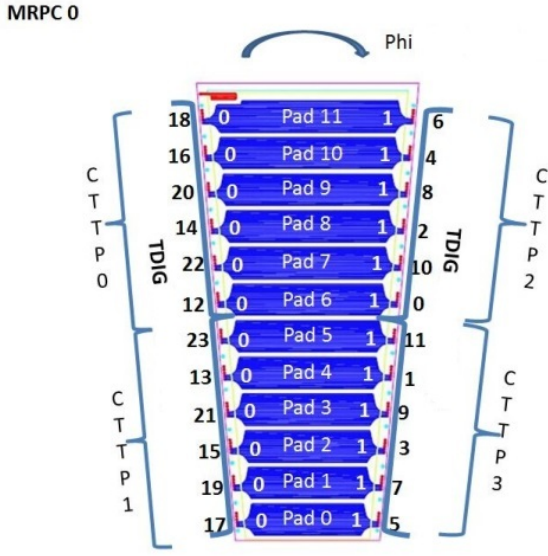


Fig. 2. MRPC FEE readout channel and OR logic structure.

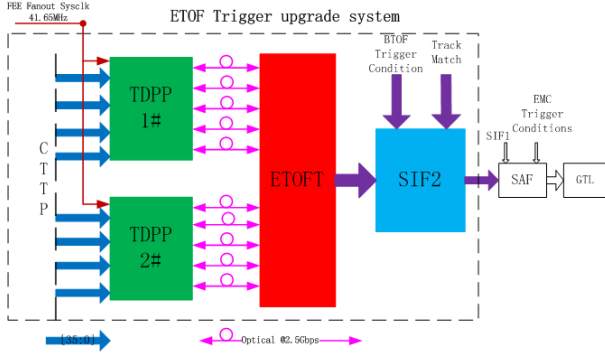


Fig. 3. Block diagram of ETOF trigger system.

#### A. Trigger Data Pre-Process

ETOF hit signals in one event has the uncertain time about 30ns which caused by drift time[4]. It may cause 2 system clock skew maximum when signal arrived at trigger system. Signals are stretched 3 system clocks(41.65MHz) before trigger logic to make sure signals in one event can be matched together. Hit signal is about one clock width. Asynchronous stretch circuit is designed to improve trigger efficiency.

#### B. Data alignment protocol

Data alignment protocol is used for data transmission between TDPP and ETOFT for making sure the data timing relationship among 10 RocketIO channels.

This protocol can meet different data rate request whose system clock under 62.5MHz. It also has the function of error rate check in trigger data transmission layer. Fig.4 and Fig.5 showed the receiving data on ETOFT side before data alignment protocol and aligned data after protocol, observed by chipscope.

C00	958C	958C	B5B5_957C	B5B5_957C	B5B5_957C	FFFF	CCCC	FFFF	DDDD	FFFF
C01	958C	958C	B5B5_957C	B5B5_957C	B5B5_957C	FFFF	CCCC_0000	FFFF	DDDD_0000	FFFF
C02	958C	958C	B5B5_957C	B5B5_957C	B5B5_957C	FFFF	CCCC	FFFF	DDDD	FFFF
C03	958C	958C	B5B5_957C	B5B5_957C	B5B5_957C	FFFF	CCCC	FFFF	DDDD	FFFF
C04	FFFF	FFFF	958C_B5B5_957C	958C_B5B5_957C	958C_B5B5_957C	B5B5_957C	B5B5_957C	FFFF	CCCC_0000	FFFF_X_D
C05	958C	958C	B5B5_957C	B5B5_957C	B5B5_957C	FFFF	CCCC	FFFF	DDDD	FFFF
C06	958C	958C	B5B5_957C	B5B5_957C	B5B5_957C	B5B5_957C	FFFF	CCCC	FFFF	DDDD
C07	958C	958C	B5B5_957C	B5B5_957C	B5B5_957C	B5B5_957C	FFFF	CCCC	FFFF	DDDD
C08	958C	958C	B5B5_957C	B5B5_957C	B5B5_957C	B5B5_957C	FFFF	CCCC	FFFF	DDDD
C09	FFFF	FFFF	B5B5_958C	B5B5_958C	B5B5_958C	B5B5_958C	B5B5_957C	B5B5_957C	B5B5_957C	B

Fig. 4. Data after Deserial on ETOFT.

C00	00000	00000	B5B5957C	AAAAAAAA	FFFFFFFF	BBBBBBBB
C01	00000	00000	B5B5957C	AAAAAAAA	FFFFFFFF	BBBBBBBB
C02	00000	00000	B5B5957C	AAAAAAAA	FFFFFFFF	BBBBBBBB
C03	00000	00000	B5B5957C	AAAAAAAA	FFFFFFFF	BBBBBBBB
C04	00000	00000	B5B5957C	0000AAAA	FFFFFFFF	0000BBBB
C05	00000	00000	B5B5957C	AAAAAAAA	FFFFFFFF	BBBBBBBB
C06	00000	00000	B5B5957C	AAAAAAAA	FFFFFFFF	BBBBBBBB
C07	00000	00000	B5B5957C	AAAAAAAA	FFFFFFFF	BBBBBBBB
C08	00000	00000	B5B5957C	AAAAAAAA	FFFFFFFF	BBBBBBBB
C09	00000	00000	B5B5957C	0000AAAA	FFFFFFFF	0000BBBB

Fig. 5. Data after alignment protocol.

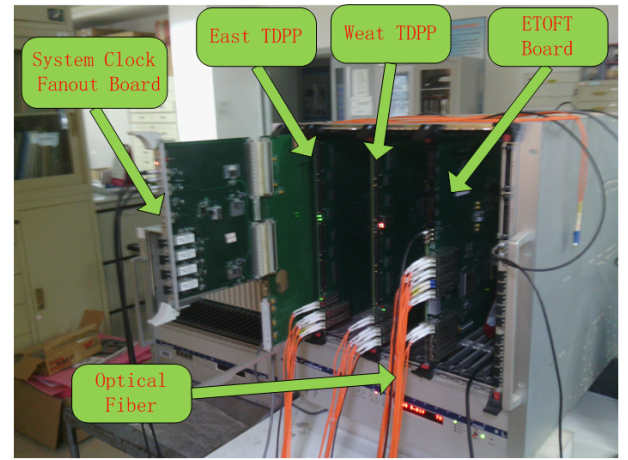


Fig. 6. Trigger system in the lab.

#### C. ETOF trigger logic algorithm

In trigger logic, one MRPC shown in Fig.3 is used as one trigger unit. For signals in trigger unit, OR logic is used for double-end signals to improve trigger efficiency.

#### D. Trigger logic verification

In trigger lab, ETOF trigger system was built with one clock fan-out board, three TDPP boards and one ETOFT boards to verify trigger logic. Clock board was used to generate system clock 41.65MHz and fan out to TDPP boards and ETOFT board. In the three TDPP boards, one is used to as a control boards to send FRST signal to backplane of VME, the other two are used as trigger data pre-process boards. Simulation data data was downloaded on TDPP. With this method, logic are verified and trigger logic efficiency is 100%, as shown in Fig.6.

### III. CONCLUSION

In ETOF upgrade, 288 channel OR signals are sent to ETOF trigger system for NETOF.GE.1, NETOF.GE.2 and NETOF.BB conditions logic. 1 to 7 location relationship with central asymmetry is figure out by trigger simulation for back to back event triggering. Trigger logic is verified and efficiency is 100% by simulation event. ETOFT was installed on Sept.

2015 and the whole system is already running half year for physics data taking. Efficiency of NETOF.GE.1 used by data taking is 99.74%. The performance of ETOF trigger system meets the design requirements.

#### ACKNOWLEDGMENT

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