THE ASSOCIATIVE MEMORY SYSTEM INFRASTRUCTURE OF THE ATLAS FAST TRACKER

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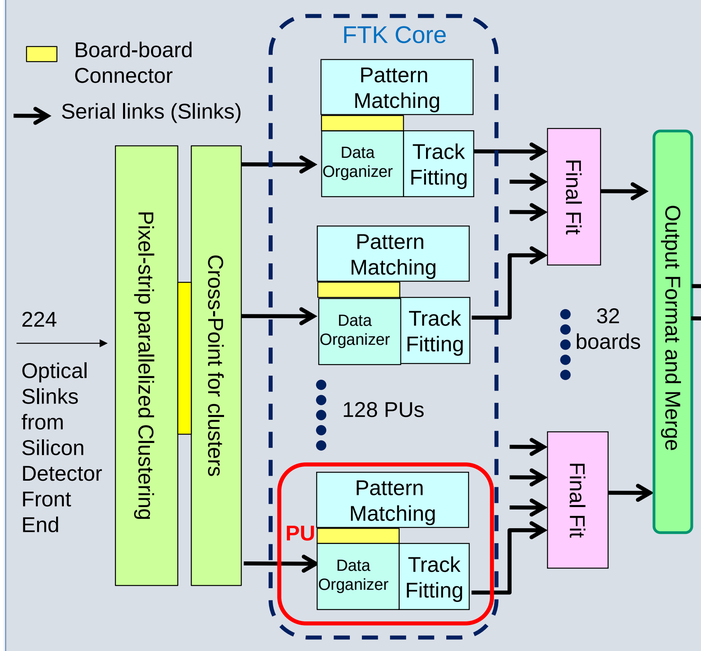
OVERVIEW

The FTK [1] is designed to perform pattern matching of detector channels hit by charged particles crossing the ATLAS experiment [2] sillicon tracker. The Associative Memory (AM) [3] system of the Fast TracKer processor has been designed is the main processing element of FTK and is based on the use of ASICs designed to execute pattern matching with a high degree of parallelism. It finds track candidates at coarse resolution that are seeds for higher precision track fitting. The AM system implementation is a collection of 128 boards, named "Serial Link Processors" (AMBSLPs) [4]. On these boards a huge traffic of data is implemented on a network of 900 2 Gb/s serial links. Even if the complete AM-based processor is much less power consuming (~40 kW) than its CPU equivalent, its size is much smaller. The result is an extremely high consumption per unit volume and the need for complex custom infrastructures in order to have a correct cooling. The AMBSLP has a consumption of ~250 W.

FTK ARCHITECTURE



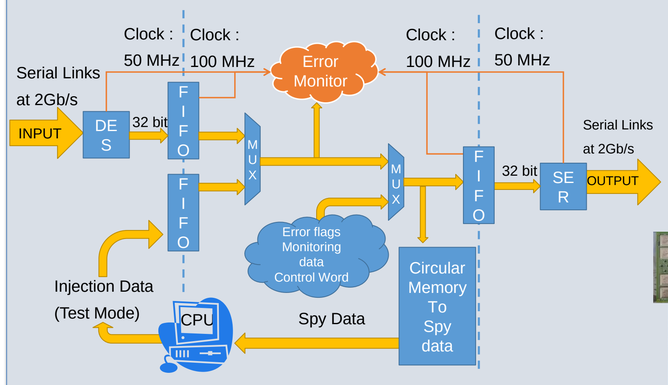
The FTK core solves the huge combinatorics required by pattern recognition.

- It is the most power and timing consuming part of FTK.
- Organized into **128 Processing Units** (PUs) which process the tracker data in parallel
- Each PU executes in pipeline the **two main FTK algorithms**, the Pattern Matching (PM) and the Track Fitting (TF).
- Data Organizer is the interface between the two algorithms
- Final Fit uses 4 additional SCT layers to remove even more fake tracks

The FTK core along with the Final Fit (Second Stage Board) are located on VME bins.

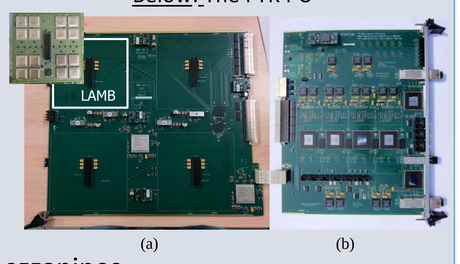
The core of FTK is compact (4 racks of electronics) and power usage is low (~50 kW) if compared to the farm of thousands of commercial CPUs [5] required to perform an equivalent task.

FTK PROCESSING UNIT (PU)



On the left: Representation of the data driven pipeline for a single data link inside the AMBSLP. Both input and output FPGA logic is controlled by the external CPU

Below: The FTK PU



(a) (b)

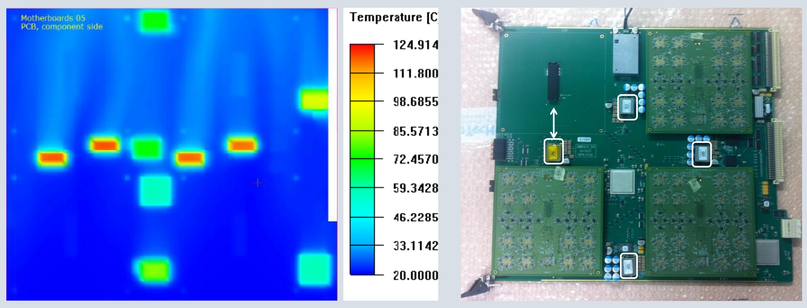
FTK PU consists of:

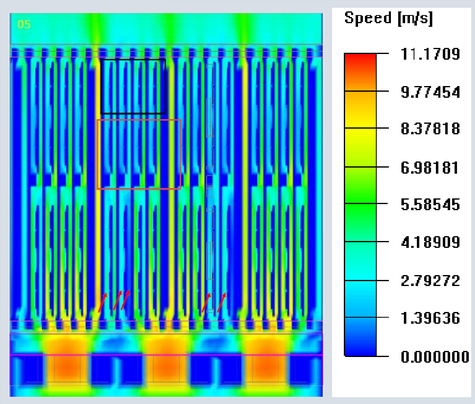
a) The **AMBSLP** (version 2)
   - Each AMBSLP has **4 LAMBs** mounted as mezzanines
   - Each LAMB contains **16 AM chips** that perform Pattern Matching
   - On the board there are **5 General Electric DC-DC converters** that distribute the 48V input to the LAMBs, keeping the power as high as possible

b) **AUX**iliary Card which contains the **Data Organizer** and the **Track Fitter**

PU's average power consumption is 250W (AMBSLP) + 80W(AUX)

TEMPERATURE SIMULATION AND TESTS



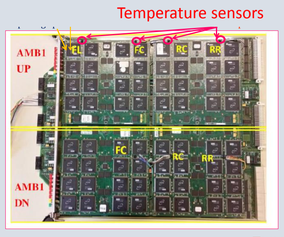


Simulations showed that DC-DC converters needed repositioning in order to improve thermal state of the upper LAMBs. PCB temperature could reach ~90°C and the AM chip some degrees more

Further simulations on the whole bin rendered necessary the investigation of the hottest VME slots as a lack of temperature uniformity was noticed.

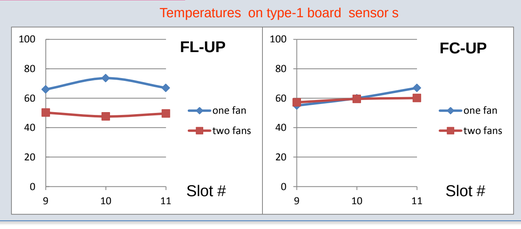
Thus, there were tests on VME bins performed using AMBSlim [7] (with AM03 [8]) with temperature sensors on it in two different VME crate setups:

- With the Wiener HB [9] below the bin
- With two fan trays (up and down)

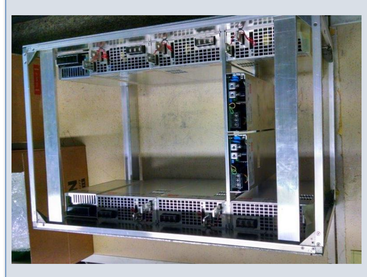


Test results indicated the unfavorable slots (center of fan wheels) and proved that the heat uniformity and temperature levels are better when using two fan trays

Temperatures on type-1 board sensor s



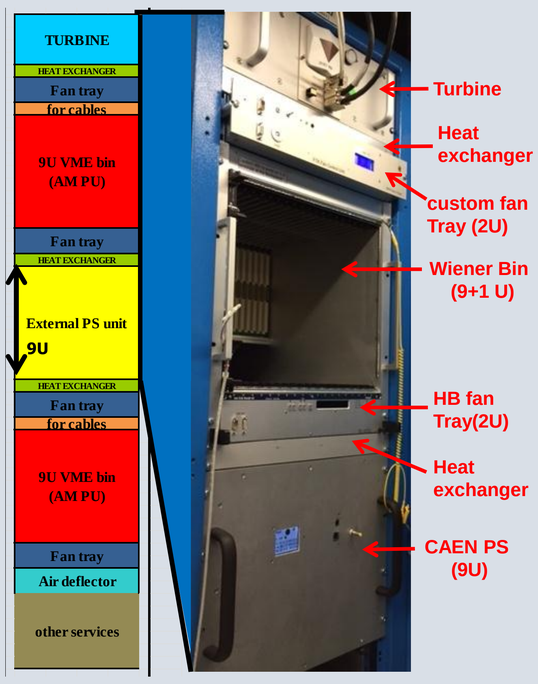
THE AM SYSTEM CUSTOM DESIGNED INFRASTRUCTURES



Custom CAEN PS

Cooling tests showed that extra cooling on the VME bins was imperative. For this purpose, two Arduino-controlled custom-made fan trays were designed and produced by INFN Pavia.

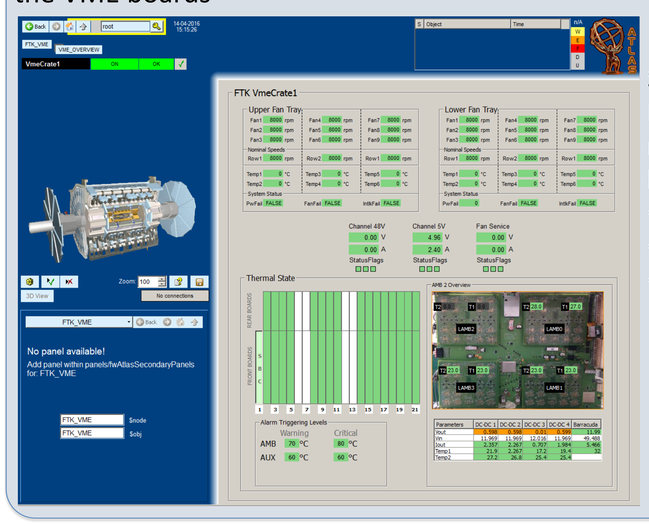
Because of the extra fan trays, space in the rack proved to be an issue. So a custom-made power supply by CAEN [6] was designed, able to provide power to two VME bins and their cooling systems and at the same time save enough space to even place extra heat exchangers.



Rack setup

DETECTOR CONTROL SYSTEM (DCS)

The fact that the AM System Infrastructure contains custom designed parts proved to be a challenge as well for the development of the FTK DCS. It introduced as new a Simple Network Management Protocol (SNMP) communication between Arduino and PC for the custom fan trays and an OPC UA Server that runs on the VME Single Board Computer (SBC) to monitor all the VME boards



Screenshot of the FTK VME DCS project in Lab4. In the main panel from top to bottom:

- Fan tray monitor
- CAEN PS monitor
- VME boards monitor

REFERENCES

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I.Maznas* on behalf of the ATLAS FTK Collaboration
*Aristotle University of Thessaloniki and PRISMA Electronics, imaznas@cern.ch