



Contribution ID: 170

Type: Oral presentation

The development of the Global Feature Extractor for the LHC Run-3 upgrade of the ATLAS L1 Calorimeter trigger system

Monday 6 June 2016 15:30 (30 minutes)

The Global Feature Extractor (gFEX) is one of several modules in the LHC Run-3 upgrade of the Level 1 Calorimeter (L1Calo) trigger system of the ATLAS experiment. It is a single Advanced Telecommunications Computing Architecture (ATCA) module for large-area jet identification with three Xilinx UltraScale FPGAs for data processing and a system-on-chip (SoC) FPGA for control and monitoring. A pre-prototype board has been designed to verify all functionalities. The performance of this pre-prototype has been tested and evaluated. As a major achievement, the high-speed links in FPGAs are stable at 12.8 Gb/s with Bit Error Ratio (BER) < 10⁻¹⁵ (no error detected). The low-latency parallel GPIO (General Purpose I/O) buses for communication between FPGAs are stable at 960 Mb/s. Besides that, the peripheral components of Soc FPGA have also been verified. After laboratory tests, the link speed test with LAr (Liquid Argon Calorimeter) Digital Processing Blade (LDPB) AMC card has been carried out at CERN for determination of the link-speed to be used for the links between LAr and L1Calo systems. The links from LDPB AMC card to gFEX run properly at both 6.4 Gb/s and 11.2 Gb/s. Test results of pre-prototype board validate the gFEX technologies and architecture. Now the prototype board design with three UltraScale FPGAs is on the way, the status of development will be presented.

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Session Classification: Upgrades 2

Track Classification: Upgrades