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## Hardware-Based Light Weight TCP/IP for 10 Gigabit Ethernet

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Ethernet has been widely used and implemented in a variety of commercial products. As their high ratio of performance to cost, many backend systems have been designed as distributed structure using Ethernet. Transmission Control Protocol and Internet Protocol (TCP/IP) is also a standard and well known protocol implemented in all mainstream operating systems, it provides a reliable and in-order data delivery featuring flow and congestion control.

Consequently, TCP/IP is becoming increasingly popular in front-end readout systems.

One example is the JUNO experiment, 1GSps 10-bit ADC is used to sample photomultiplier tubes (PMT) for supernova explosion observation, the sampling time may be as long as 1~2 seconds.

Another is the large area silicon pixels detector. The data size grows quickly as the pixel size decreases. The instantaneous bandwidth of 30 cm2 for DAQ may up to 10Gbps.

This paper presents a simplified and unidirectional TCP/IP, called FeTCP (Fast electronic TCP), for 10 Gigabit Ethernet (10GbE) with field programmable gate array (FPGA) implementation. As the hardware can be built on one chip, the detectors can be built as modules with a common interface. We prototyped the design on a KC705 development board, the preliminary test shows that the throughput of FeTCP is about 808MBps. A mechanism for slow control over User Datagram Protocol (UDP) is also provided.

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