WIR SCHAFFEN WISSEN – HEUTE FÜR MORGEN

Martin Brückner

A multiple 10 Gbit Ethernet data transfer system for EIGER

20th Real Time Conference

Outline

- The EIGER Detector

- Readout Firmware
  - Overview (Front End and Back End)
  - Image Summation
  - Online Compression
  - Data Rates

- Network / Data Transfer
  - Round Robin with Delay

The EIGER Detector

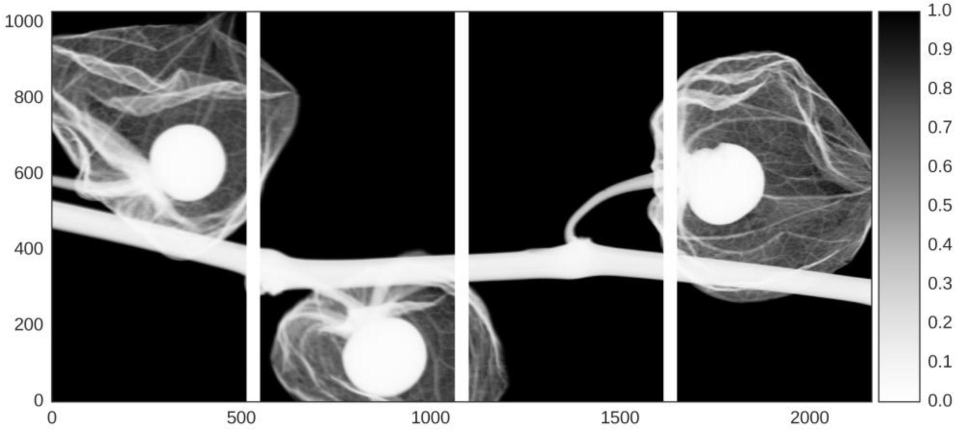
EIGER is a single photon counting detector

65536 pixels/readout chip

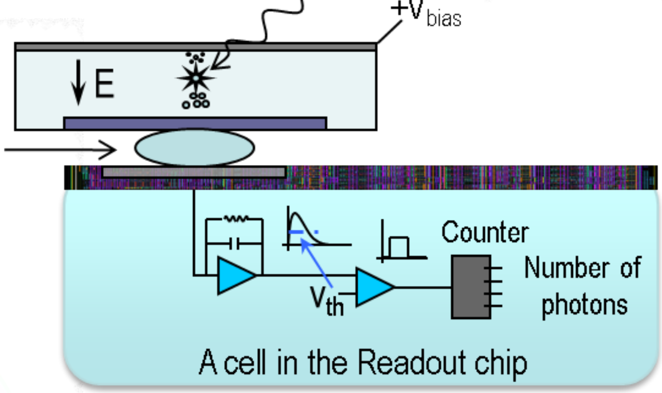
4x2 readout chips/module

Configurable 4/8/12 Bit counter

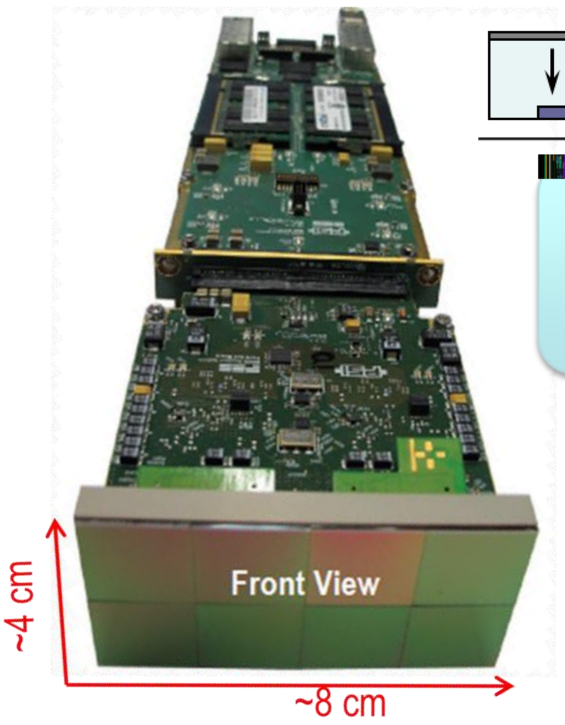
Max. Frame Rate 22/11/5.9 kHz



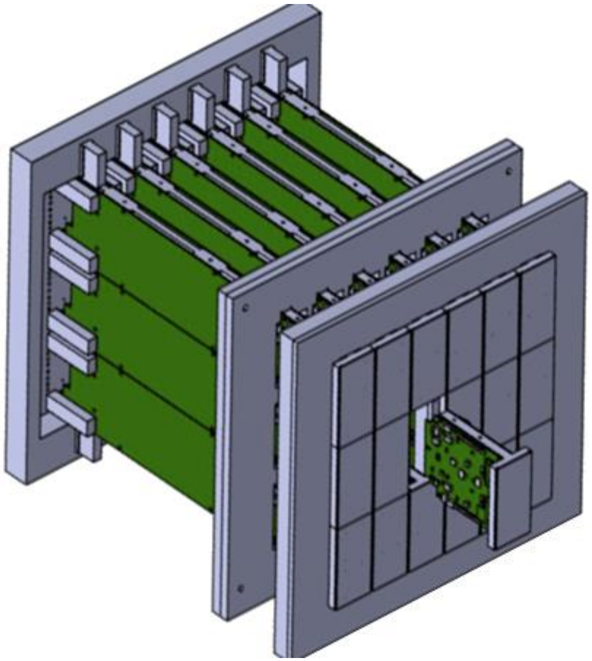
X-rayed flower shot with the 2 Mpixel detector



A cell in the Readout chip

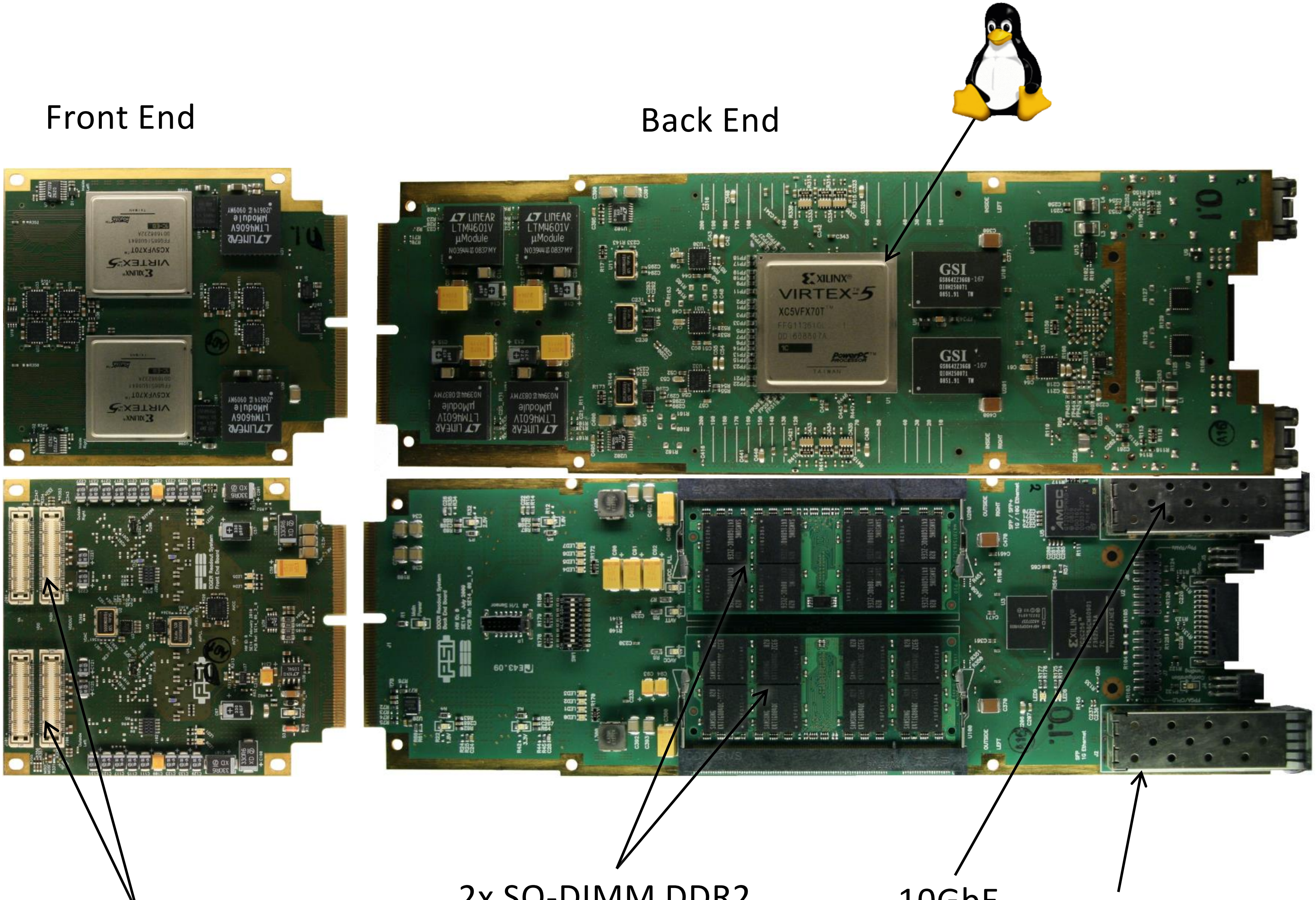


EIGER 500 kPixel Module
(2 Half Modules)



9MPixel Detector
18 Modules/36 Half Modules

The EIGER Detector – Readout Hardware



Front End

Back End

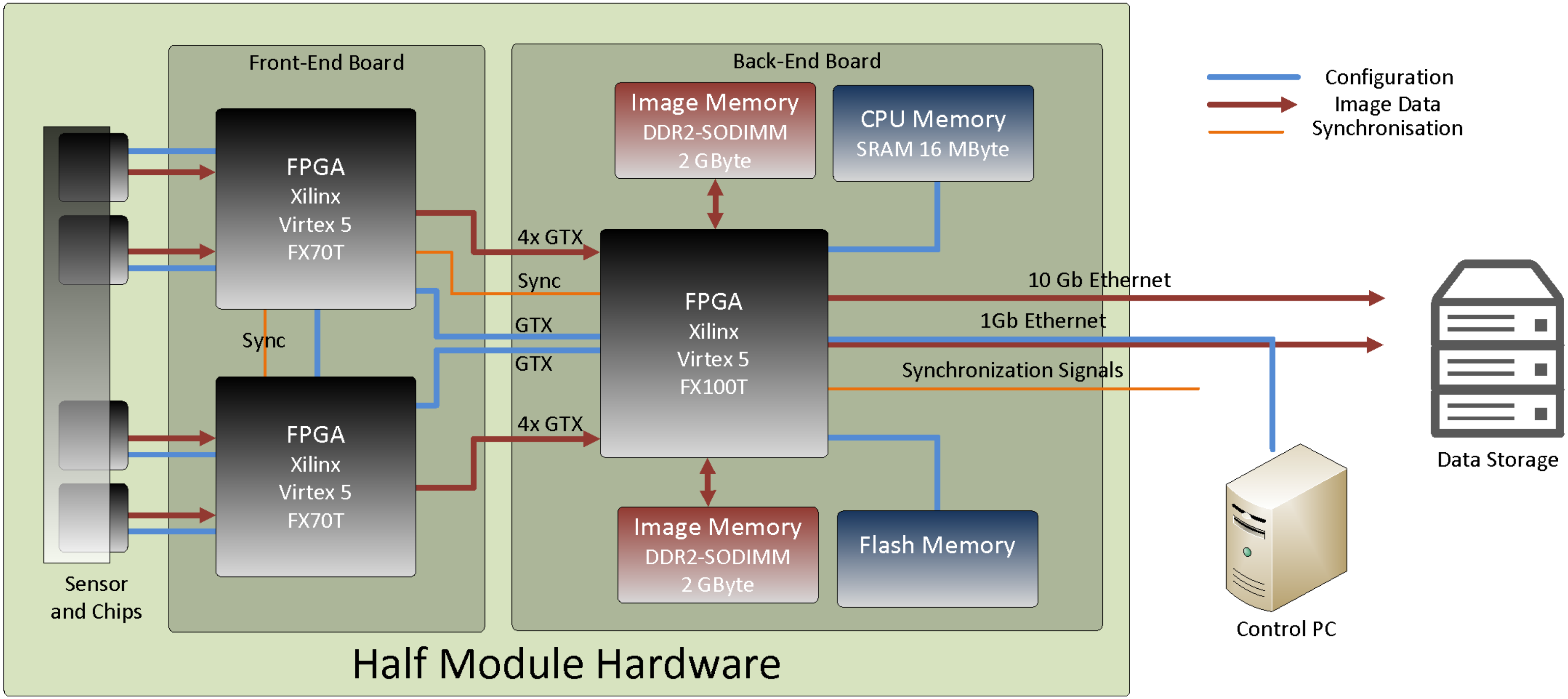
Read out chips connectors
2 chips per FE-FPGA

2x SO-DIMM DDR2
Memory

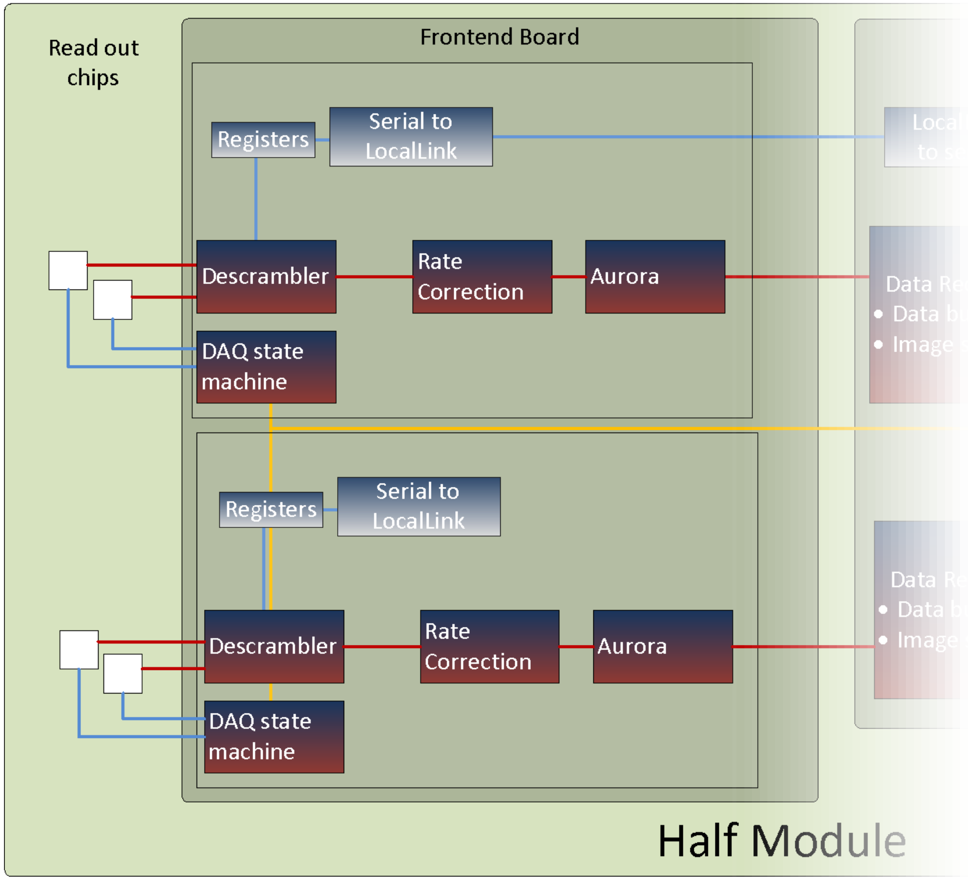
10GbE

1GbE

The EIGER Detector – Readout Hardware



Firmware – Overview Frontend Board



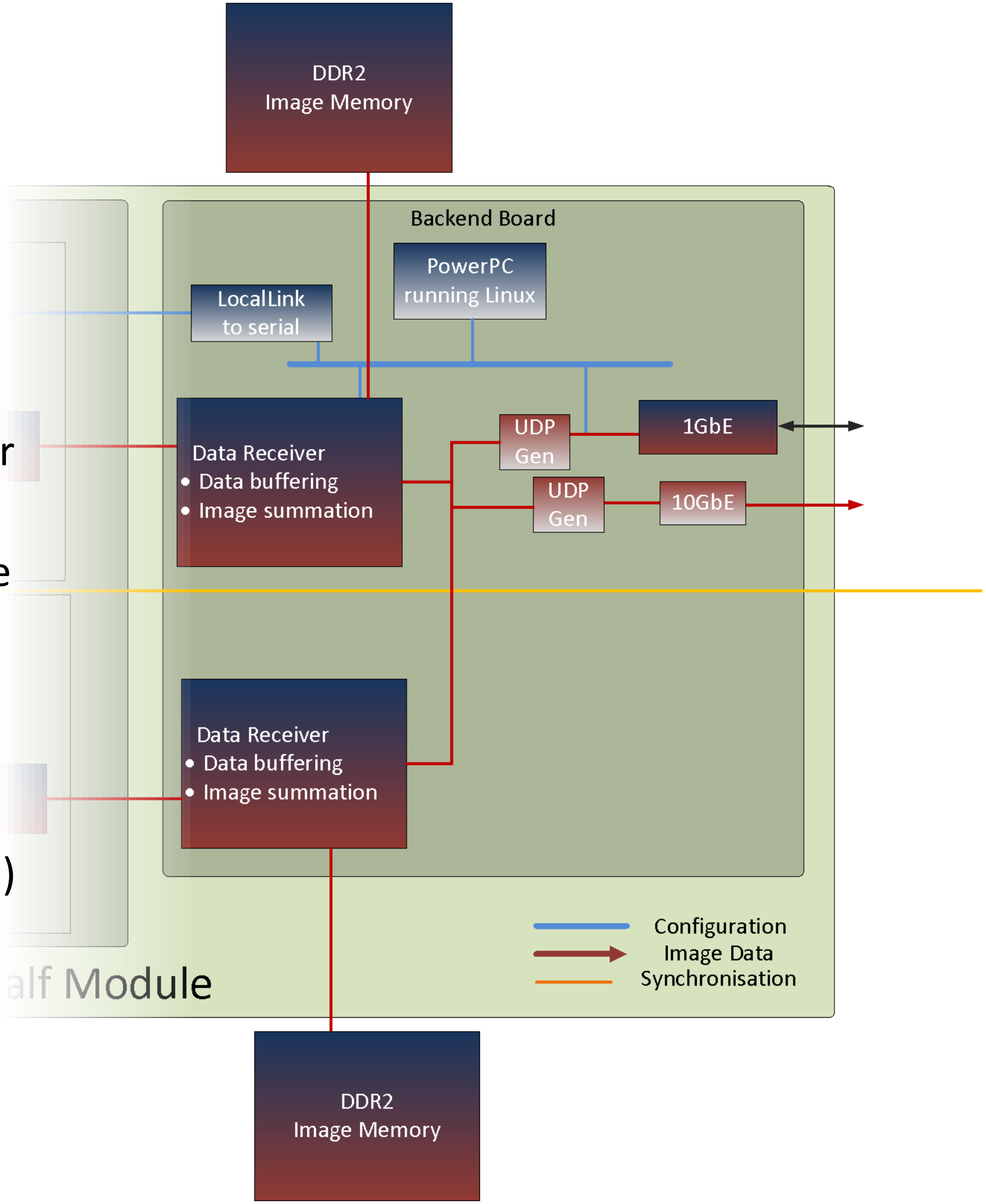
Front End Board FPGAs

- DAQ state machine
- Synchronization between the 2 front end FPGAs
- Descrambling (32 lines per readout chip)
- Rate Correction
  - Look Up Table
  - Interpolation
- Frame data send to BEB over GTX
- Chip read out max frequency is 200 MHz (6Gbit/s)
- Min. Dead time 4µs

Firmware – Overview Backend Board

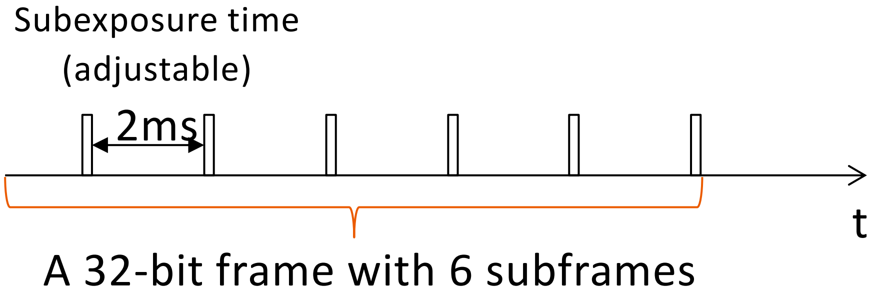
Back End Board FPGA Firmware

- PLB based processor system
  - Linux
  - Self-made Software
  - TCP communication to Server
- Independent data paths for image data from left and right front end FPGAs
- DDR2 memory used for
  - Data buffering (2k-8k images)
  - Image summation
- UDP packet generator for 1GbE and 10GbE (bypassing CPU)



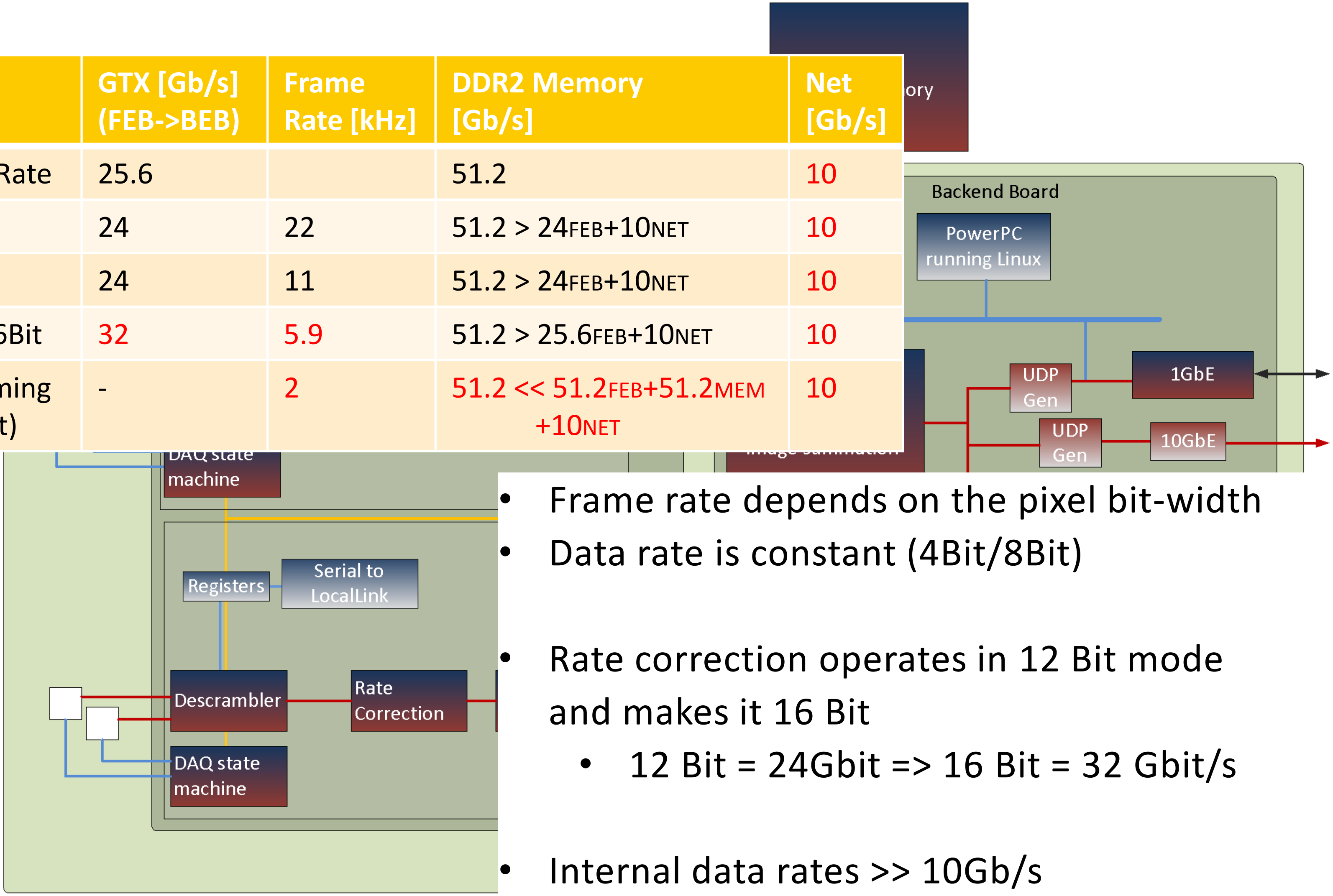
Firmware – Image Summation

- Increases the dynamic range to 32 bit
- Allows longer exposures
- Subframes send from the FEB to the BEB, stored and summed up in memory
- Rate correction is applied on this subframes
- Only resulting image is sent to the server



Firmware - Data Rates

	GTX [Gb/s] (FEB->BEB)	Frame Rate [kHz]	DDR2 Memory [Gb/s]	Net [Gb/s]
Max Rate	25.6		51.2	10
4Bit	24	22	51.2 > 24FEB+10NET	10
8Bit	24	11	51.2 > 24FEB+10NET	10
12/16Bit	32	5.9	51.2 > 25.6FEB+10NET	10
Summing (32Bit)	-	2	51.2 << 51.2FEB+51.2MEM +10NET	10



- Frame rate depends on the pixel bit-width
- Data rate is constant (4Bit/8Bit)

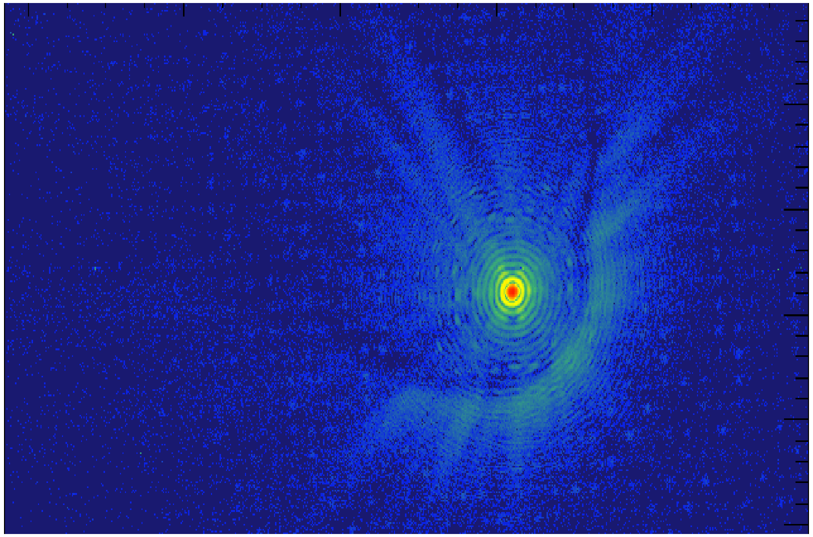
- Rate correction operates in 12 Bit mode and makes it 16 Bit
  - 12 Bit = 24Gbit => 16 Bit = 32 Gbit/s

- Internal data rates >> 10Gb/s

- Due to the buffer (2000-8000 images) short high frame rate bursts possible

Data Transmission – Online Compression

Widen the Ethernet bottleneck



EIGER 500k (1 Module)

In normal use case:

- A lot of homogeneous areas which can be compressed quite well
- Simple approach is being implemented in the FPGA
  - Send only pixel differences either as
    - 4bit (if -4 < pixel1-pixel2 < 4)
    - 16bit (else)
    - Unfortunately no result yet, best case packet size reduced to 1/4
- More complex approach:
  - Reshuffle the bits of the pixels: first send the 8 most significant bits for n pixels followed by the 8 least significant bits for n pixels
    - E.g. 0x0013 0x0023 0x009f would become 0x00 0x00 0x00 0x13 0x23 0x9f
  - Compress with LZ4 (Roughly: repeating sequences get a new symbol)

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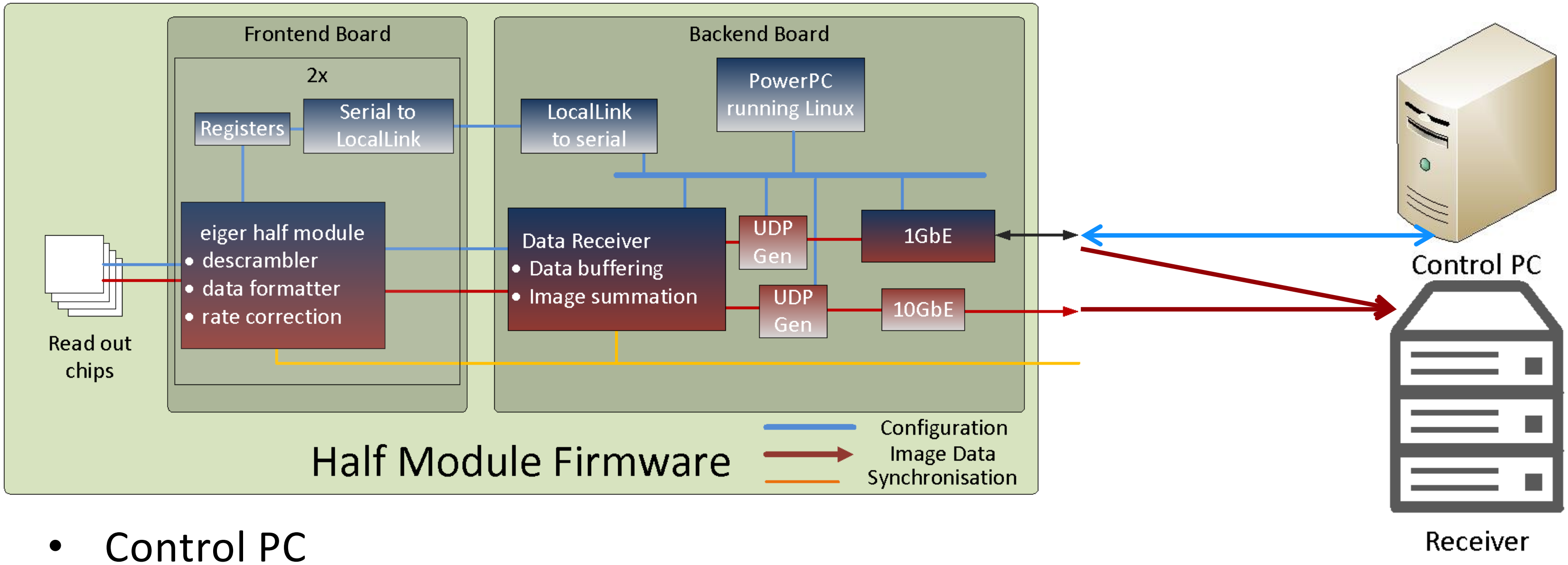
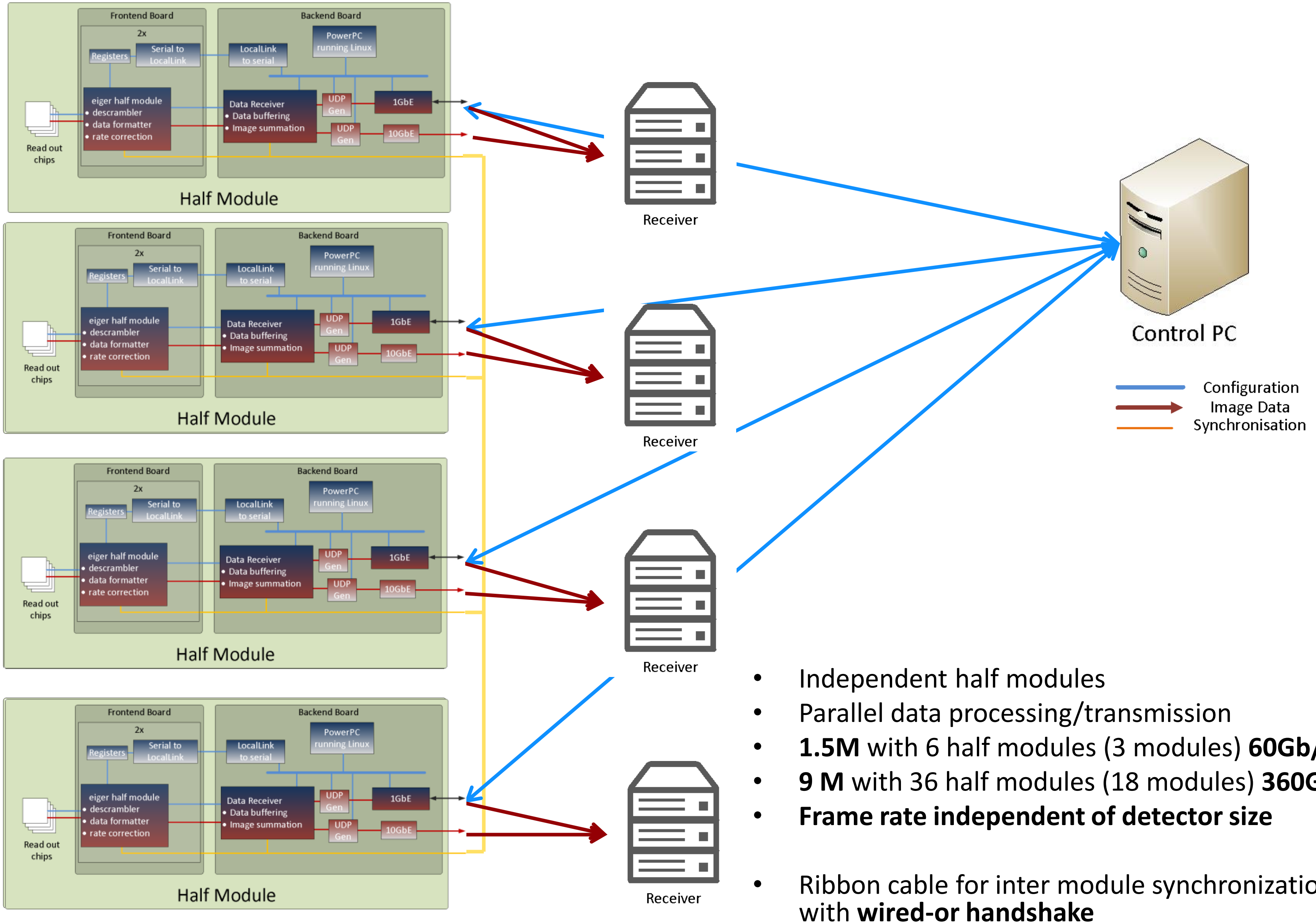
Data Transmission – Half module



- Control PC
  - TCP connection to onboard Linux Software
    - Configures the Detector
    - Writes UDP header for the image data for 1 GbE and 10GbE
    - Slow software controlled connection

- Receiver
  - Receives UDP packets send from the Hardware bypassing CPU either from 1GbE or 10GbE interface and writes them to disk(s)

Data Transmission – Multi-Module



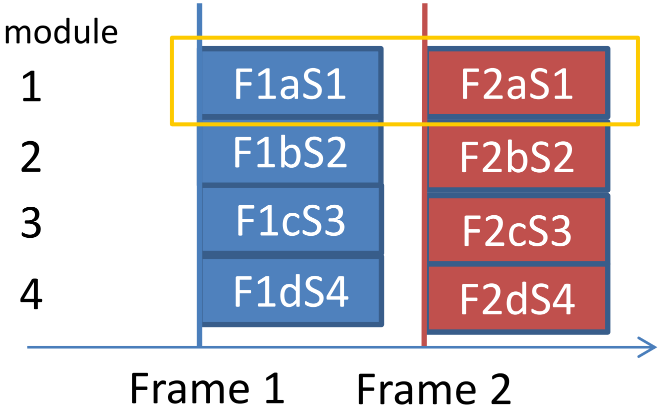
- Independent half modules
- Parallel data processing/transmission
- **1.5M** with 6 half modules (3 modules) **60Gb/s**
- **9 M** with 36 half modules (18 modules) **360Gb/s**
- **Frame rate independent of detector size**

- Ribbon cable for inter module synchronization with **wired-or handshake**

Data Transmission - Round Robin + Delay

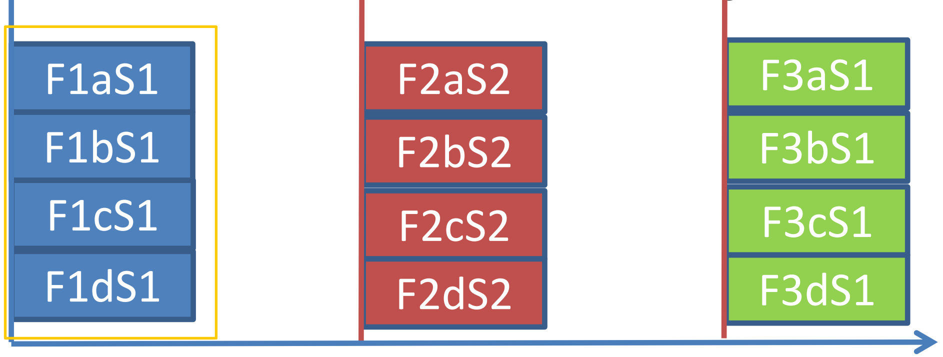
- UDP Header for several Servers stored in FPGA memory
- Address counts on each frame

No Round Robin

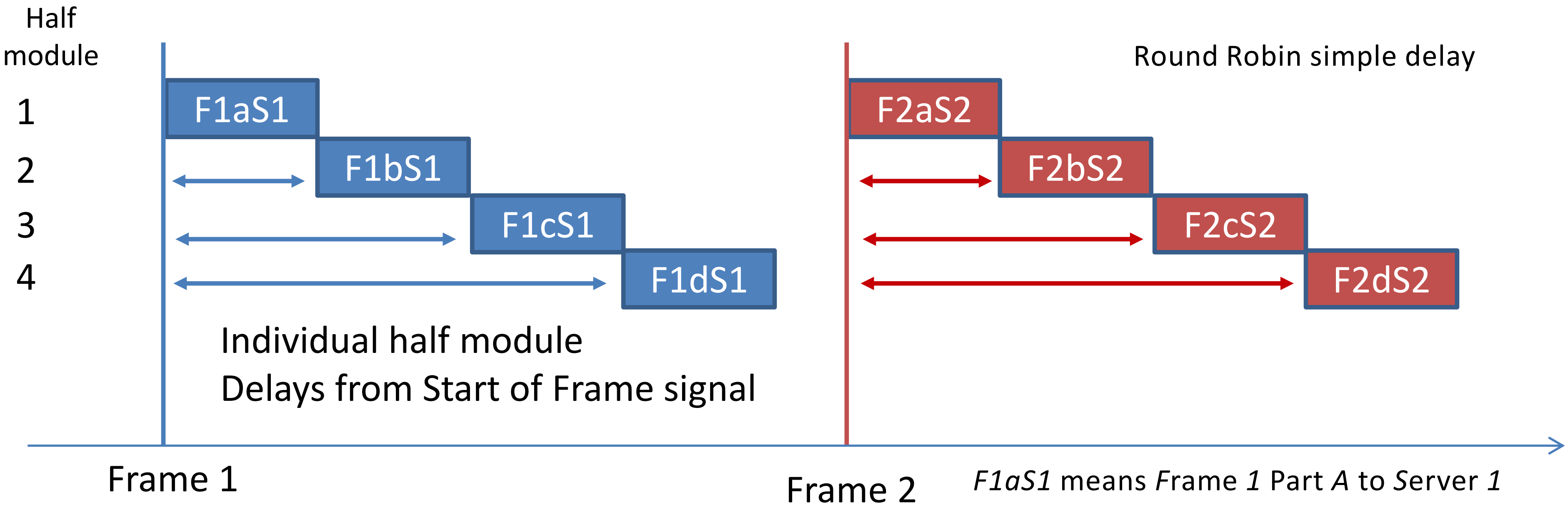


Round Robin without delay

- High CPU load peaks
- Long breaks



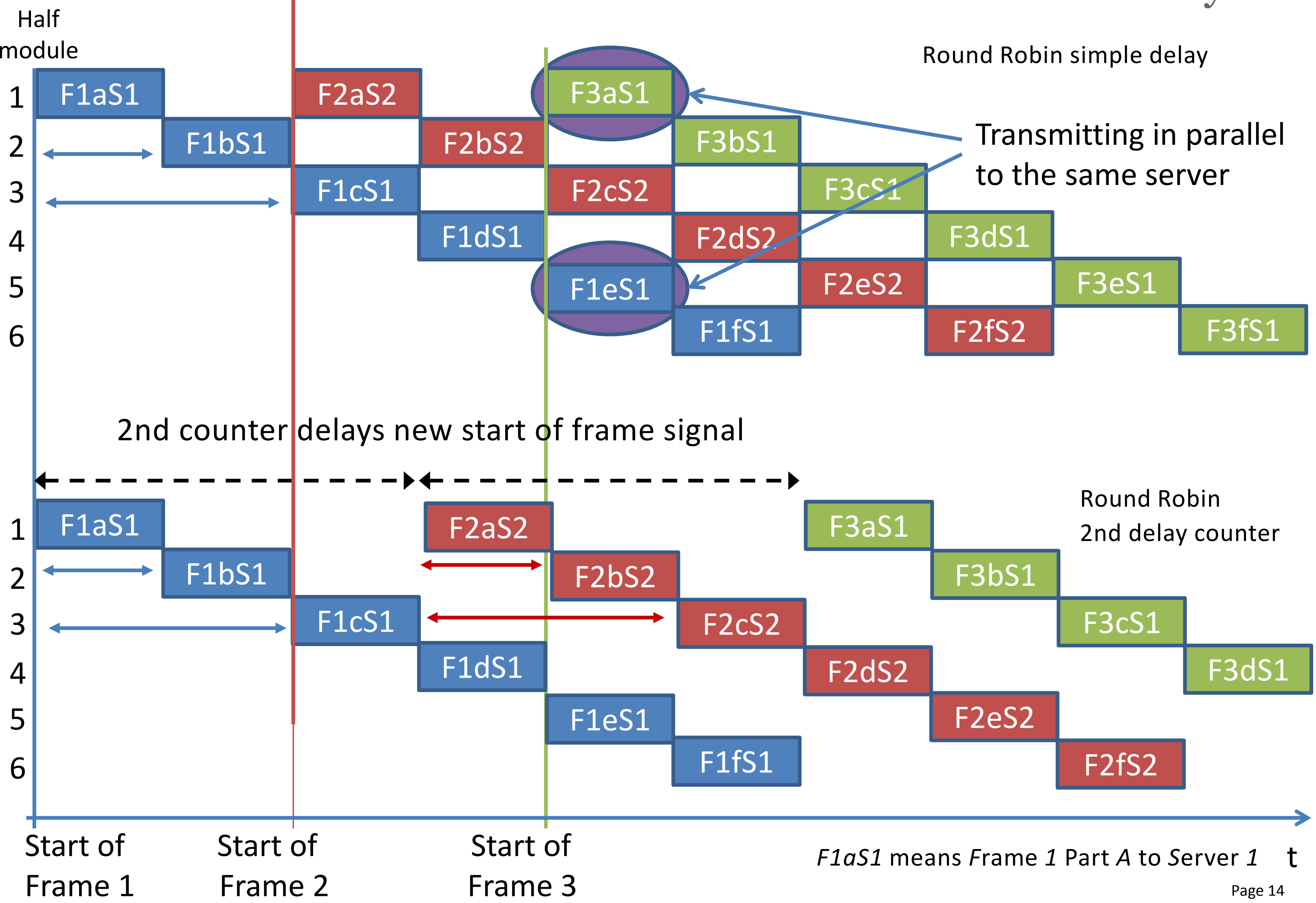
Round Robin simple delay



Individual half module
Delays from Start of Frame signal

F1aS1 means *Frame 1* Part *A* to Server *1*

Data Transmission - Round Robin + Delay



F1aS1 means Frame *1* Part *A* to Server *1*

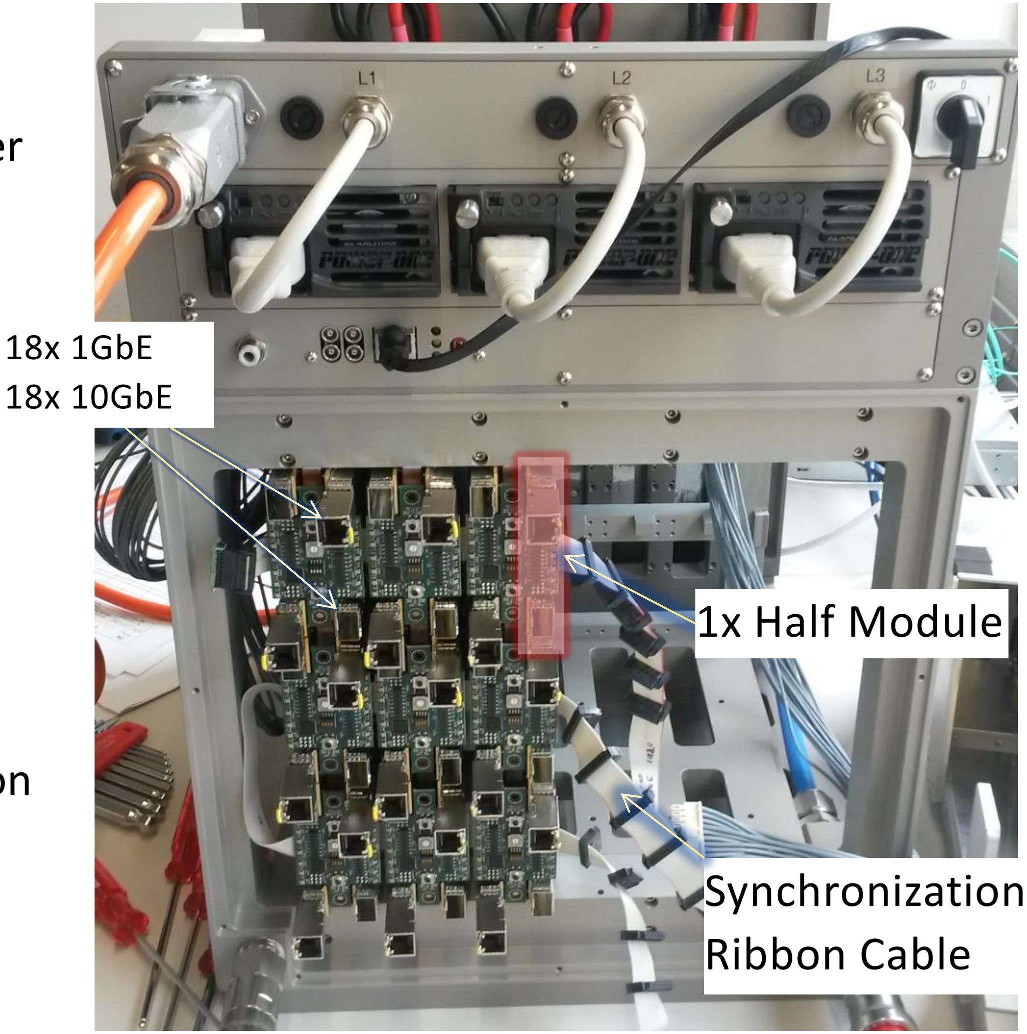
Summary and Outlook

Summary

- Higher dynamic range and longer exposure time with summing
- The EIGER detector is an easy scalable detector due to its independent half modules
- This leads quickly to high data rates
  - Round Robin with Delay helps balancing the data transmission

Ongoing work

- Minimizing bottlenecks
  - Online compression


18x 1GbE
18x 10GbE

1x Half Module

Synchronization Ribbon Cable

9MPixel (18 Modules) case equipped with 9 Modules/18 Half Modules

Thank you

SLS Detectors Group www.psi.ch/detectors/detectors-group

Top Left: S. Cartier, B. Schmitt, D. Mayilyan, D. Thattil, S. Redford, D. Greiffenberg, M. Ramilli, E. Fröjdh, R. Dinapoli, M. Brückner, D. Mezza, C. Ruder, X. Shi, L. Schädler, J. Zhang
Bottom Left: A. Mozzanica, A. Bergamaschi, G. Tinti

Firmware - Synchronization

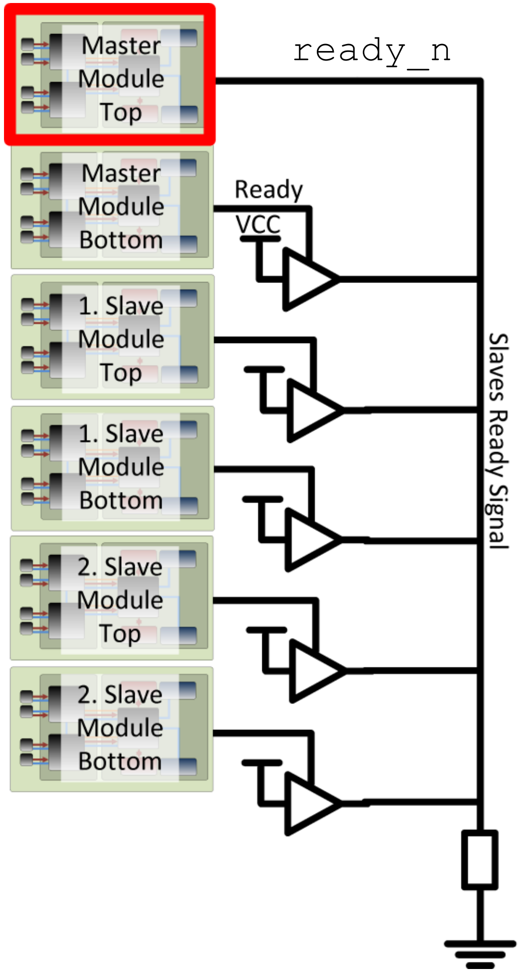
Idle:

- All slaves set '1' to `ready_n` line
- Master gets a '1'

Start acquisition:

1. Master sends "Get Ready for Acquisition"
2. All Slaves get ready and disconnect from `ready_n` line
   Master receives a '0'
3. Master sends "Start Acquisition"
   All half modules receive data

Master and Slave role is software defined



Firmware – Rate Correction

Counting error due to the pile-up effect

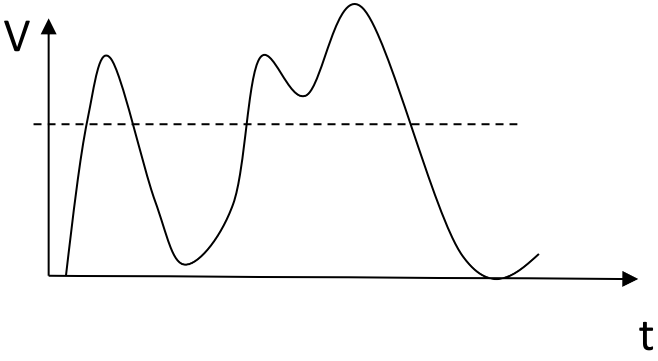
- 2 photons arrive to close to be counted seperatly
- Depends on the gain and the threshold

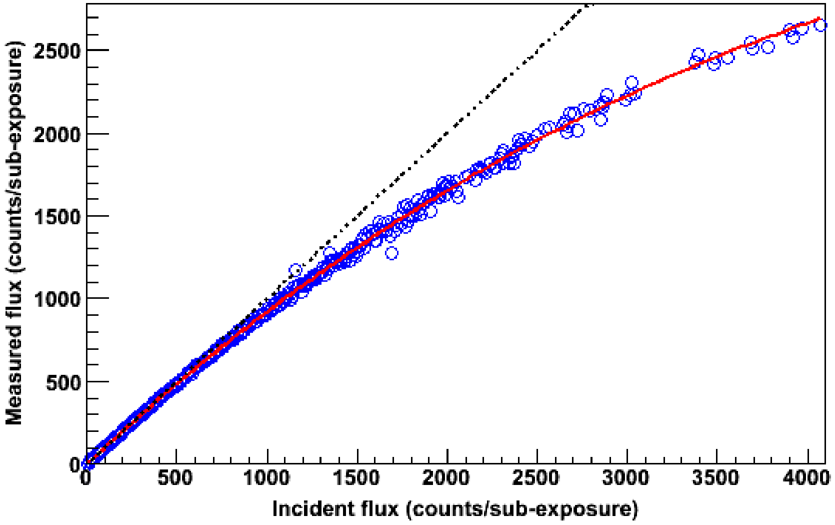
- Can be precalculated for specific gain settings
  - For Eiger: high, medium, low

- Write a r_m to r_i table into FPGA memory (16kByte) interpolating the last 2 bits

$$r_m = r_i e^{-r_i \tau}$$

- r_m - measured rate
- r_i - incident rate
- τ – dead time constant




Measured flux (counts/sub-exposure)
Incident flux (counts/sub-exposure)