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A Testbench Based On UVM Research For ABCstar

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As physicists want to put more and more functionalities and algorithms in frontend ASICs, the logic design (of some ASICs) becomes more complicated. A reliable, robust functional verification testbench is one of the most important part during ASIC design. The full name of UVM is Universal Verification Methodology, which based on SystemVerilog, and it split traditional verification testbench into several hierarchical functional units. It provides the best frame work to achieve coverage-derive verification(CDV). Combining automatic test generation, self-checking to identify undesired behavior, and functional coverage to measure progress and identify non-exercised functionality.
The ATLAS inner tracker detector is being completely rebuilt with an all-new all-silicon detector, which includes inner pixel detector and outer strip detector, for Phase-II upgrade. For the strip detector readout, the chip named ABCStar is under design, which digital part would include two level of buffering, several possible trigger modes, cluster identification and data formatting.
This paper presents the development of a well-constructed, robust testbench by UVM for the ABCStar digital part, including the testbench structure, functional coverage evaluation, comparison of functional results with a reference model.

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