# A Testbench Research Based on UVM for ABCStar

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***Abstract*—As physicists want to put more and more functionalities and algorithms into frontend ASICs, the logic design (of some ASICs) become more and more complicated. A reliable, robust functional verification testbench is one of the most important part during ASIC design.**

**The full name of UVM is Universal Verification Methodology, which based on SystemVerilog, and split traditional verification testbench with several hierarchical functional units, for purpose of reusing and extension. It provides a great frame work for digital ASIC functional simulation and verification. Main features of which including[1]:**

- **Automatic test generation with special constrained randomized stimulus to simulate the real data input activity.**
- **Automatic comparing output result of the Design Under Test(DUT) with a reference model, which has the same function with DUT written by other high-level language like C language, to check the correction of the design.**
- **Automatic collecting desirable functional coverage message to measure progress and identify non-exercised functionality.**

**Also UVM provides a layer to track registers content of the DUT, which is called register model. The register model presents a great convenient way to simulate the action of writing and reading for registers.**

**Furthermore, there is a very powerful self-checking function in SystemVerilog, which is SystemVerilog Assertion(SVA). SVA is simply a checker, which can be used in temporal domain with complex timing or non-temporal domain executing, and to identify undesired behavior of DUT during test.**

**The Large Hadron Collider (LHC) in CERN, is the largest proton-proton collider in the world, which is designed for particle physics research. It has several upgrade projects after its discovery of higgs[2][3]. In Phase-II upgrade, the LHC will run at the center-of-mass energy of 14 TeV, with an integrated luminosity upgraded to $3000\ \mathrm{fb}^{-1}$. To process this unprecedented collision, one of the four big detectors in LHC, ATLAS, whose inner tracker detector is planning being completely rebuilt with an all-new all-silicon detector, including inner pixel detector and outer strip detector[4]. For the strip detector readout, the chip named ABCStar is under design. The main functional modules of digital part of the ABCStar presently including[5]:**

- **An Input Register model, receiving 256-channels hit message from front-end, with functions of enabling any bad or noisy channel to be turned off through a mask register, and different detection models within three bunch crossing clocks.**
- **A trigger controlling model for three trigger data flow controls(L0, LP, PR) according to physicists demands, including two level of buffers for solving these triggers latency.**
- **A cluster finder module to identify all clusters in the data.**
- **A readout module that read out packets with all clusters by sequence through a fast-clock serializer.**
- **A command decoder module for chip reset and internal registers configuration.**

**The full functional blocks diagram of ABCStar showed in Fig. 1. To verifying the design, one of the big challenge we met is**

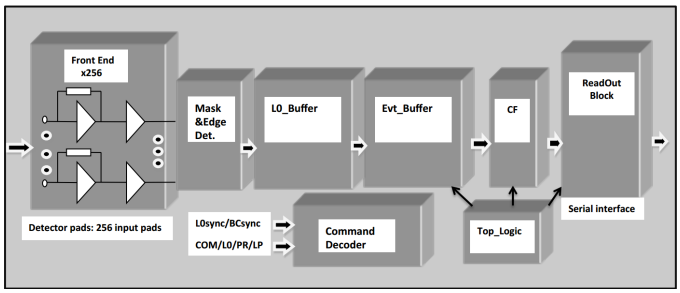


Fig. 1. Block diagram of the ABCStar.

**building reference module. The function of triggers controlling data writing to or reading from buffers, is very difficult to rewritten with a C-like language, since its complex timing. Also another cumbersome part is producing stimulus for all inputs, including 256-channels data input, three trigger signals with special distribute, and commands input to configure the chip, since they are independent with each other in timing.**

**Considering simulating and verifying all these features and functions of the design, we built a testbench based on UVM for it. Main features of the testbench including:**

- **Making five constrained randomized stimulus producing paths for three trigger signals(L0, LP, PR), 256-channels data input, and command input, respectively. In additional, there is a register model for the command path.**
- **Building a reference model with a mixture language of SystemVerilog and C, since systemverilog is profitable in timing modeling, and C has advantage in data processing modeling.**
- **Adding some SystemVerilog Assertions to the testbench, for checking some key functional features of ABCStar in realtime. The functional features that asserted during test including maskbits function that enabling any bad or noisy channel to be turned off, edge detection function, etc.**
- **Building a coverage model, collecting desirable functional coverage message during test. The desirable message includes whether all 256 channels of input data have at least one hit during test, and whether each channel of the input data experiences being turned off with a hit occurring during the test, etc.**

**The structure of the testbench showed in Fig. 2.**

**Based on the testbench we built, we did several tests aiming in verifying the main functions of the design. Including edge detection test, maskbits test, trigger combination test, etc. The**

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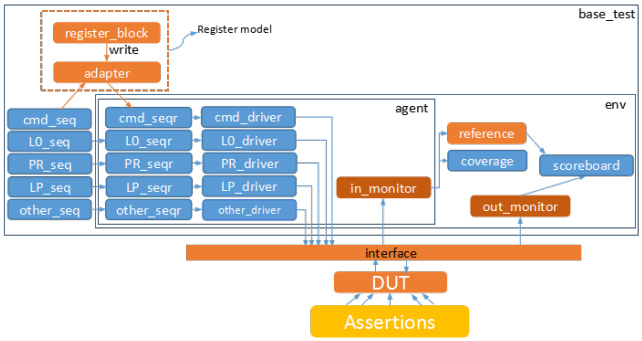


Fig. 2. Diagram of ABCStar testbench based on UVM

**stimulus for each test is special randomized according to tests, to simulate the real input activity.**

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