Upgrade of the Central Logic Board for the Phase-2 of the KM3NeT Neutrino Telescope

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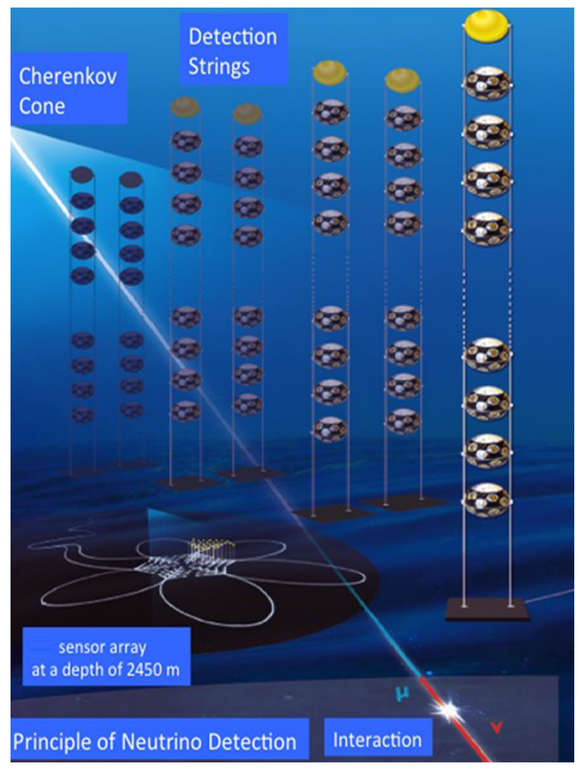
KM3NeT experiment

KM3NeT is an European research facility in the Mediterranean sea which will house a neutrino telescope of cubic kilometer scale. Cherenkov light from secondary particles induced by neutrinos, will be detected by an array of optical modules consisting in high pressure resistant glass vessels with photomultipliers inside. This vessel is called the Digital Optical Module (DOM) and it is composed of 31 small 3 inch PMTs distributed around the glass sphere, which collects the Cherenkov light and transform it into electronic signals. 18 DOMs are arranged on string-like structures anchored on the sea bed and kept vertical by buoyancy system, the so-called Detection Units. The Detection Units are connected with submarine Junction Boxes and through them to shore for power feed and data transmission. The DOM contains a printed circuit board, the Central Logic Board (CLB), which controls the readout systems, the synchronization protocol and the rest of the instrumentation devices.



Central Logic Board

The DOM Central Logic Board (CLB) is the main electronic board in the readout chain of the KM3NeT. The LDVS signals generated by the PMT arrive to the CLB where they are discretized by means of 1ns resolution TDCs. The TDC data is sent to the shore station after being organized and timestamped at the CLB. In order to synchronize the DOMs, the CLB integrates the White Rabbit protocol that provides a global time with 1 ns of resolution. The CLB takes care also of the read-out of several instruments, as it is the case of the compass, tilt meter, temperature sensor, piezo, nanobeacon and the acoustic hydrophone. The main component of the CLB is an Artix-7 FPGA.

Firmware

The firmware of the DOM is based on two LM32 microprocessors, an open source firmware from Lattice. One of them is dedicated to the White Rabbit protocol which directly manages the tunable oscillators and the optical link traffic, in order to achieve a time synchronization of sub-nanosecond level with the Grand Master clock of the on-shore station. The rest of the modules are managed by the second microcontroller, which has access to all the communication interfaces (SPI, UART, GPIO and I2C) needed for the instrumentation devices, the acoustic and optical readout systems and the multiboot module. 31 TDCs are responsible to record the arrival time and the width (with 1 ns of resolution) of the hits incoming from the PMTs. An acoustic readout is dedicated to decode the AES3 formatted input stream. All the data, together with some other slow control monitoring information (as temperature, humidity, tilt meter, compass, currents, etc.) are put in UDP packets and connected to an IP/UDP packet buffer stream selector (IPMUX). This IPMUX splits the data into separate streams, based on UDP port number and sends them to the shore station via the endpoint, a normal Ethernet MAC but it has time stamping capabilities allowing sub-nanosecond timing precision, such that it facilitates the Precision Time Protocol (PTP-IEEE588). The block diagram of the firmware is shown in figure 2.

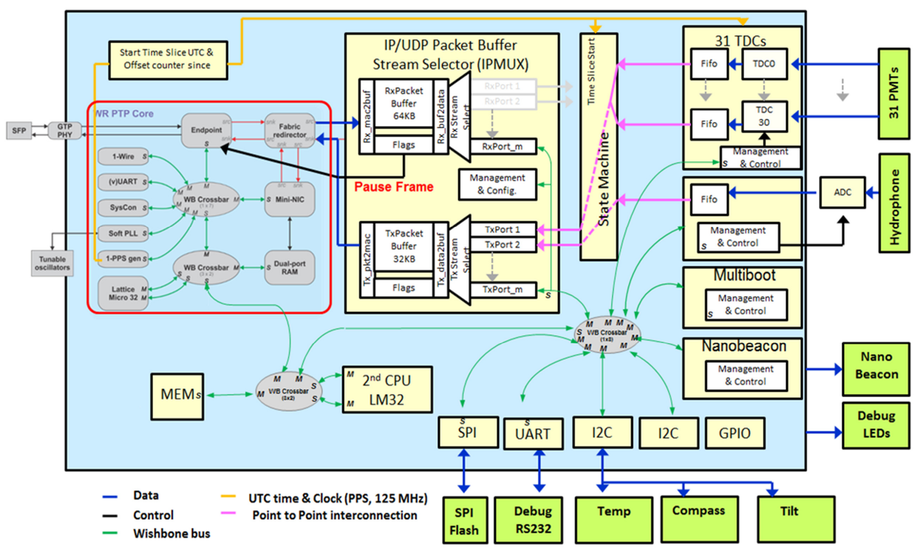


Figure 2. CLB firmware architecture implemented in Artix-7

Tests

Several tests have been done on the CLB by the electronic group of the KM3NeT collaboration. The tests covered all the functionality of the board, and were performed separately, by focusing on the dedicated hardware and firmware sections. The most important tests are about the time synchronization and the optical communication link. The PMT signals acquisition and acoustic module were also analyzed in different conditions of high voltage and plugging the acoustic device to the CLB. Multiboot and the rest of the instrumentation were tested by using a shell command interface.

A thermal analysis was also performed on the board, showing two hot regions near the FPGA and near the SFP connector, having in both cases a maximum temperature of about 40ºC.

Electromagnetic interference analysis was performed on the CLB. The results showed the presence of two hot spots in the center of the board due to DC-DC converters on the power supply board, these hot spots were reduced by inserting a metal plane between the two boards.

Hardware

The CLB has been designed with 12 layers (6 signal layers, 2 power planes and 4 ground planes). The layers are symmetrically disposed around the 2 alimentation layers. Ground planes are positioned at the sides of the signal layers to have better signal integrity. Particular attention was put on the differential pairs routing keeping the time difference less than 100 ps between different PMT signals, and less than 20 ps between clock signals. A reliability analysis using the FIDES method was performed, showing an estimated risk of failure less than 10 % after 15 years. Several signal integrity simulations were performed on different signals on the board, showing a good level discrimination. The CLB and its schematic block are shown in figure 1.

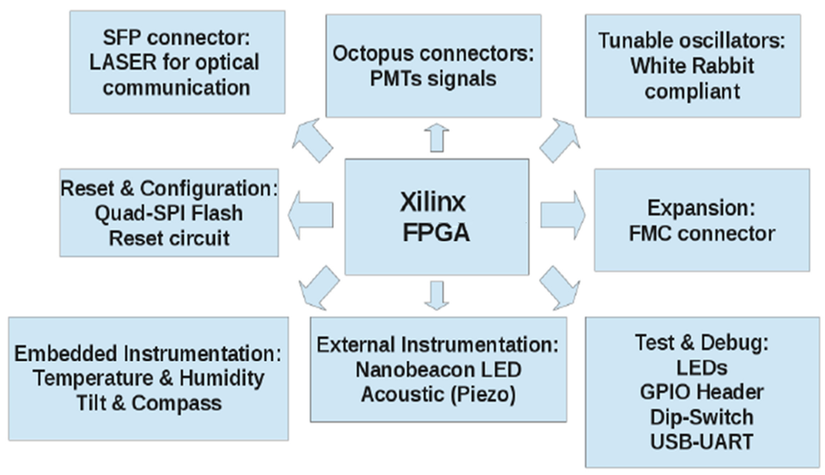


Figure 1. CLB hardware

Software

The control of the DOM is achieved through a complex and robust embedded software running in the LM32. No operative system is used in order to reduce power consumption. The software allows multiple parties to work on it and extending it without compromising stability and clarity. The software has been layered into three main modules, named Common, which contain the common functions, macros and standard libraries. Platform layer, which includes the start-up code and drivers, and Application layer for the specific code for detectors, peripherals and slow control. Figure 3 shows the modular structure of the embedded software.

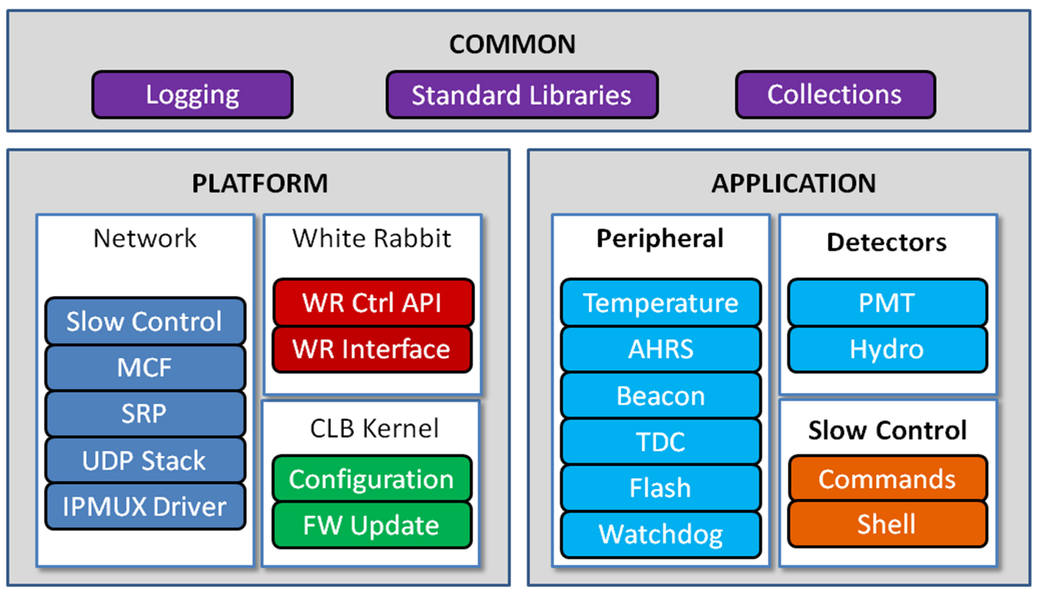


Figure 3. Modules of the embedded software for the CLB