# Upgrade of the Central Logic Board for the Phase-2 of the KM3NeT Neutrino Telescope

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***Abstract*–The KM3NeT Collaboration aims at the construction of a multi-km3 high energy neutrino telescope in the Mediterranean Sea consisting of thousands of glass spheres, each of them containing 31 photomultiplier of small photocathode area. The readout and data acquisition system of KM3NeT has to collect, treat and send to shore, the enormous amount of data produced by the photomultipliers, the acoustics sensor and the rest of the instrumentation. The electronics design includes a multiboot module which allows for the re-configuration of the nodes of the telescope remotely from the shore station. All the modules and subsystems are controlled by two embedded microprocessors, implemented on a Xilinx FPGA, and complex embedded software. The first prototype of Digital Optical Modules based on Kintex-7 has been deployed. The next generation based on Artix FPGA has been designed.**

## I. Introduction

THE KM3NeT neutrino telescope is a deep-sea neutrino infrastructure to be deployed in the Mediterranean Sea. The telescope has been designed to detect extraterrestrial neutrinos with energies above 50 GeV by means of the Cherenkov photons induced by the passage of relativistic charged particles through the seawater [1]. When a neutrino interacts in the material surrounding the detector, it can produce a muon, which travels across the detector at a speed greater than the speed of light in water. Such a particle generates a faint blue luminescence called Cherenkov radiation. The arrival times of the photons collected by optical detectors disposed in a three dimensional array can be used to reconstruct the muon trajectory, and consequently that of the neutrino, which is strongly correlated. The main elements of a neutrino telescope are, therefore, the sensitive optical detectors which in the case of KM3NeT are small photocathode area photomultiplier tubes (PMTs) distributed around the glass sphere of the so called Digital Optical Module (DOM) [2]. Each DOM has 31 small photomultipliers that collect the Cherenkov light and convert it into electronic signals. In order to translate these signals into the arrival time of the photons, they are processed by Time to Digital Converters (TDCs) implemented on an Artix-7 field-programmable gate array (FPGA). A TDC performs conversion of a time interval (TI) into a digital value achieving sub-nanosecond resolution.

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The KM3NeT neutrino telescope uses the all-data-to-shore concept. All digitized photon arrival times (t0) and time over threshold (ToT) that are recorded by the PMTs are sent via an optical fiber network to a shore station, where a farm of processors applies trigger and selection algorithms to reduce the data. This method allows for sophisticated algorithms to filter the overwhelming background by searching for space-time correlated photon hits which are signatures of neutrino interactions. The expected average photon-counting rate of 5-10 kHz per PMT will lead to an outgoing data-rate of a few MB/s per DOM**.**

## II. HARDWARE

The CLB has been designed with 12 layers (6 signal layers, 2 power planes and 4 ground planes). The layers are symmetrically disposed around the 2 alimentation layers. Ground planes are positioned at the sides of the signal layers to have better signal integrity. Particular attention was put on the differential pairs routing keeping the time difference less than 100 ps between different PMT signals, and less than 20 ps between clock signals. A reliability analysis using the FIDES method was performed, showing an estimated risk of failure less than 10 % after 15 years. Several signal integrity simulations were performed on different signals on the board, showing a good level discrimination.

## III. FIRMWARE

The CLB is the responsible to synchronize all the nodes and it is also the main electronic board in the readout chain of KM3NeT. The digitized data are sent onshore after being organized and time stamped. The CLB takes care also of the readout of several instrumentation devices, as it is the case of the compass, tilt-meter, acoustic piezo sensor, LED nanobeacon and temperature sensor, all of them integrated on the same PCB.

The CLB firmware is based on Lattice Mico LM32 embedded microprocessor, an open source firmware microprocessor from Lattice. The system includes two LM32. One of them is dedicated to the White Rabbit protocol which directly manages the tunable oscillators and the optical link traffic, in order to achieve a time synchronization of sub-nanosecond level with the Grand Master clock of the on-shore station. The rest of the modules are managed by the second microcontroller, which has access to all the communication interfaces (SPI, UART, GPIO and I2C) needed for the instrumentation devices, the acoustic and optical readout systems and the multiboot module.

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The CLB is responsible to control the readout systems. For the optic readout, the LVDS signals generated by the PMT bases arrive to the CLB where they are discritized by means of 1 ns of resolution Time to Digital Converter (TDC) based on deserializer primitives. The board includes a 25 MHz crystal oscillator. This clock signal is first transferred from a clock pin to a buffer in the center of the FPGA, and then fanned out to the inner PLLs to provide two high frequency clocks of 250 MHz and 90º phase shifted. A 4-oversampling method increases the sampling frequency up to 1 GHz achieving the desired accuracy of 1 ns for PMT events. The samples produced by deserializers are sent to specific blocks called Data Recovery Units (DRUs) where the data are reorganized and the digital pulse information is computed. The system readout generates an output of 48 bits where the 8 most significant bits are used to encode the PMT identifier, the next 32 bits indicate the time-stamp and the 8 less significant bits are used to digitize the length of the pulse.

The CLB timing reference clock with a 1 ns phase precision and the UTC time are supplied by the White Rabbit PTP Core (WRPC) [3]. The CLB is connected to Ethernet via the 1000BASE-X MAC that is also incorporated in the WRPC. Readout data is transmitted to shore via the endpoint of WRPC. This endpoint is basically a normal Ethernet MAC but it has time stamping capabilities allowing sub-nanosecond timing precision, such that it facilitates the PTP protocol [4].

## IV. SOFTWARE

The control of the DOM [5] is achieved through complex and robust embedded software running in the Lattice Mico LM32 microprocessor. No operative system is used in order to reduce power consumption. The software allows multiple parties to work on it and extending it without compromising stability and clarity. The software has been layered into three main modules, named Common, Platform and Application. The Common layer contains the common functions, macros and standard libraries. The Platform layer includes the start-up code and drivers. Finally the Application layer includes the specific code for detectors, peripherals and slow control.

## V. CONCLUSIONS

Several tests have been done on the CLB by the electronic group of the KM3NeT collaboration. The tests covered all the functionality of the board, and were performed separately, by focusing on the dedicated hardware, firmware and software sections. The most important tests are the time synchronization and the optical communication link. The PMT signals acquisition and acoustic modules were also analyzed in different conditions of high voltage and plugging the acoustic device to the CLB. Multiboot and the rest of the instrumentation were tested by using a shell command interface.

A thermal analysis was also performed on the board, showing two hot regions near the FPGA and near the SFP connector, having in both cases a maximum temperature of about 40ºC.

Electromagnetic interference analysis was performed on the CLB. The results showed the presence of two hot spots in the center of the board due to DC-DC converters on the power supply board. These hot spots were reduced by inserting a metal plane between the two board.

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