HotLink receiver on CompactRIO for the ITER Electron Cyclotron Control System

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***Abstract*—The ITER Electron Cyclotron (EC) System will have a crucial role in the plasma breakdown, central heating and current drive applications as well as control of magneto-hydrodynamic instabilities. Fast events, such as arcs, might occur in the Gyrotrons or in the rest of the EC millimeter-wave components; a protection system capable of switching off the High Voltage Power Supplies in less than few microseconds is therefore needed. During the design of this protection system, the need to implement fast threshold detection on the electrical measurements from the High Voltage Power Supplies was identified. To this end, a custom compactRIO (cRIO) module has been designed and is the subject of this paper. This module includes a HotLink receiver channel, an FPGA and two 16 bit DAC. In order to provide enough flexibility and to allow using the modules on future applications, the available PCB space has been used to house two channel 16 bit ADC and an STM32F756 MCU. The HotLink module delivers the current/voltage measurements from the power supply to the FPGA, which outputs them back in analogue format through the DAC. In parallel these measurements are also evaluated in the FPGA and all the relevant information (e.g. measurement values, system status and alarms) are made available to the cRIO environment through its backplane. The module can also be used with a more general configuration where the two ADCs inputs are used instead of the HotLink receiver (resulting on a significant cost reduction). In both cases, the MCU can be added as mechanism to increase the complexity of the analysis algorithms that are performed over the measured power supply signals. The first prototype of this module is currently being tested, and some results of preliminary tests are presented.**

***Index Terms*—ITER, HotLink, CompactRIO, FPGA, Control System.**

I. Introduction

THE ITER Electron Cyclotron (EC) System will operate at 170 GHz, aiming at pulse durations of up to 3600 seconds. It is comprised of 24 Gyrotrons and it will be used for plasma breakdown, central heating and current drive applications as well as control of magneto-hydrodynamic instabilities, making it a crucial system for the successful operation of ITER. The Gyrotrons will be powered by 12 sets of high voltage power supplies. In order to protect the Gyrotrons and other EC millimeter-wave componets from fast events, such as arcs, a protection system is needed. This system has to be able to switch off the High Voltage power supplies in less than a few microseconds[2]. For this a bespoke hardware solution based in the cRIO framework was developed.

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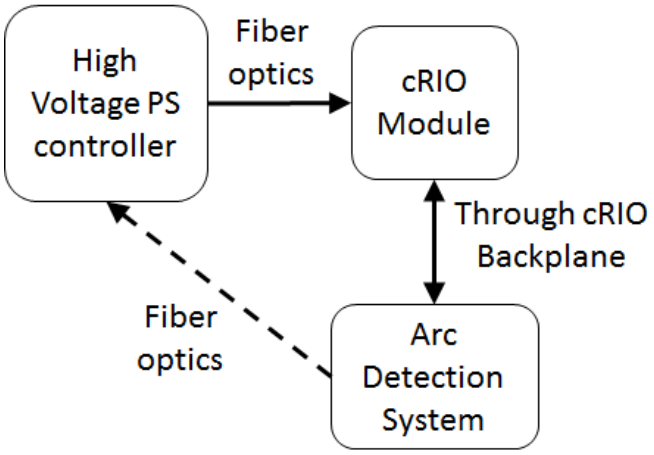

Fig. 1. simplified closed protection loop for the ultrafast protection system for arc detection.

II. Electron Cyclotron Control System

One of the ITER Electron Cyclotron Control System (ECCS) functions will be to provide ultrafast protection. Ultrafast protection functions are established to have reaction times of less than 20μs, and their main purpouse is to protect from event such as arcs in the proximity of the Gyrotrons and arcs in the RF dummy load, diamond window and launchers[2]. There is no Hardware/Software solution for the implementation of these functions from ITER CODAC, since fast PIS is to slow, and FlexRIO is not adequate[1]. A cRIO based solution has been developed for this purpose; it interfaces on one side to the arc detection systems and on the other side to the High Voltage Power Supplies controller, closing a protection loop which guarantees the required performances.

In the case of the high voltage power supplies for the EC gyrotrons, the currents and voltages are measured continuously at 10Msample/s, with a local analogue to digital converter module. This module uses an Hotlink connection to output the data to the cRIO hardware module. The cRIO module receives this digital data and publishes it in one of the DAC available channels providing a replica of the voltage or current measured by the analogue to digital converter present at the power supply. At the same time, this voltage or current value is also published to the cRIO backplane FPGA, through the backplane cRIO connections making it available to the protection system.

III. CompactRIO hardware module

In order to satisfy all the requirements for the protection system, a bespoke cRIO hardware module was designed. The choice of the components was done on the basis of the functional requirements, of cost minimization, but also taking into account the space constraints of the compactRIO form factor and the power consumption limits, which are limited to 1.5 W per module[4]. Also, the solution had to be based on commercial off-the-shelf components.

A. Hotlink connection

The main limitation for the low cost and off-the-shelf components was the Hotlink connection itself, since the technology is somewhat outdated nowadays. This meant that the choice for a receiver chip was very limited. In fact there was only two easily available components, and one of them was a receiver and transmitter. This way the chosen chip was the Cypress CY7B933 Hotlink receiver[3]. For the optical receiver, the options were also very limited, as there was only one receiver capable of withstanding the Hotlink requirements and that could be connected to the Cypress chip without requiring complex interface electronics. The choice was the HFBR-2119TZ from Avago[5].

B. FPGA

The core of the cRIO module is the FPGA itself. The HotLink receiver delivers the current/voltage measurements from the power supply to the FPGA, which outputs them back in analogue format through the DAC. In parallel these measurements are also evaluated in the FPGA and all the relevant information (e.g. measurement values, system status and alarms) are made available to the compactRIO environment through its backplane.

Since there are inumerous options nowadays for very powerfull and full of features FPGAs, some of the main factors for deciding the one used were the power consumption, operating voltage required, footprint and price. The Lattice XO2 family[6] provided a good solution since it is low cost, has low power requirements without sacrificing performance and resources provided, and it is available in packages that are easy to mount in a circuit board (TQFP instead of the standard BGA chips). The choise was for the LCMXO2-2000/4000, 144 pin, TQFP package FPGA.

C. Additional hardware

In order to provide enough flexibility and to allow using the module on future applications, the available PCB space was used to house a two channel 16 bit ADC and an STM32F756 MCU[7]. This way, the module can also be used with a more general configuration where the two ADC inputs are used instead of the HotLink receiver (resulting on a significant cost and power consumption reduction). In both cases, the MCU can be added as mechanism to increase the complexity of the analysis algorithms that are performed over the measured power supply signals.

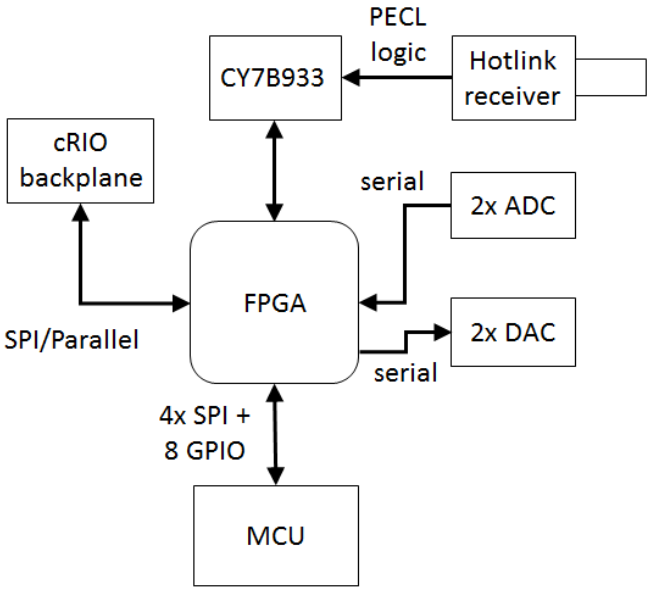

Fig. 2. cRIO module connection diagram.

IV. Preliminary tests and results

Preliminary tests were made, in order to validate the initial component selection, but also project design choices. Several different tests were made, namely measurement of the output waveforms vs. the input waveforms, measurement of the latency between the input signal and the output signal, and overall power consumption.

A. DAC output

For this test, a proprietary analogue to digital conversion module with an Hotlink output connection was used[8]. This module is the same that will be used by the power supply manufacturer, and thus allowed to test the DAC output in close to real conditions. When using a sinus wave input signal, the output of the DAC presents a very good representation of the

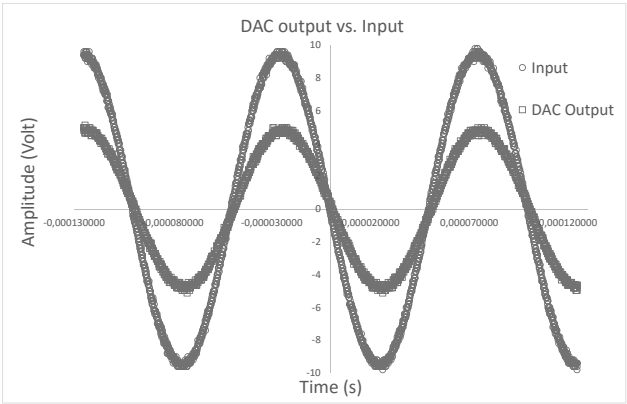

Fig. 3. DAC output vs. the input signal.

input analogue signal, regardless of a conversion scale factor due to the different analogue range and resolution for the ADC and DAC.

B. Latency measurement

The same analogue to digital conversion module was used in order to perform this test, but in this case, a square wave signal was used. From the plot we can see that the delay between the input signal and the DAC output is roughtly 1μsec, which is acceptable since the ADC is working at 10Msample/sec vs the DAC output working at 5Msample/sec.

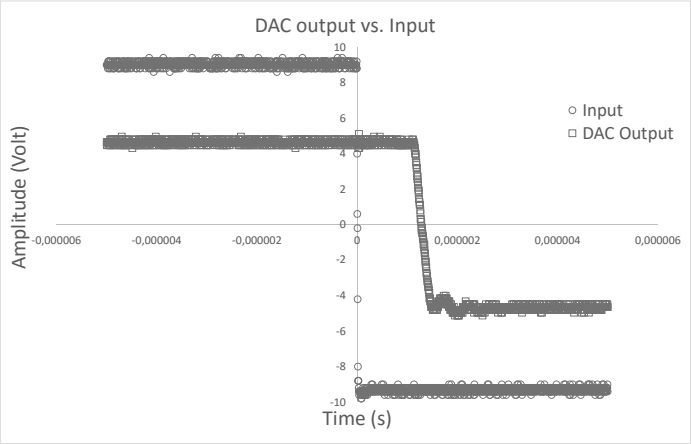

Fig. 4. Delay measurement between the Input signal and the DAC output

C. Power consumption

A very simple power consumption test was made using a shunt in the power supply line to the module. The first time this test was made the measured power was roughtly 1.8W, thus surpassing the cRIO limit. Since the main cause for this power consumption were the Hotlink components, a strategy to minimize it was adopted. The first step was to minimize the current in the PECL communication lines between the Cypress chip and the optical receiver. Increasing the polarization resistors to three times their value meant a three time decrease in the current, thus the same decrease in power. The second step was to change the signal detect line. Since this signal does not need to be has fast as the data lines, the polarization scheme was altered to only one 1kΩ pulldown resistor in each line.

These two changes to the circuit electronics decreased the overall power consumption to only 1.3W, well bellow the cRIO limit.

V. Conclusion and future work

Preliminary testing validated the choice of components and the design strategy. Moreover, the use of almost real conditions for the testing (using the same analogue to digital conversion module and a cRIO backplane), also provided a very usefull way of testing the firmware development, especially the connection to the cRIO backplane. Future work comprises the ongoing firmware development, but also the MCU and DAC connection to the FPGA. Moreoverthere will be some minor modification in the circuit design. In the next version of the prototype the connections between the FPGA and the MCU will be a double quadSPI connection plus eigth GPIOs.

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