A coprocessor for the Fast Tracker Simulation

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Introduction

The Fast Tracker (FTK)[1], an ATLAS upgrade, executes real time tracking for online event selection exploiting maximum parallelism and pipelining. The ATLAS detector records the hit positions of charged particles traversing its volume. These hits constitute an image (an event), and the job of FTK is to analyse the image and reconstruct the tracks of these particles in real time. Track reconstruction is executed in two steps: the Associative Memory (AM)[2][3] first implements a pattern matching (PM) algorithm by recognizing track candidates at low resolution. Then the Track Fitter (TF), implemented in FPGAs (Field Programmable Gate Arrays), performs Track Fitting in full resolution.

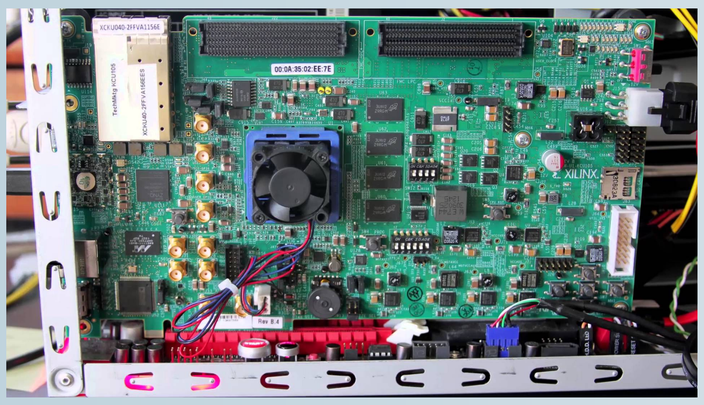
The use of such parallelized architectures for real time event selection opens a new huge computing problem related to the analysis of the acquired samples. For each kind of implemented trigger, millions of events have to be simulated to determine with a small statistical error the efficiency and the bias of that trigger. The AM chip emulation is a particularly complicated and time-consuming task.

The use of a hardware co-processor in place of its simulation can solve the problem. We report about a new compact embedded system for tracking simulation. It is a miniaturization of the complex FTK processing unit, suited for other High Performance Computing applications, as well.

Development Board

Xilinx KCU105 evaluation board

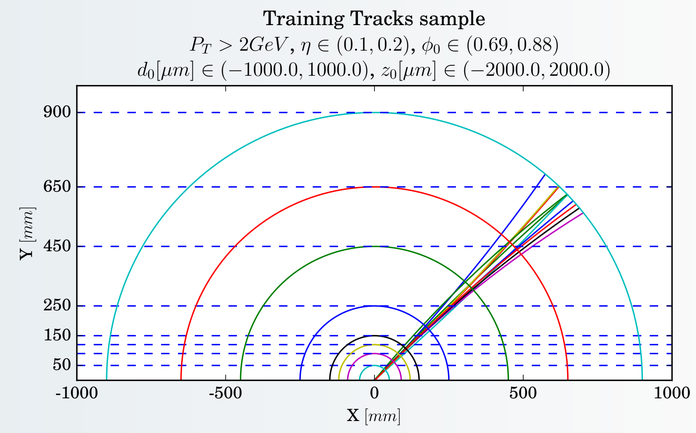
- Kintex-7 Ultrascale FPGA
- 2 FMC connectors for the PM mezzanine
- Ethernet and PCI interfaces for the PC



Xilinx FPGA development board

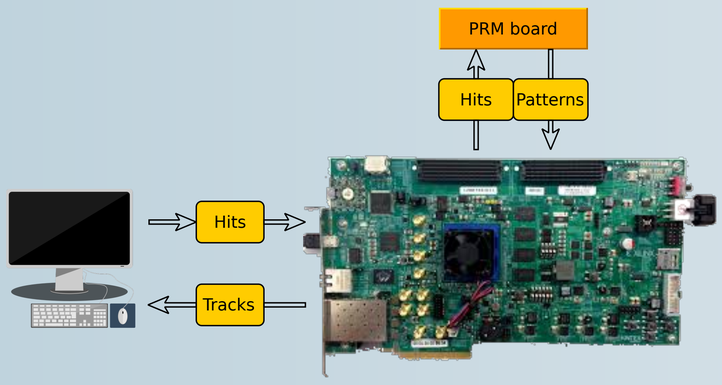
Toy detector model

- Stand-alone Python application
- Implements a "toy" detector model
  - Emulates barrel section of a detector
  - 3 inner layers resemble pixel detectors
  - 5 inner layers resemble strip detectors
- Helical tracks, described by 5 parameters
  - A linear fit[5] is used to compute parameters from full resolution local coordinates
- The application produces input vectors and hardware testing configuration
  - Tracks, layer intersection coordinates (hits)
  - Pattern bank for pattern matching
  - Linear fit constants for track fitting
- Produces plots from the hardware results



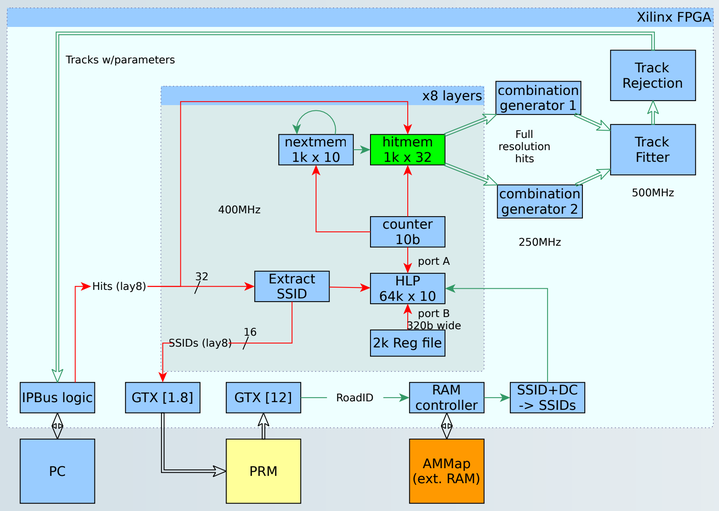
Cross-sectional view of cylindrical "Toy" detector layers, 10 random tracks confined in a very narrow region are shown (see plot title for exact ranges). The region shown is used for the tracks in the "vs Occupancy" plots, shown below.

Data flow



1. The PC sends hits to the FPGA board
2. The FPGA computes SuperStrips (SS) used for PM and stores the corresponding hits
3. SS data are sent to the PM mezzanine
4. Pattern matching results (roads) get read back from the PM, into the FPGA
5. A RAM module used as a look-up-table decodes each road to a list of SS
6. Hits associated with the SS list are retrieved
7. From the hits of each road, all possible track-forming combinations are generated
8. A linear fit is computed for each combination, using the appropriate fit constants
9. Combinations get approved or rejected according to the χ^2 value of their fit
10. Good combinations (tracks) are sent back to the PC

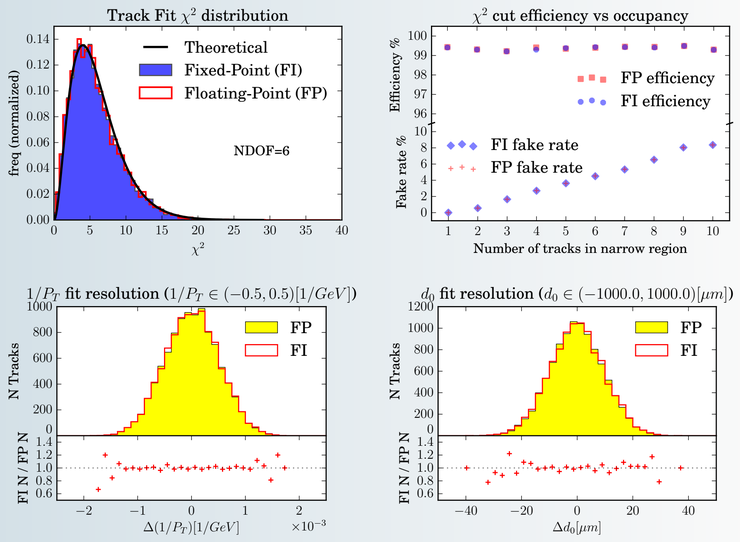
Firmware description and features



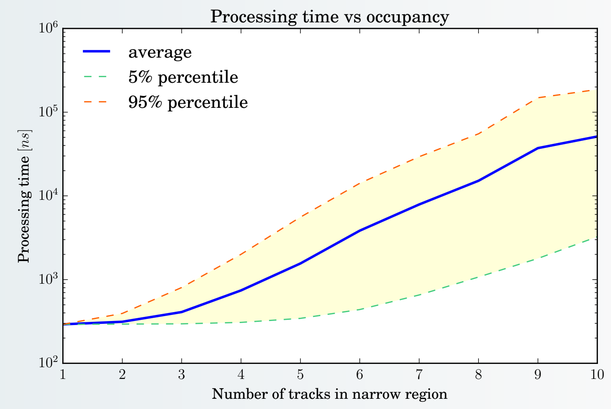
Simplified FPGA firmware block diagram

- IPBus handles Ethernet communications
- Data Organizer: Central component[4]
  - Up to 8 output ports in parallel
  - Can ignore up to the last 3 bits of SS
  - Fully supports patterns with missing layers
- Combination Generator
  - Handles one combination / clock cycle
  - 2 units feed 1 Track Fitter
- Track Fitter
  - Handles one combination / clock cycle
  - 4 units can fit to give 2GFits/s performance

Fixed-point HW fit resolution



Processing performance



Processing time vs occupancy, expressed by the # of tracks/event in a narrow region (see tracks plot, above); to generate each data point many events are processed, until the target of 10000 tracks per point is reached

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Acknowledgments

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