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A hardware implementation of the Levinson routine in a radio detector of cosmic rays to improve a suppression of the non-stationary RFI

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Radio detector of the ultra high-energy cosmic rays in the Pierre Auger Observatory operates in the frequency range 30-80 MHz, which is often contaminated by the human-made RFI. Several filters were used to suppress the RFI: based on the FFT, IIR notch filter and FIR filter based on the liner prediction. It refreshes the FIR coefficients calculating either in the external ARM processor, internal soft-core NIOS processor implemented inside the FPGA or hard-core embedded processors (HPS) being a silicon part of the FPGA chip.
Refreshment times significantly depend on used type of calculation process. For stationary RFI the FIR coefficients can be refreshed each minute or rarer. However, an efficient suppression of non-stationary short-term contaminations requires a much faster response. FIR coefficients calculated by an external ARM take several seconds, by NIOS on the level of hundreds milliseconds. The HPS allows a reduction of refreshment time to ˜20 ms (for 32-stage FIR filter). This is still not too long.
A symmetry of covariance matrix allows using much faster Levinson procedure instead of typical Gauss routine solving a set of linear equations.
The Levinson procedure calculated even in the HPS takes relatively a lot of time.
A hardware implementation this procedure inside the FPGA fabric as specialized
microprocessor requires only ˜40 000 clock cycles. By the 200 MHz ADC and global FPGA clock, this corresponds to ˜200 us - 2 level of magnitudes less than for the HPS.
We practically tested this algorithm on the radio-detector Front-End Board
and compared with the previous approaches: FFT, IIR, NIOS and HPS.
As a signal source was used the Butterfly antenna with the LNA used in the
Auger Engineering Radio Array.

The code has been implemented into several various chips for a comparison
of speed, resource occupancies, however, a target is Cyclone V E FPGA
5CEFA9F31I7 used in the Front-End Board for the Pierre Auger radio detector.
The FIR filter should operate in the fly, it means with the same clock as ADCs.
In order to avoid aliasing, according to Nyquist rule the sampling frequency should be at least twice higher than the higher frequency in the signal spectrum. The spectrum is formed by the band-pass filters to 30-80 MHz. Selected sampling frequency in the radio detectors is 200 MHz.

The hardware Levinson procedure does not need to operate with the same ADC clock, however, it is recommended to avoids temporarily memories.
The 200 MHz speed has been achieved in the StratixIII FPGAs (speed grade - 2).
Cyclone V (speed grade - 7) needs some more optimizations and probably
additional pipeline stages. Nevertheless, the algorithm operating with lower clock then 200 MHz can be used also in the FIR filter. 180 MHz obtained at present in Cyclone V enlarges a refreshment time on ˜10% only.
We plan to test the algorithm in real radio stations in Argentinean pampas.

Author: SZADKOWSKI, Zbigniew (University of Lodz)

Presenter: SZADKOWSKI, Zbigniew (University of Lodz)

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