

A hardware implementation of the Levinson routine in the radio detector of cosmic rays to improve a suppression of non-stationary RFI Zbigniew Szadkowski¹ IEEE Member, for the Pierre Auger Collaboration ¹ University of Łódź, Poland

ABSTRACT

The radio detector system for ultra high-energy cosmic rays in the FFT, IIR notch is often contaminated by human-made RFI. Several filters were used to suppress the RFI: based on the FFT, IIR notch filter and FIR filter based on the linear prediction. The last refreshes the FIR coefficients calculating either in the external ARM processor, internal soft-core NIOS[®] processor, in of the FPGA chip. Refreshment times significantly depend on the type of calculation process. For stationary RFI, the FIR coefficients can be refreshed each minute or rarer. However, an efficient suppression of non-stationary short-term contaminations requires a much faster response. Calculations of FIR coefficients in an external ARM take 1-2 seconds, by the soft-core virtual NIOS[®] processor on the level of hundreds milliseconds. The HPS allows a reduction of refreshment time to \$\sim\$20 ms (for 32-stage FIR filter). A symmetry of covariance matrix allows one to use the much faster Levinson procedure instead of typical Gauss routine for solving a set of linear equations. The Levinson procedure calculated even in the HPS takes relatively a lot of time. A hardware implementation of this procedure inside the FPGA fabric as specialized a micro-controller requires only ~53 800 clock cycles. We used 64- or 48-bit floating-point representations to calculate FIR coefficients. Resources occupation is relatively high, as the design was optimized for a maximal register performance. However, the RFI suppression is very efficient. We expect significant suppression of even short-term non-stationary RFI.

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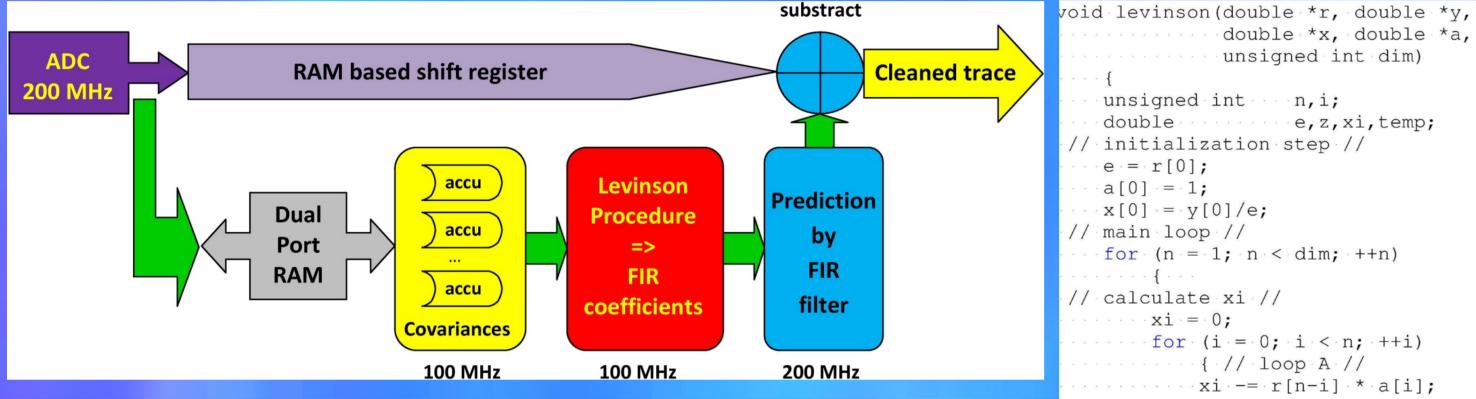
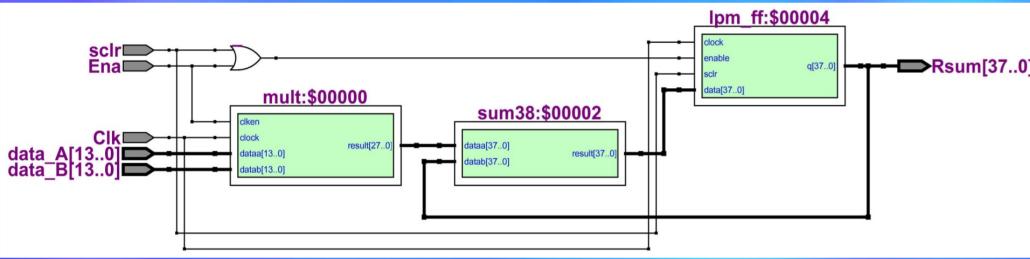


Fig. 1 – The structure of data flow for the hardware implementation of the Levinson algorithm.



				{ // loop C //	01101	13 C1B96528E4000000	01101	13 C1B96528E40	\sim			28440296	01101	13 3FA35	D93444F276E	01101	13 3FA3
Loop A	Loop B	Loop C	Loop D	z = r[n-i] * x[i];	01110	14 419DB827E0000000 15 41B76BF048000000	01110	14 419DB827E00 15 41B76BF0480	0 XL15	$\mathbf{J} = \mathbf{BF9}$	983FF4	4DØ5F382	01110		F7128440292	01110	14 BFA
xi = 0;	a[1] = 0;	z = y[1];	x[1] = 0;	// update x //	10000	16 C1AB4D57E8000000	10000	16 C1AB4D57E80		1 = 3FA	C197FI		10000		3FF4D05F369 97FE3E98D5F	01111 10000	15 BF99
n=1 xi -= r[1] * a[0];	a[1] += a[0] * xi;	z = r[1] * x[0];		x[n] = 0;	10001	17 C1B3CBAEF4000000	10001	17 C1B3CBAEF4				C9FFF32C 074CCE1D	10001	17 3F84F2	268C9FFF333	10001	17 3F84
xi /= e;		pm = z/e;	x[1] += a[0] * pm;	<pre>for (i = 0; i <= n; ++i)</pre>	10010	18 41B2E8BDDA000000 19 41AD8BC7A8000000	10010	18 41B2E8BDDA 19 41AD8BC7A8	300 ×L19	1 = 3F7	547581	B4FFEA3A	10010		046074CCE1A 758B4FFE9FA	10010	18 BFA
	a[2] = 0;	z = y[2];	x[2] = 0;	x[i] += a[n-i] * z/e;	10100	20 C1B6D549B0000000	10100	20 C1B6D549B00	00 ×[20	1] = 3FA 1 = DPQ		05997661 7C08D25C	10100		A2605997662	10100	20 3FA
	a[2] += a[0] * xi;	z = r[2] * x[0];			10101	21 C1A16A85D6000000 22 41B9256DD6000000	10101	21 C1A16A85D6 22 41B9256DD60				DØ4D720D	10101		BB29C08D23E	10101	21 BF94
	a[1] += a[1] * xi;	z = r[1] * x[1];		return;	10111	23 41803AC34000000	10111	23 41803AC3400	o x[23	1 = 3FA	15495)	DC86954A	10110		3BAD04D721C 495DC86952D	10110	22 BFA
xi /= e;	,	pm = z/e;	x[2] += a[0] * pm;	· · · · }	11000	24 C1B9AF60D1000000 25 41932CDD44000000	11000	24 C1B9AF60D10 25 41932CDD440				03DE1B5D CA51A5F5	11000	24 3FA56	00703DE1B6A	11000	24 3FA
	a[3] = 0;	z = y[3];	x[3] = 0;	Fig. 3 $-$ C code of the Levinson algorithm.	11001	26 41B8696AD600000	11001	26 41932C0D440	00 ×[26	1 = BF9	E68FBI	E15D3C04	11001		D82CA51A5E3 8FBE15D3BE5	11001	25 BFA 26 BF98
	a[3] += a[0] * xi;	z = r[3] * x[0];		rig. 5 – C code of the Levinson argorithm.	TIOTI	27 C1A68E61F0000000	11011	27 C1A68E61F00					11011	27 3FAB1	FA41D56540D	11011	27 3FA
	a[2] += a[1] * xi;	z = r[2] * x[1];			11100 11101	28 C1B56A867F000000 29 41B0F77527000000	11100	28 C1B56A867F0 29 41B0F775270				BA76DFA1 BA638B4B	11100		703BA76DF5C 01D8A638B4C	11100	28 3F90 29 BFA
		z = r[1] * x[2];			11110	30 41B0E8D2E7000000	11110	30 41B0E8D2E70	» ×[30	I = BF2	D9E9B8	3548D7CB	11110		E9B8548D05C	11110	30 BF3
xi /= e;	[a[1]] = a[2] = a1	pm = z/e;	x[3] += a[0] * pm;	Z Z Z Z Delay Line	ne 11111	31 C1B5754418000000	11111	31 C1B57544180	» XI31	1 = 3FA	D47CE:	3F1FC98A	11111	31 3FAD4	7CE3F1FC99F	11111	31 3FA
	a[4] = 0;		x[4] = 0;				4 1 40	1 • 4 •	•••••	1.0.1			•	1.4.1.		. 1 11	1
	a[4] = 0; a[4] += a[0] * xi;	z = y[4];				- Comparison of 64											
		z = r[4] * x[0];		$c_0 - (X) c_1 - (X) c_2 - (X) c_3 - (X) \leftarrow Coefficien$		64-bit (4th column)											isible. F
	a[3] += a[1] * xi;	z = r[3] * x[1];		Multipliers	the rela	tive accuracy is on	a level c	of 10^{-13} . The ac	ccuracy for	48-bit cal	culation	s dramatica	ally drops	s down to	o a level of	$f 10^{-4}$.	
	a[2] += a[2] * xi;	z = r[2] * x[2];															
	a[1] += a[3] * xi;		x[3] += a[1] * pm;	Adder Tree	ee	0 ps		81.92 us	163.84 us		245.76 us		327.68 us		409.6 us	49	91.52 us
xi /= e;		pm = z/e;		yout		12.0 us											
etc				*		Ext_start				17 V 10 V 10	<u>v</u> 20 √	<u>01 V 00 V 00</u>	2 1 24	25 V 26		ne √ 20	V 20 V
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Fig. 4 – Four	r first steps in the Levin	nson algorithm impler	mentation	Fig. 5 – The structure of the FIR filter.		main_cnt:\$00003 B_next											
						main_cnt:\$00003 C_next main_cnt:\$00003 D_next											
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la 400000			Ja 400000		rig. 10	– Quartus [®] simula										· · · · · · · · · · · · · · · · · · ·	
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double *x, double *a, unsigned int dim) unsigned int n, i; e,z,xi,temp; initialization step // e = r[0];a[0] = 1; x[0] = y[0]/e;// main loop // for $(n = 1; n < \dim; ++n)$ // calculate xi // xi = 0;for (i = 0; i < n; ++i)</pre> { // loop A // $xi \rightarrow r[n-i] \ast a[i];$ $x_i = x_i/e;$ // update a // a[n] = 0;for (i = 0; i <= (n-1)/2; ++i)</pre>

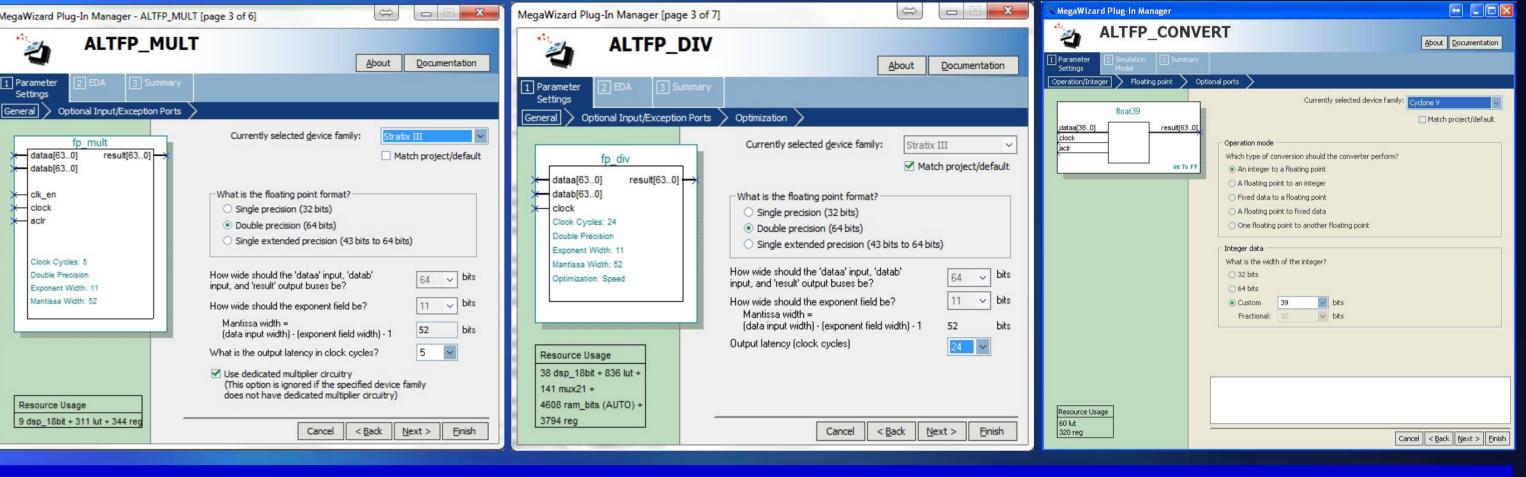
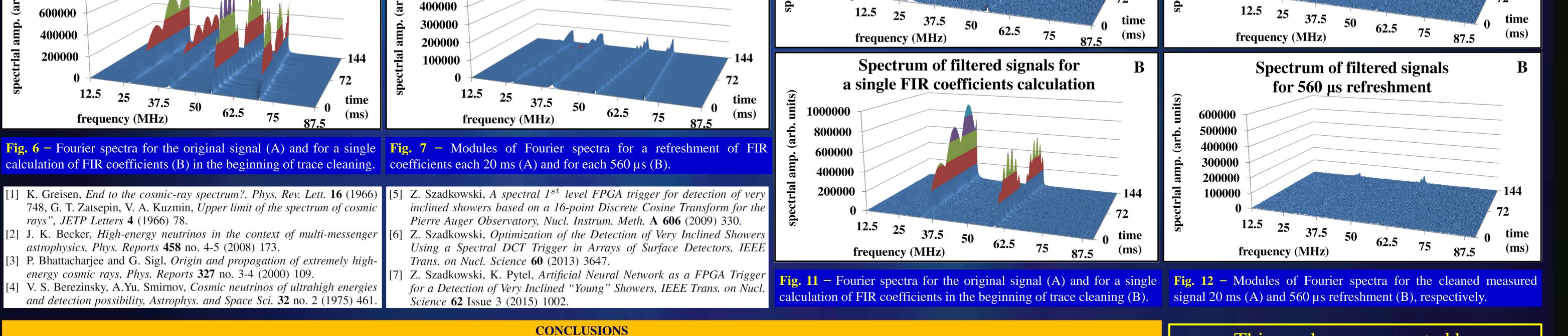


Fig. 8 – Altera® mega-functions multiplying, dividing and converting floating-point 64-bit variables.

		$\left(/ / 1_{000} P / / \right)$									
	۹(370] C Rsum[370]	$\frac{1}{1000 B} / \frac{1}{1000} = a[i];$	A4A0 A	Addr Data	A4A0 Addr Da	ta VIAI = B	FA 6F07586C27DE	A4A0 Add	r Data	A4A0 Addr	Data
		a[i] = temp + a[n-i] * xi;		41C9B90FA1000000			FA 57F9E6A740A4		BFA6F07586C27DEC		BFA6DBDF1763
mult:\$00000 sum38:\$00002		a[n-i] = a[n-i] + temp * xi;	00004	C18B1E4650000000	00001 1 C18B1E46		FA 12F38D2EFEF1		3FA57F9E6A740A50		3FA5A2633C72
		a[n-1] = a[n-1] + cemp = x1,	00010 2	C1B8D29003000000	00010 2 C1B8D29		FA A193AC848139		3FA12F38D2EFEF1A		3FA114C1A420
		$\cdots \cdots if (n \cdot div \cdot 2) == 0$	00011 3	41A3F75D56000000	00011 3 41A3F750		F9 4656A3BE5488		BFAA193AC84813A8		BFAA3231EB6E
Ciken clock dataa[130] dataa[130] datab[130] datab[130] datab[130]		$\prod_{i=1}^{n} (\prod_{i=1}^{n} (\prod_{i=1}^{n} (\sum_{i=1}^{n} (\sum_{i=1}^{n} (\prod_{i=1}^{n} (\sum_{i=1}^{n} (\sum_{i=1}^{n} (\prod_{i=1}^{n} (\sum_{i=1}^{n} (\sum_{i=1}^{n} (\sum_{i=1}^{n} (\prod_{i=1}^{n} (\sum_{i=1}^{n} (\sum_{i=1}^{n} (\prod_{i=1}^{n} (\sum_{i=1}^{n} (\sum_{$	00100 4	41B62BB675000000	00100 4 41B62BB		FA CD412690B773:		BF94656A3BE5487B		BF942AFF5924
		a[i] = a[i] + a[n-i] * xi;	00101 5	C1AFBE876C000000	00101 5 C1AFBE8	$\frac{76C00}{x[6]} = 3$	F7 3DB44E3564BC		3FACD412690B773D	00101 5 3	3FACE3B91FC7
			00110 6	C1B1F47130000000	00110 6 C1B1F47	$13000 \times [7] = B$	FA D7E5DCDA7CC3		3F73DB44E3564BBA	00110 6 3	3F72F1F900E9
		// calculate e //	00111 7	41B4A42C99000000	00111 7 41B4A42		F8 5A695C7E3165'	00111 7	BFAD7E5DCDA7CC45		BFAD85ACBC40
		(1 - xi + xi);	01000 8	41A8F1BB14000000	01000 8 41A8F1B		FA COB680B07FE6:	01000 8	3F85A695C7E31640		3F8610AB1112
Fig. 2 – A structure of 32 fast logic blocks calculating covariances (a	courin Fig. 1 All data are	// calculate 1 //	01001 9	C1B7F44206000000	01001 9 C1B7F442	ALLOI - D.	F9 9D6F1546EF951		3FAC0B680B07FE51		3FAC0C57D25A
	ccu in Fig. 1. An uata are	z = y[n];	01010 1	0 C1987006E4000000 1 41B993B0A7000000	01010 10 C1987006 01011 11 41B993B0	XLLLI - D.	FA 895F3ACB7CC6		BF99D6F1546EF95B		BF9A034EDADE
the fixed-point representation.		for $(i = 0; i < n; ++i)$	01100 1	2 C165E69A2000000	01100 12 C165E694	$\mathbf{X} \mathbf{L} \mathbf{I} \mathbf{Z} \mathbf{J} = \mathbf{J}$	FA 3806BF55DACO		BFA895F3ACB7CC6F		BFA89319F72B 3FA391F8054B
			01101 1	3 C1B96528E4000000	01101 13 C1B96528	XLIJI = J	FA 35D93444F277		3FA3806BF55DAC03 3FA35D93444F276E		3FA359146CA4
	Leep D	$z \rightarrow z = r[n-i] \times x[i];$	01110 1	4 419DB827E0000000	01110 14 419DB82	XLI4J = B	FA 8AF712844029		BFA8AF7128440292		BFA8BCD1888F
Loop A Loop B Loop C	Loop D		01111 1	5 41B76BF048000000	01111 15 41B76BF0	XLI5I = B	F9 983FF4D05F38		BF9983FF4D05F369		BF997B67F9C3
xi = 0; $a[1] = 0;$ $z = y[1];$	x[1] = 0;	// update x //	10000 1	6 C1AB4D57E8000000	10000 16 C1AB4D5		FA C197FE3E98D6'		3FAC197FE3E98D5F		3FAC241284F8
n=1 xi $-=$ r[1] * a[0]; a[1] $+=$ a[0] * xi; z $-=$ r[1] * x[0]		x + y + y + y + x [n] = x 0;	10001 1	7 C1B3CBAEF4000000	10001 17 C1B3CBA		F8 4F268C9FFF32		3F84F268C9FFF333		3F84E6219809
		••••••• for (i = 0; i <= n; ++i)	10010 1	8 41B2E8BDDA000000	10010 18 41B2E8B		FA D8046074CCE1		BFAD8046074CCE1A	10010 18 B	BFAD892ACE87
xi /= e; pm = z/e;	x[1] += a[0] * pm;	• • • • • • • • • • • • { • // • loop • D • //	10011 1	9 41AD8BC7A8000000	10011 19 41AD8BC	- FOOT	F7 54758B4FFEA3(FA CCA260599766)	1 1 1 1 1 1 1 1	3F754758B4FFE9FA	10011 19 3	3F754FA1BD7E
xi = 0; $a[2] = 0;$ $z = y[2];$	x[2] = 0;	x[i] += a[n-i] * z/e;	10100 2	0 C1B6D549B000000	10100 20 C1B6D54	00000	F9 4BBB29C08D25		3FACCA2605997662	10100 20 3	3FACD331C8BD
n=2 xi $-=$ r[2] * a[0]; a[2] $+=$ a[0] * xi; z $-=$ r[2] * x[0]		· · · · · · · · · · · · · · · · · · ·	10101 2	1 C1A16A85D6000000	10101 21 C1A16A8	FOOT D	FA A03BAD04D720		BF94BBB29C08D23E	10101 21 B	BF94B8FF8316
		· · · · · · · · }	10110 2	2 41B9256DD6000000	10110 22 41B9256E	FOOT O	FA 15495DC86954		BFAA03BAD04D721C		BFAA0EEF105C
xi -= r[1] * a[1]; a[1] += a[1] * xi; z -= r[1] * x[1]]; x[1] += a[1] * pm;	return;	10111 2	3 41803AC34000000	10111 23 41803AC		FA 5600703DE1B5		3FA15495DC86952D		3FA151F1B57D
xi /= e; $pm = z/e;$	x[2] += a[0] * pm;	· · · · }	11000 24	4 C1B9AF60D1000000 5 41932CDD44000000	11000 24 C1B9AF6 11001 25 41932CD		FA 70D82CA51A5F	24	3FA5600703DE1B6A		3FA56EA8367F
			11001 2	6 41B8696AD600000	11001 25 41932CD	FOCT D	DO TZOBBTICBOOG	11001 23	BFA70D82CA51A5E3		BFA70B4E5097
xi = 0; $a[3] = 0;$ $z = y[3];$	x[3] = 0;	Fig. 3 – C code of the Levinson algorithm.	11010 2		11010 20 41866567 11011 27 C1A68E6		F9 E68FBE15D3C0 FA B1FA41D56540		BF9E68FBE15D3BE5		BF9E8DF57638
xi -= r[3] * a[0]; a[3] += a[0] * xi; z -= r[3] * x[0]]; x[0] += a[3] * pm;		11100 2	8 C1B56A867F000000	11100 28 C1B56A8		F8 FC703BA76DFA:		3FAB1FA41D56540D		3FAB1FBC0ACE 3F9010A098A2
n=3 xi -= r[2] * a[1]; a[2] += a[1] * xi; z -= r[2] * x[1]			11101 2	9 41B0F77527000000	11101 29 41B0F775		FA D401D8A638B4	11100 20	3F8FC703BA76DF5C BFAD401D8A638B4C		BFAD44F3D8FF
			11110 3	0 41B0E8D2E7000000	11110 30 41B0E8D2		F2 D9E9B8548D7C	11101 20	BF2D9E9B8548D05C		BF3B83C098F7
xi = r[1] * a[2]; a[1] += a[2] * xi; z = r[1] * x[2]		Z ⁻¹ Z ⁻¹ Z ⁻¹ Z ⁻¹ Tapped Delay Line	11111 3	1 C1B5754418000000	11111 31 C1B57544		FA D47CE3F1FC98		3FAD47CE3F1FC99F		3FAD53DBFD56
xi /= e; $pm = z/e;$	x[3] += a[0] * pm;						فيقبقه والمتعادة والمتعادة والمتحد والمتحد		STAD47CEST 11 CSST		
xi = 0; $a[4] = 0; z = y[4];$	x[4] = 0;				1 40 1 4	· · · · · · · · · · · · · · · · · · ·		• • • • • • • • • • • • • • • • • • • •	(1)	• 1 11 1	1
		+ $+$ $+$		• • • • • • • • • • • • • • • • • • •		ovariances (two left					
xi = r[4] * a[0]; a[4] += a[0] * xi; z = r[4] * x[0]]; x[0] += a[4] * pm;	$c_{0} - (X) = c_{1} - (X) = c_{2} - (X) = c_{3} - (X) - Coefficient$	FPGA 6	4-bit (4th column)	and 48-bit (right c	olumn). Some discre	pancy on least signi	ficant bits for	64-bit calculation	ns are visible.	. However,
n=4 xi -= r[3] * a[1]; a[3] += a[1] * xi; z -= r[3] * x[1]]; x[1] += a[3] * pm;					e accuracy for 48-bit					, í
xi = r[2] * a[2]; a[2] + a[2] * xi; z = r[2] * x[2]			the relat	ive accuracy is on	a level of 10 ⁻² . The	e accuracy 101 46-011	calculations dramati	carry drops de	Dwil to a level of	10 .	
	1 · v [2] 1 – a [1] * mm ·										
xi = r[1] * a[3]; a[1] + a[3] * xi; z = r[1] * x[3]]; x[3] += a[1] * pm;			0 ps	81.92 us	163.84 us	245.76 us	327.68 us	409,6 us	491.52 us	565.0 us
], x [5] +- a[1] " pm,	Adder Tree		0 ps 12.0 us	81.92 us	163.84 us	245.76 us	327.68 us	409.6 us	491.52 us	565.0 us +537.315 us
xi /= e; pm = z/e;], x [5] +- a[1] [~] pm,	Adder Tree		0 ps 12.0 us	81.92 us	163.84 us	245.76 us	327.68 us	409,6 us	491.52 us	
], x [5] +- a[1] ⁻ pm,	yout Adder Tree		0 ps 12.0 us Ext_start	81.92 us	163.84 us	245.76 us	327.68 us	409.6 us	491.52 us	
xi /= e; pm = z/e;		yout Adder Tree		sel_cnt 0 2 3	81.92 us	163.84 us	245.76 us	327.68 us	409,6 us	491.52 us	
xi /= e; pm = z/e; etc		yout		sel_cnt 0 (2/3) main_cnt:\$00003 A_next	81.92 us	163.84 us	245.76 us	327.68 us	409,6 us	491.52 us	
xi /= e; pm = z/e;		Adder Tree yout Adder Tree Fig. 5 – The structure of the FIR filter.		sel_cnt 0 (2/3) main_cnt:\$00003 A_next main_cnt:\$00003 B_next	81.92 us	163.84 us	245.76 us	327.68 us	409,6 us	491.52 us	
xi /= e; pm = z/e; etc		yout		sel_cnt 0 (2/3) main_cnt:\$00003 A_next	81.92 us	163.84 us	245.76 us	327.68 us	409,6 us	491.52 us	
xi /= e; pm = z/e; etc Fig. 4 – Four first steps in the Levinson algorithm impletered in the steps in the	lementation	Fig. 5 – The structure of the FIR filter.	;00256 cntr_l4h:auto	sel_cnt 0 2/3/ main_cnt:\$00003 A_next main_cnt:\$00003 B_next main_cnt:\$00003 C_next	81.92 us	163.84 us	245.76 us	327.68 us	409,6 us	491.52 us	
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The hardware Levinson procedure implemented into FPGA fabric significantly shortens the refreshment time in the linear predictor approach used for RFI suppression. With Cyclone[®] IV (FPGA used at present in the Dutch AERA digitizers) and in Cyclone[®] V E (considered as FPGA for the future upgrade) the refreshment time is on a level of 560 µs (with 100 MHz clock for covariances calculation and the Levinson recursion). The 200 MHz speed has been achieved in the Stratix [®] III FPGAs (speed grade - 2) and allowed a reduction of refreshment time to 275 µs, however, the Stratix[®] series are too power consuming and too expensive. We plan to use the above algorithm for tests of RFI suppression: a) in Łódź environment using the standard AERA antenna and b) in real radio stations on Argentinean pampas.

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