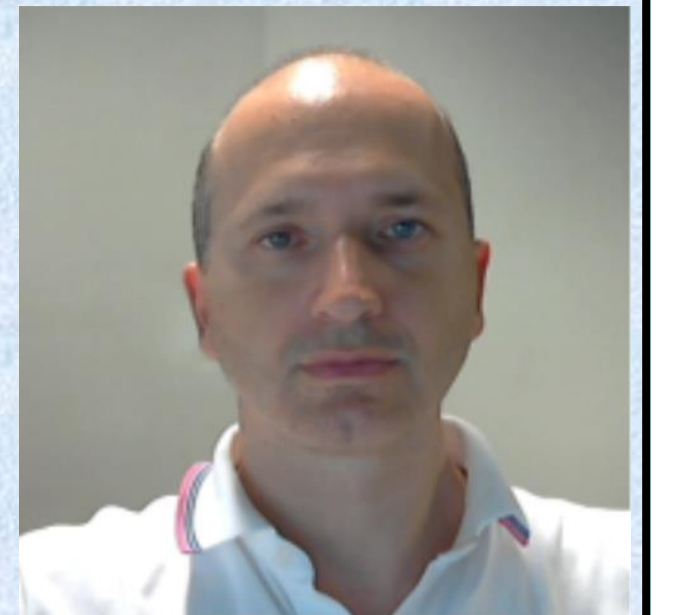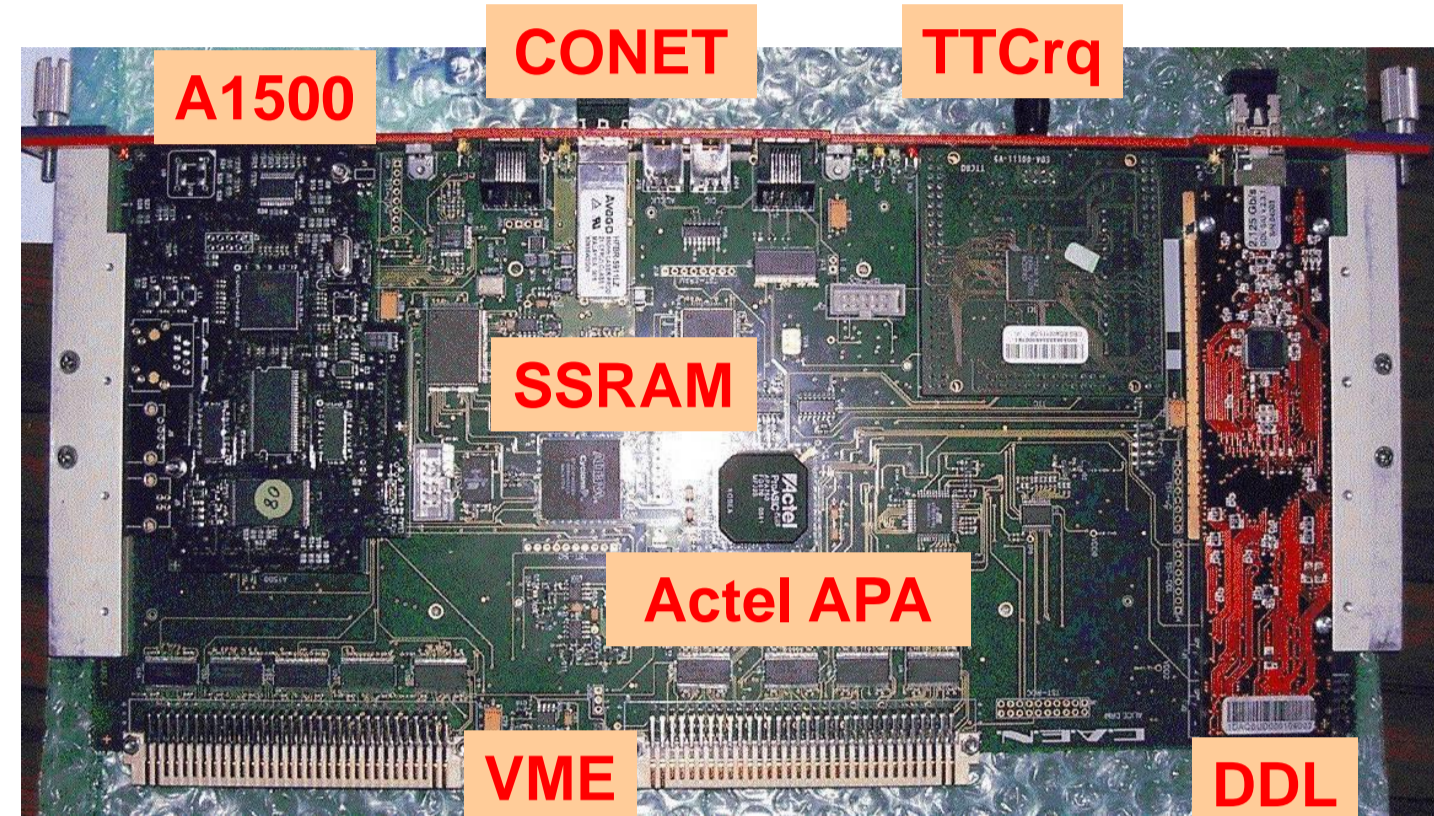# Design and test of a GBTx based board for the upgrade of the ALICE TOF readout electronics
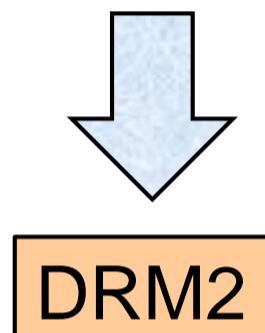
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This poster shows the results achieved with a test board that has been designed as a first step towards the upgrade of the ALICE TOF readout electronics foreseen in 2019-2020 at CERN. The board features a radiation hard SERDES ASIC from CERN, named GBTx, which, in connection to the rad-hard optical transceiver VTRx, implements the newer generation optical links for many detector readout systems at LHC. The heart of the board is a commercial FPGA from Microsemi, an Igloo2 device, which is expected to cope with the moderately hostile radiation environment, as a total dose of 0.13 krads is expected in 10 years of data taking. The board has been extensively tested with a special attention devoted to the Igloo2-GBTx devices: a measurement of the optical link BER is presented, together with the test results obtained connecting the board to a PC using the standard ALICE DAQ board (C-RORC).

DRM1 used in RUN1-RUN2

GBTX test board

DRM2   for RUN3 - …

Board description

The GBTx test board was born as a feasibility study to show how the GBTx ASIC can be used as an interface towards the DAQ and the trigger system, thus replacing the DDL and the TTCrq mezzanines which were used on the **DRM1**, the Digital Readout Module for the TOF detector at CERN. The idea is to study the main building blocks towards the **DRM2** design, which has already started.

In connection to the optical transceiver VTRx, the GBTx allows the implementation of a 4.8 Gbps bi-directional optical link between the detector zone and the off-detector electronics zone. We are actually using just **3.2 Gbps** out of the total bandwidth, since the remaining bits are used for data integrity check and correction. In our case the board shall sit at ~4m from the beam pipe and for this reason it will be exposed to an expected integrated radiation dose of 0.13 krads in 10 years and a flux of 0.26 kHz/cm^2 of hadrons with energy greater than 20 MeV, relevant for Single Event Upset (SEU) effects. The GBTx and VTRx are designed to be working in a much harsher radiation environment (they can cope with the Mrad dose range). The board also needs an intelligent device providing the configuration to all the interfaces and sending data / receiving triggers: we chose a Microsemi Igloo2 for the purpose. Being Flash memory based, it is inherently immune to upsets in the configuration memory. For protecting the logic and the flip-flops, we are going to implement a Triple Modular Redundancy to minimize the effects of SEUs. Igloo2 devices have already been qualified for working in environments with a few krads total dose without major problems.

The test board also hosts an ARM processor on a mezzanine, which is already being used on the DRM1 board. Its purpose is to remotely re-program via an Ethernet link the Igloo2 FPGA when a new firmware revision is produced. However, the main slow control functions are implemented via an optical link that uses the CAEN proprietary protocol CONET2. From the hardware point of view, this is realized with a commercial SFP+ transceiver connected to the Igloo2 internal SERDES.

Board components

The main components of the GBTx test board are:

- Microsemi Igloo2 FPGA (**M2GL090T-FG676 device**)
- CERN **GBTx** ASIC (4.8 Gbps SERDES)
- CERN optical transceiver **VTRx** (4.8 Gbps)
- Commercial SFP+ device connected to the Igloo2 internal SERDES
- A1500 (ARM processor board) mezzanine
- Cypress SSRAM (CY7C1350DG) for data buffering
- Xilinx CPLD for power supply and JTAG control
- Power supply (both switching and linear regulators)
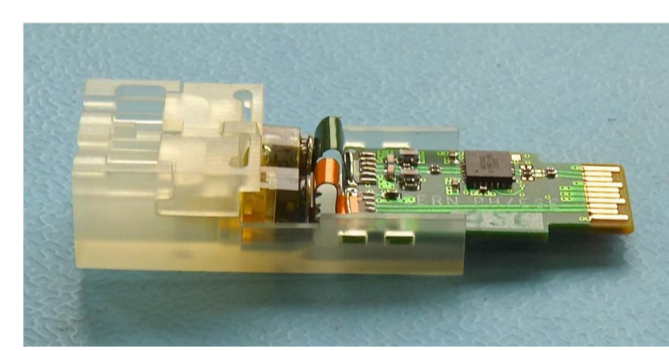

GBTx   VTRx

Board configuration and control

The board components can be controlled in either of 3 ways:

- **NI8451**:
  This USB NI controller drives an I2C port used to access the 365 GBTx internal registers and the board power regulators (voltage-current), via custom I2C slave + I2C master firmware blocks on the FPGA. A custom Virtual Instrument has been designed to control these parameters via a 3-wire cable.

NI8451
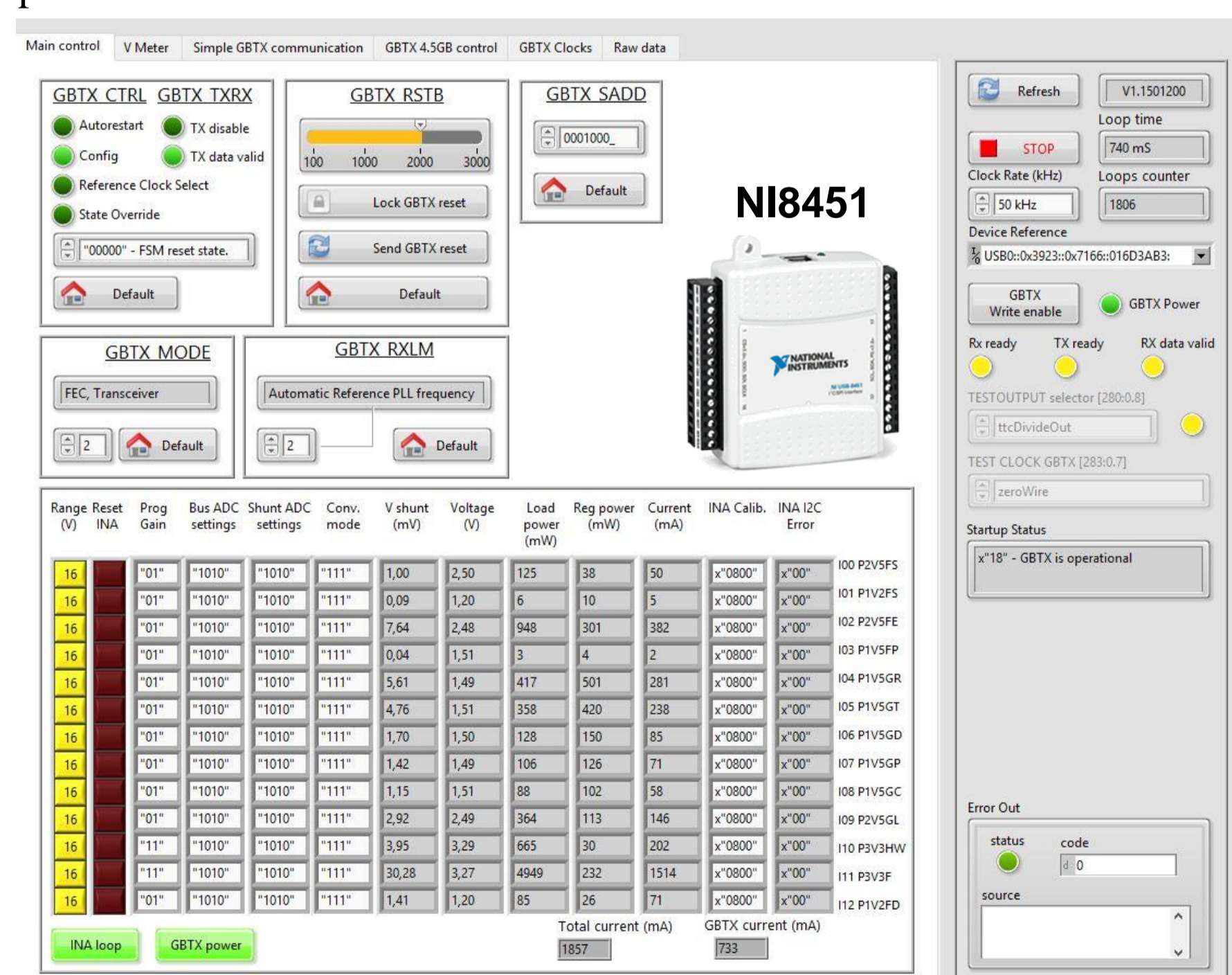
- **A1500**:
  The ARM processor on the mezzanine controls the FPGA via a 16-bit data bus and a 8-bit address bus. The main usage of this link is to re-program the FPGA, but it can also be used to access the FPGA-GBTx internal buffers and registers.
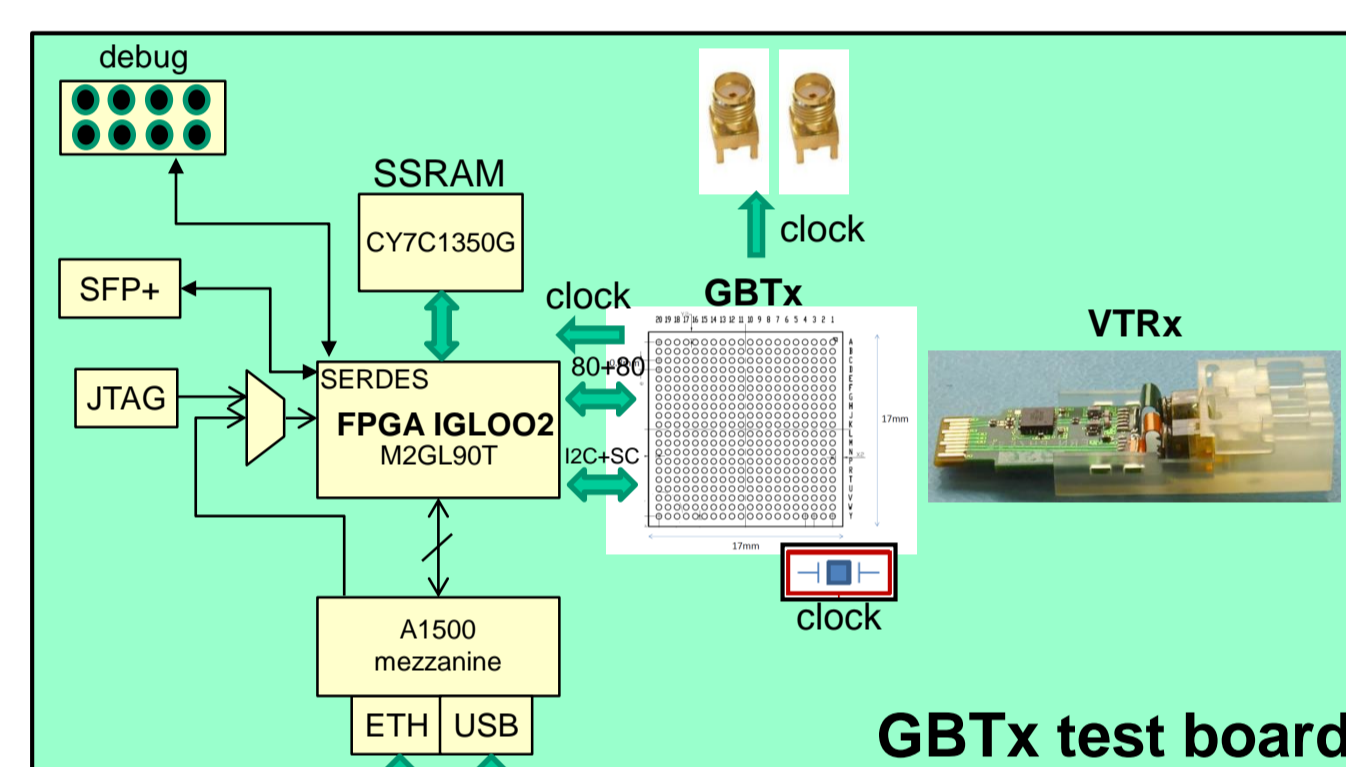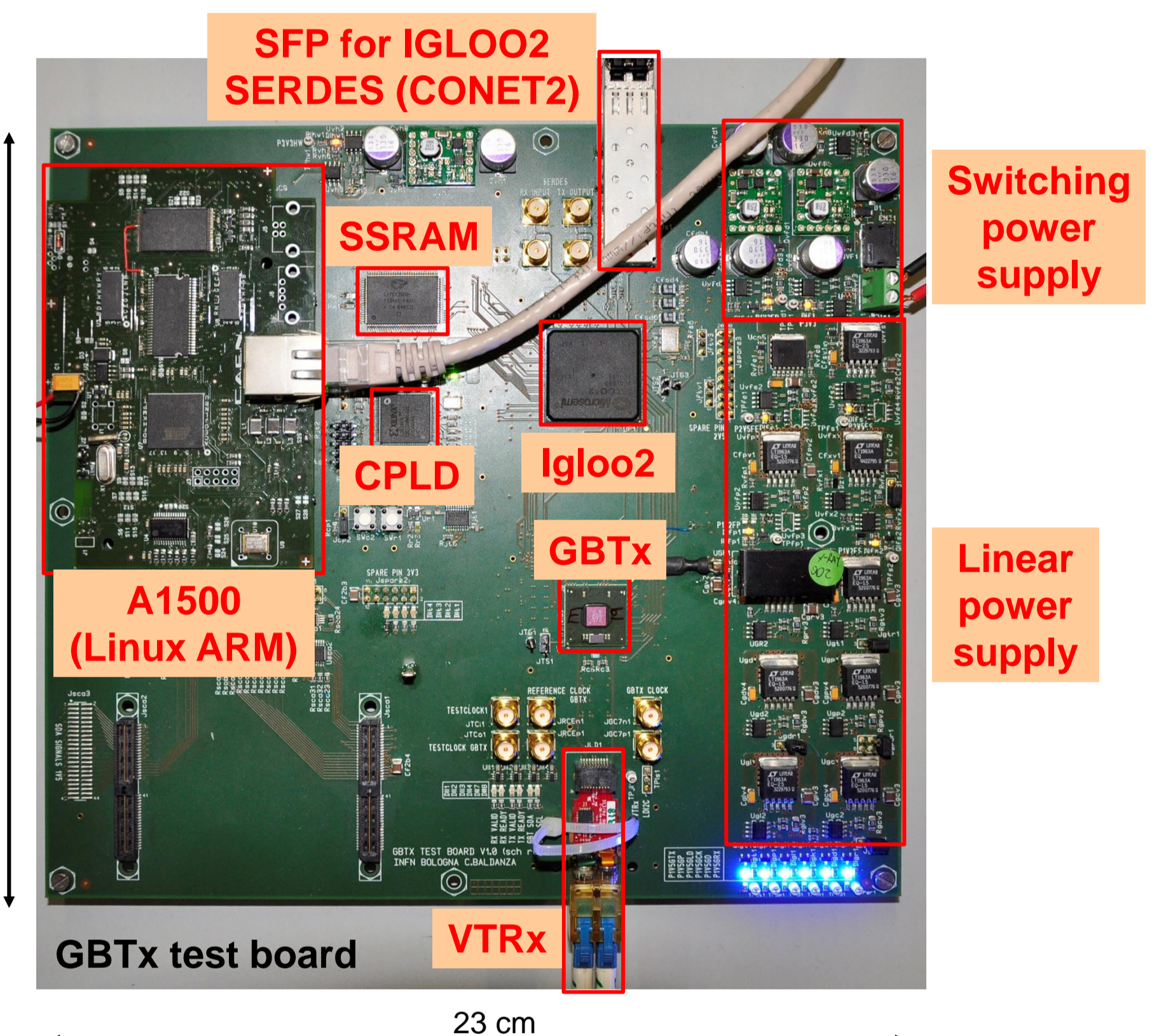- **CONET2**:
  This is a proprietary 1.25 Gbps serial link from CAEN used as a slow control link for spying temperatures, voltages, vital parameters of the board and for monitoring physics data. It can also be used to access all the FPGA buffers and, in the real experiment, it is used to upload the configuration to all the readout electronics, such as the TDC cards.

GBTx test board


ALICE C-RORC

Igloo2 – GBTx interface: E-Links

We implemented a direct connection between the Igloo2 and the GBTx without any termination (the internal termination is activated on-chip on both receiving ends). The PCB tracks have been designed avoiding vias and minimizing length skews.

GBTx register #234 was used to test the E-Links: it allows to send back to the Igloo2 the same pattern as it has been received, implementing a sort of **parallel loopback**. This feature allowed us to fully characterize the proper behavior of the 3.2 Gbps parallel link using a pseudo-random pattern generator on the FPGA and then checking the received data.

BER measurements

The 4.8 Gbps optical link has been tested using an optical loopback. The GBTx register #28 allows to send known patterns on the serial output and to compare the incoming serial line with the expected values. A pair of 8-bit counters stores the 16-bit error counter value, which can be used to measure the optical link Bit Error Rate (BER). With this method we were able to measure a **BER lower than 10^{-14}** using an 80m-long multi-mode optical fiber, by running the system for 30 hours without errors.
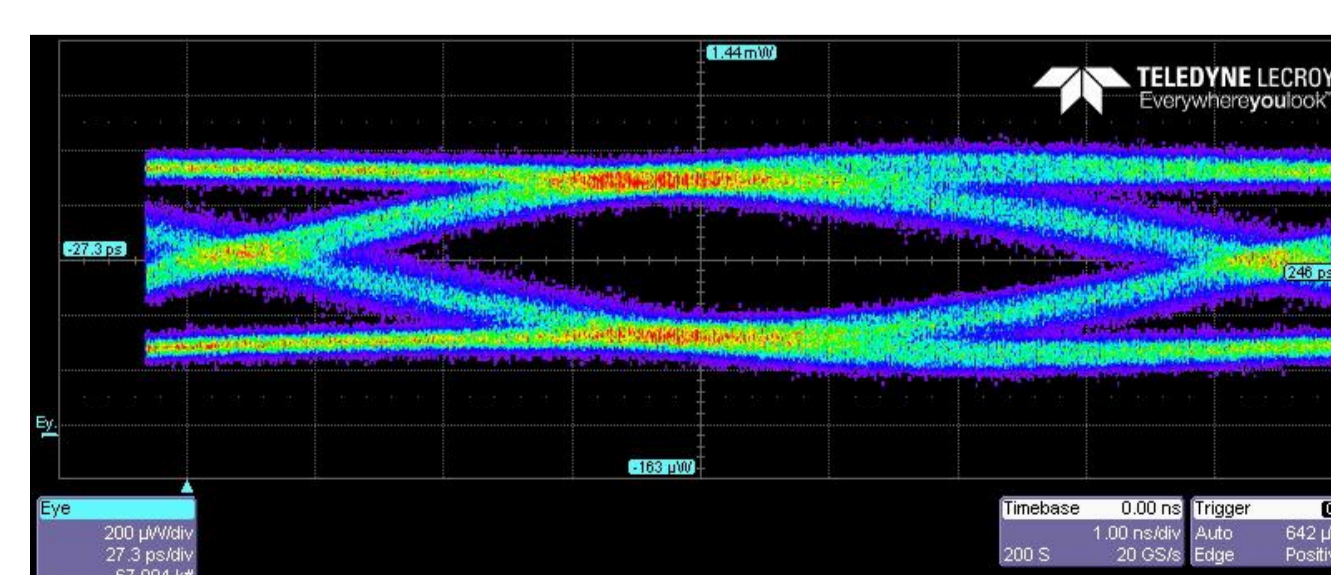
Using a 20 GS/s serial data analyzer featuring an optical input, we acquired the eye diagram of the serial line as reported in the above picture. The shape of the eye is compatible with the already measured BER.

GBTx test board – C-RORC connection tests

We tested the data transfer between the GBTx test board and the C-RORC, the standard ALICE PCIe data acquisition board, with firmware adapted to use GBTx protocol. The bidirectional communication was tested:

- triggers (and trigger info: bunch counter and orbit number) sent from the C-RORC to the GBTx test board at fixed bunch crossing values (9 equally spaced in time during an orbit),
- event data sent from the GBTx test board upon trigger reception to the C-RORC, including the bunch number, the orbit number and a data counter payload of 100 words.

Using this configuration we operated 2 GBTx test boards connected to 1 C-RORC with the following performances:

- **200 kHz trigger rate,**
- **270 MB/s throughput**

When the PC asserts the flow control (for instance when dumping data on disk), the event rate drops down to 5 kHz without getting stuck and without introducing any data corruption.

The ALICE DATE software performs checks on the bunch + orbit number received and on the size of the events. No evidence of data corruption has been observed on both link directions after many hours of operation.
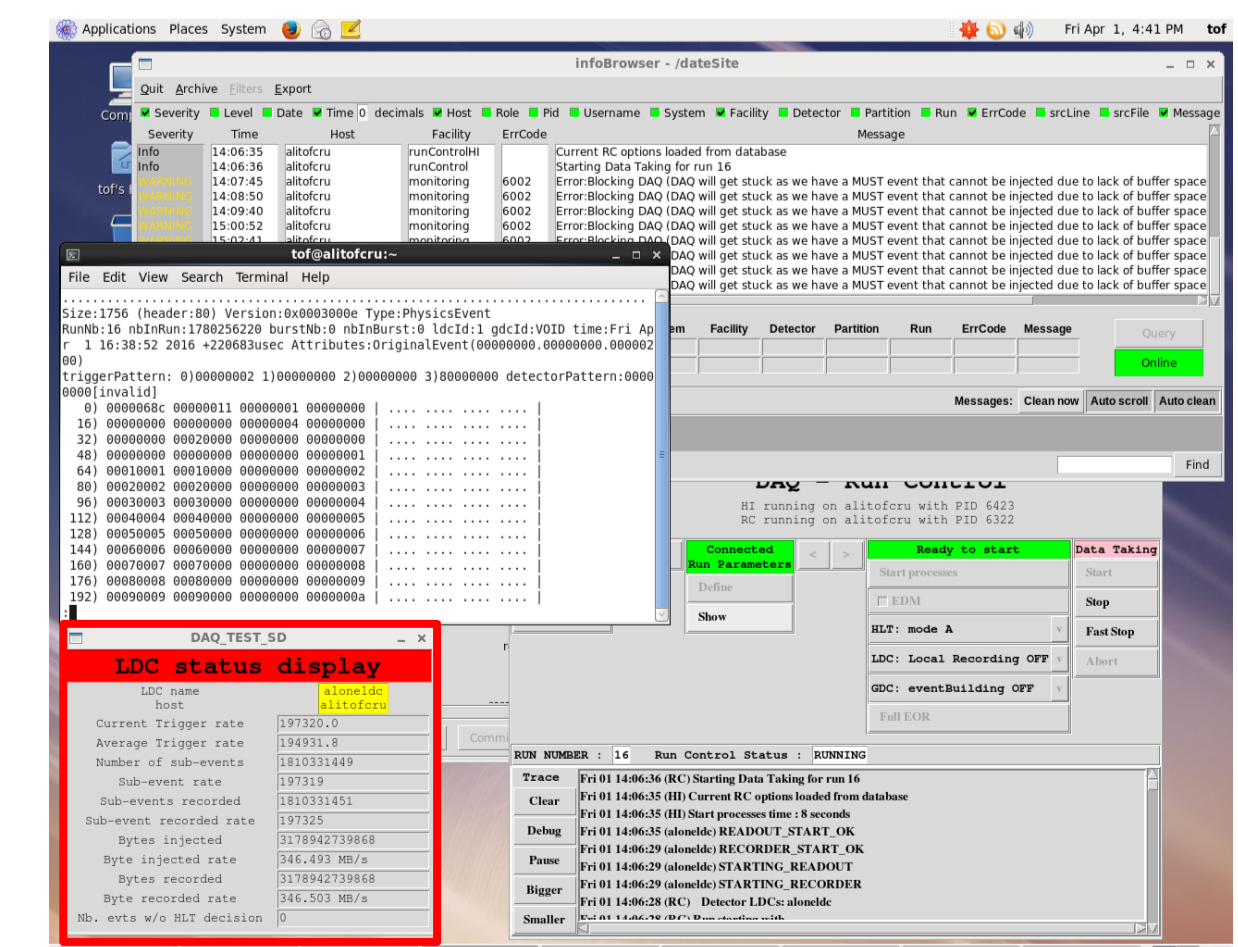
Conclusion

The GBTx test board allowed us to thoroughly test the GBTx-VTRx optical link features, together with the Microsemi Igloo2 device, letting us finalize the choices on how the DRM2 will look like. The board also allowed us to develop and test part of the firmware that will also be commissioned for the DRM2 board. Furthermore, the same board will also be used to qualify, in a radiation environment, the electronic components for the final DRM2 board.