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Engineering Array Tests of High-Resolution Front End Electronics for Water Cherenkov Air Shower Detectors equipped with Cyclone V

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Seven Front-End Boards (FEBs) equipped in the biggest Cyclone V E FPGA 5CEFA9F31I7N,
supporting 8 channels sampled up to 250 MSps @ 14-bit resolution have been successfully installed in seven surface detectors on the Pierre Auger Engineering Array. Surface detectors use 6 channels with a sampling of 120 MHz.
Two rest channels with independent sampling were tested as the radio channels
with the sampling of 200 MHz. The FEBs have been developed without anti-aliasing filters to keep a maximal flexibility. A communication between surface detectors and the Central Data Acquisition Station (CDAS) has been established via standard radio link without any modification of a standard protocol. Any tuning of required processes typically being a task of the Unified Board (UB) has been moved to the FPGA algorithm.

The power consumption by the new FEBs is on a level of 18 W, but an average power
solar panel efficiency is ˜10 W. An external power control circuit with a hysteresis
cuts off/on the supply of the entire surface detector electronics to avoid a total battery discharging and its damage. Such an interrupted operation reduces significantly a statistics of registered events.
A second (or larger) solar panel would eliminate this inconvenience, however, we
would like to collect also experiences with a lack of energy in real pampas conditions.

We installed seven FEBs in the Pierre Auger Engineering Array in November 2015.
Data acquisition is going smoothly on the T1 trigger only. The ToT (Time over Threshold) trigger has not been implemented due to its instabilities. In March 2016 we plan to modify the FPGA code including parallel the DCT trigger keeping the same sigma-delta algorithm for a trigger stability rate as for previous Cyclone III FEB tested in 2011.

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