Tests of High-Resolution Front-End Electronics for Water-Cherenkov Air Shower Detectors equipped with Cyclone® V on the Pierre Auger Test Array

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ABSTRACT

Seven Front-End Boards (FEBs) equipped with the biggest Cyclone®V E FPGA 5CEFA9F31I7N, supporting 8 channels sampled up to 250 MSps @ 14-bit resolution have been successfully installed in seven surface detectors on the Pierre Auger Test Array. Surface detectors use six channels with a sampling of 120 MHz. Two remaining channels with independent sampling were tested as radio channels with the sampling of 200 MHz. The FEBs have been developed without anti-aliasing filters to keep a maximal flexibility. Communication between surface detectors and the Central Data Acquisition Station (CDAS) has been established via a standard radio link without any modification of a standard protocol. Any tuning of required processes, typically being a task of the Unified Board (UB), has been moved to the FPGA algorithm. The power consumption by the new FEBs is on a level of 18 W, but an average power solar panel output is ~10 W. An external power control circuit with a hysteresis cut off/on supplies the entire surface detector electronics to avoid a total battery discharging and its damage. Such an interrupted operation reduces significantly statistics of registered events.A second (or larger) solar panel would eliminate this inconvenience, however, we gather experiences with a lack of energy in real pampas conditions. We installed seven FEBs in the Pierre Auger Test Array in November 2015. Data acquisition is going smoothly on the T1 trigger only. The ToT (Time over Threshold) trigger has not been implemented due to instabilities.

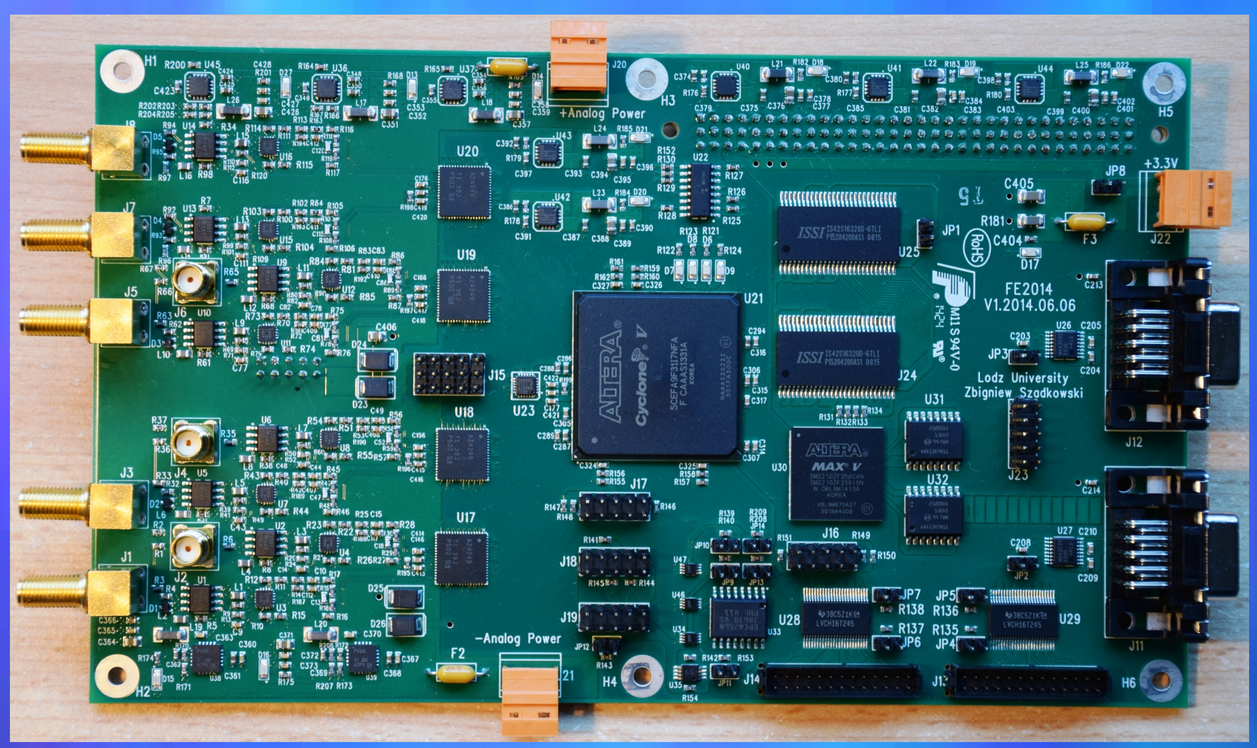


Fig. 1 – Front-End Board with Cyclone®V E FPGA and 4 double 14-bit ADCs (ADS4249 - Texas Instr.) with maximal 250 MSps sampling.

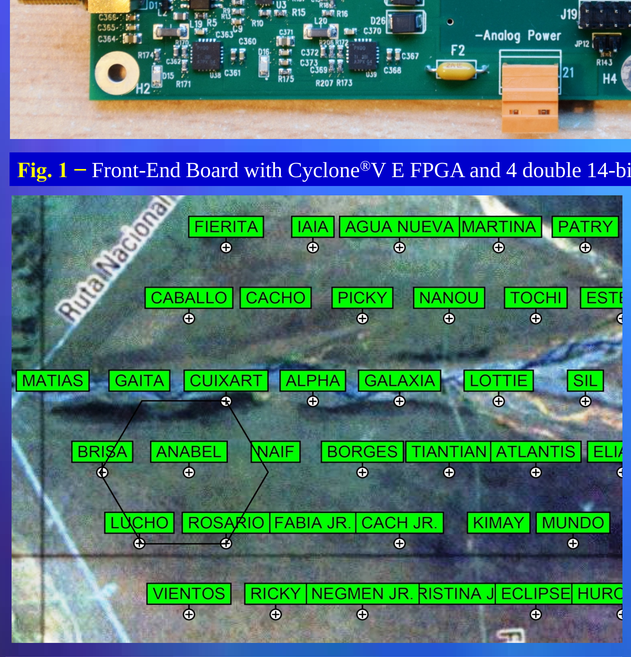


Fig. 3 – Location of the hexagon on the Pierre Auger Test Array

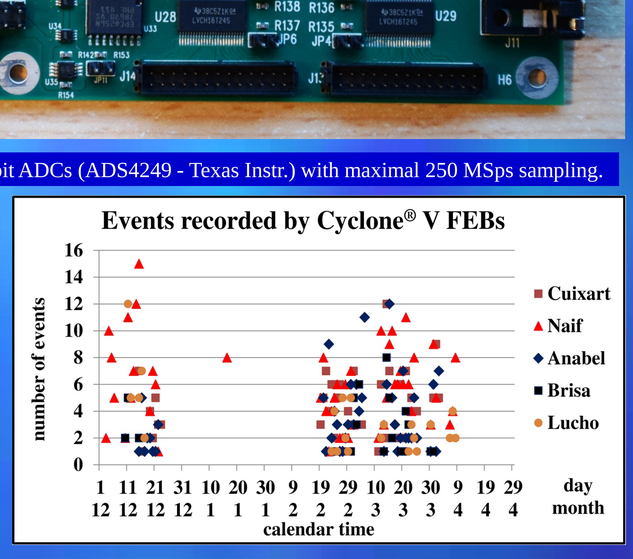
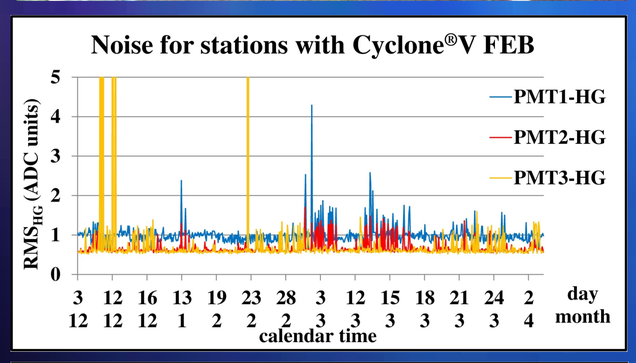
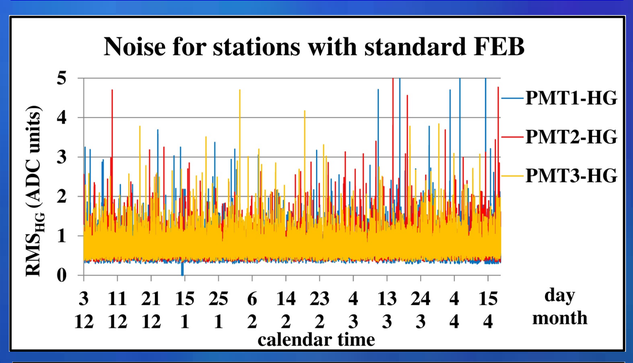
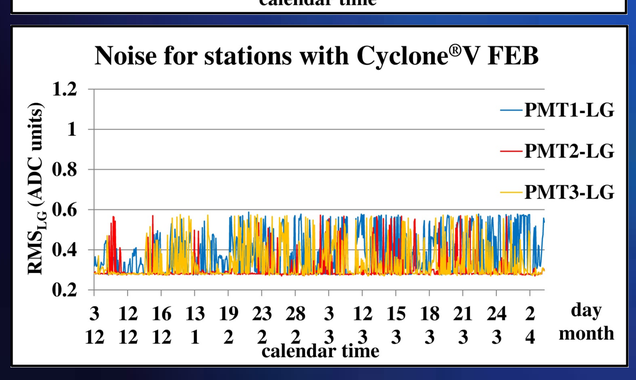


Fig. 2 – Events registered within December 2015 - April 2016







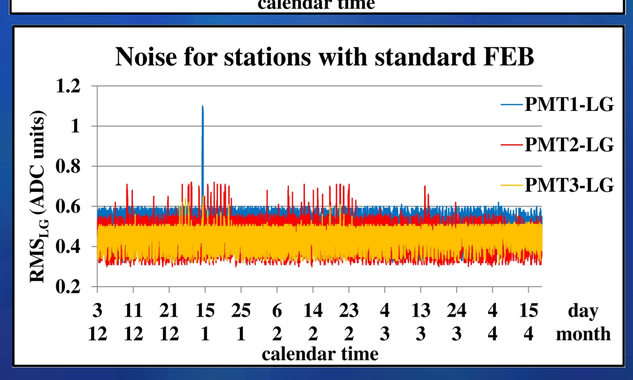


Fig. 4 – RMS for HG and LG channels for FEB equipped with Cyclone®V E FPGA. Data are presented without time gaps.

Fig. 5 – RMS for HG and LG channels for FEB equipped with standard Cyclone® FPGA.

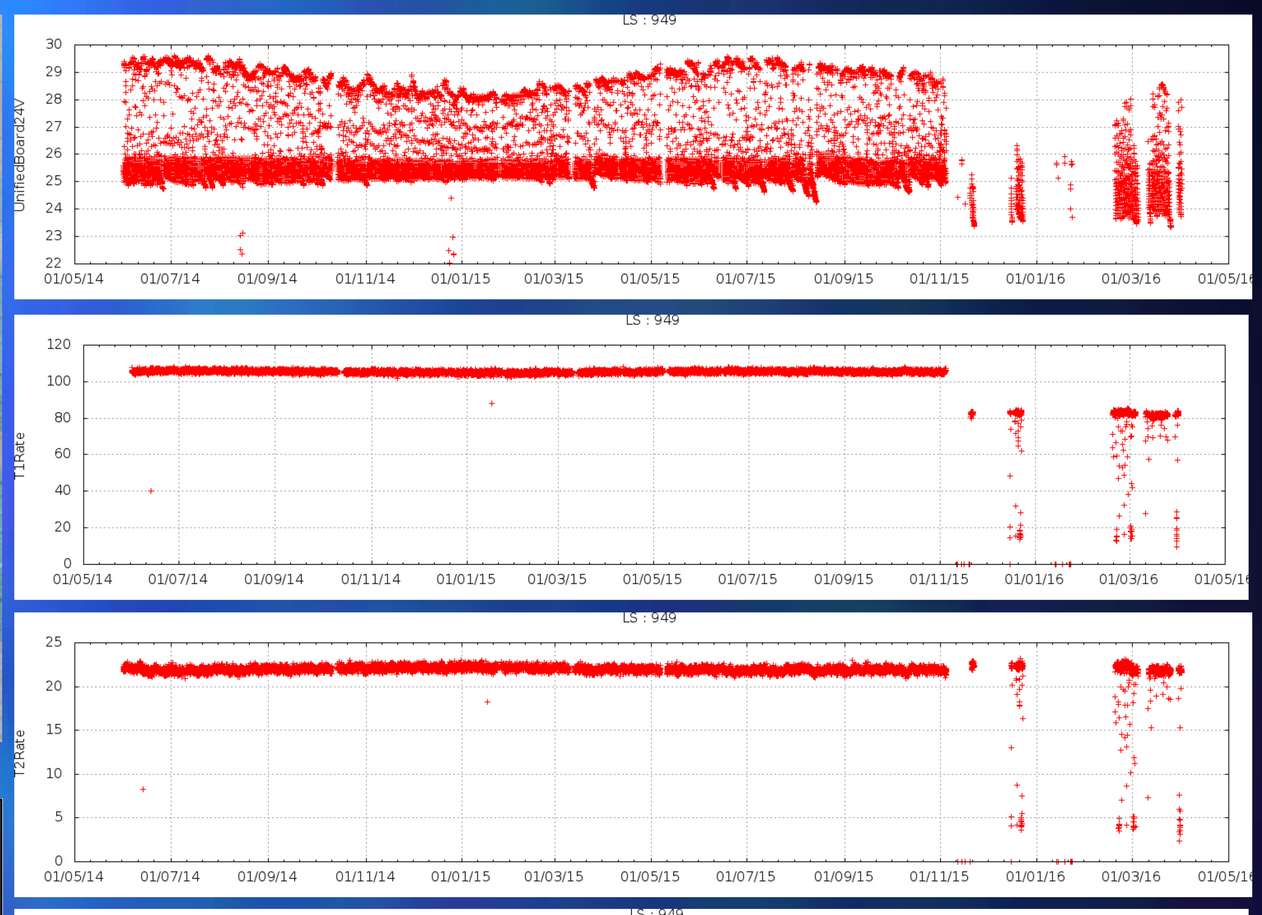


Fig. 6 – Monitoring data for Cuixart (949) surface detector. Graphs for other detectors in a hexagon equipped in Cyclone®V E Front-End Boards are similar. Gaps due to interrupted mode are clearly visible since Nov. 2015

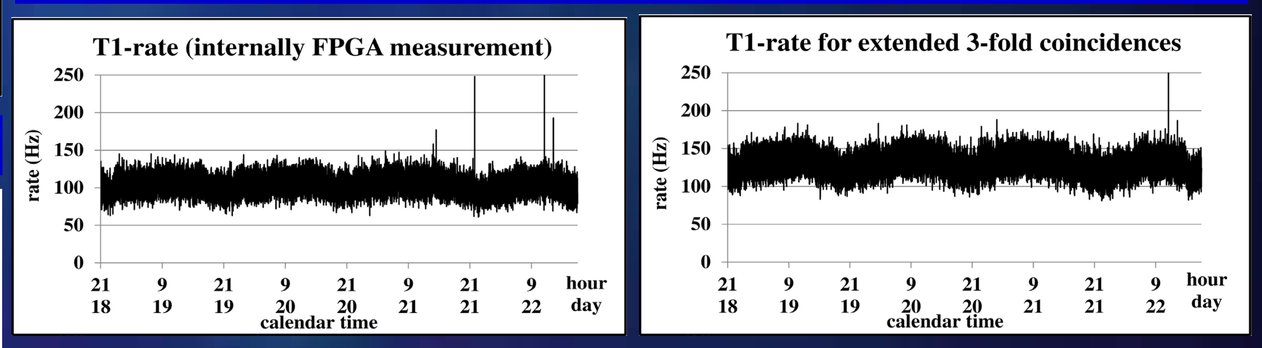


Fig. 7 – Standard and extended (3 fold coincidences in any 3 consecutive time bins) T1-rate measured in the FPGA in „Jamie" detector.

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[3] Z. Szadkowski, *Trigger Board for the Auger Surface Detector with 100 MHz Sampling and Discrete Cosine Transform, IEEE Trans. on Nucl. Science* **58** (2011) 1692.

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CONCLUSIONS

All FEBs delivered to Argentina successfully passed all tests in the field conditions. We tested standard protocols with higher sampling rates (120, 160, 200 and 240 MSps) and 12-bit resolution in a narrower window (6.4, 4.8, 3.84 and 3.2 μs instead of 19.2 μs due to higher sampling rate) and with standard and optimized thresholds. Cloudy days impaired a power budget and selected detectors had to be remotely switched off for the night to ensure that the battery did not discharge to a level menacing of a total damage. We had to add a remote temporary digital power disconnection (supplied from the same power line) to allow independent FPGA reprogramming from the standard configuration chip (a theoretically simultaneous turning on the power for UB and FEB practically generates a race hazard which sometimes leaves the FPGA not programmed). Two surface detectors could not provide a communication with the CDAS (Gaita) or could not provide ADC data (Rosario). Nevertheless, the new Front-End Boards with Cyclone®V E FPGA smoothly provided valuable data for 120 MHz sampling and fully confirmed their reliability in the field conditions.

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