A modular data acquisition system using the 10 GSa/sec PSEC4 waveform recording chip

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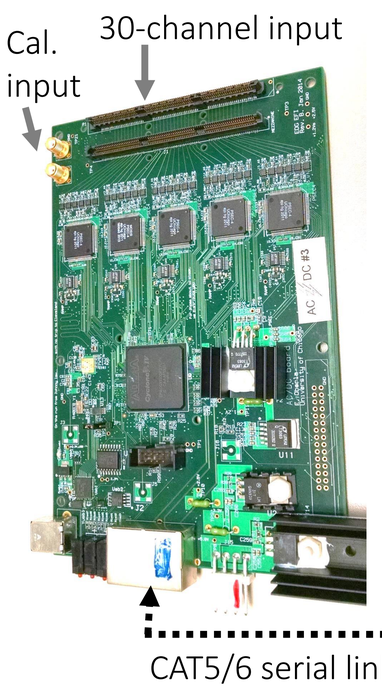
Abstract

A data acquisition system using the 10 Gigasample-per-second waveform-recording PSEC4 chip is described. The system architecture incorporates two levels of hardware, FPGA-embedded system control, and data processing. The front-end unit is a 30 channel circuit board that holds five PSEC4[1] ASICs, a clock jitter cleaner, and a control FPGA. The analog bandwidth of the front-end signal path is 1.5 GHz. Each channel has an on-chip threshold-level discriminator that is monitored in the FPGA, from which a flexible on-board trigger decision can be formed. To instrument larger channel counts, a `back-end' 6U VME32 central card was designed. This central card incorporates a single large FPGA that manages up to 8 front-end cards using one or two network (CAT5) cables per board, which transmits the clock and communicates data packets over a custom serial protocol. Data can be read off the board via USB, Ethernet, or dual SFP links in addition to the VME interface. To scale to larger systems, the central card architecture allows this board to serve also a `crate master' board, which receives data from up to 8 central cards (with each managing 8 front-end cards), allowing a single VME crate to control up to 1920 channels of the PSEC4 chip.

Hardware



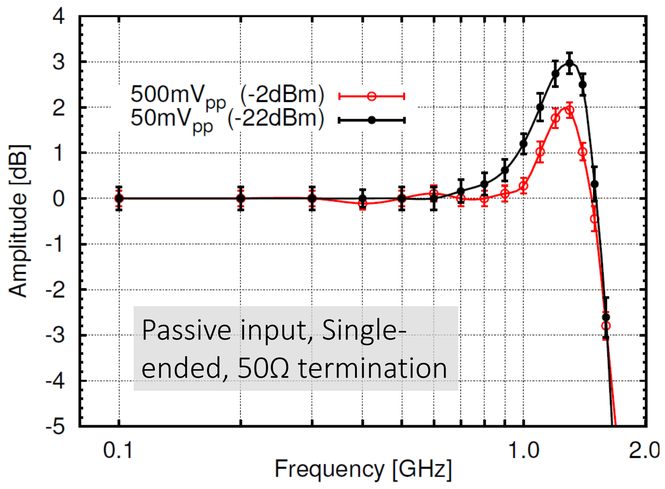
Left: **ACquisition and Digitization with pseC4 (ACDC) card**

Right: **ANNIE Central Card (ACC)** [2]

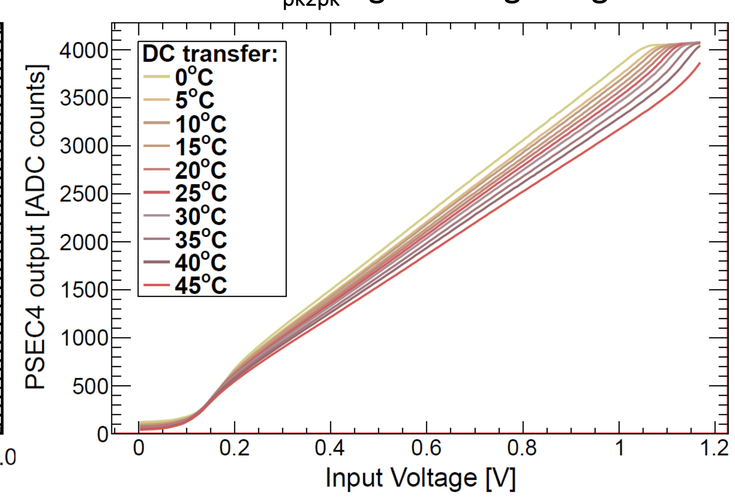
Each back-end ACC manages up to 8 front-end ACDC boards using two network cables per board. Data are transferred using SerDes with a custom protocol at a rate of up to 1.6 Gbps. A single differential pair on the link is dedicated to the system clock, which is sent to a jitter-cleaning chip on ACDC cards.

Performance

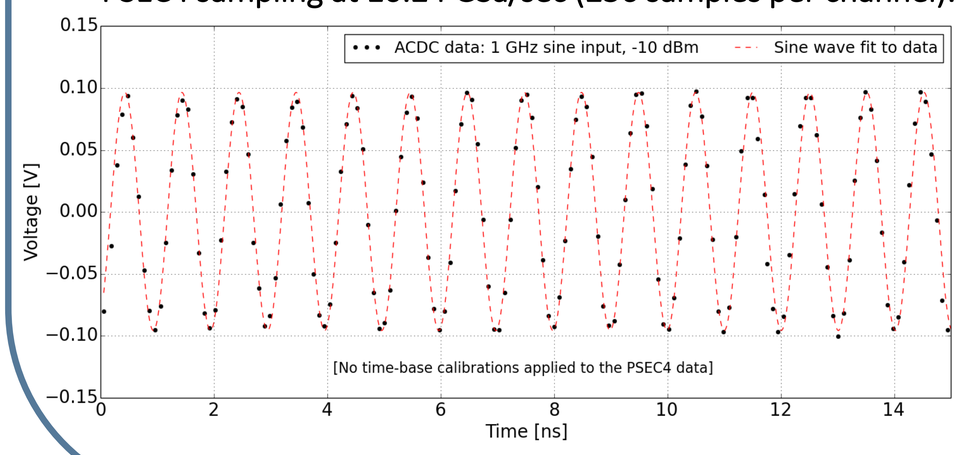
Front-end analog bandwidth[1] > 1 GHz

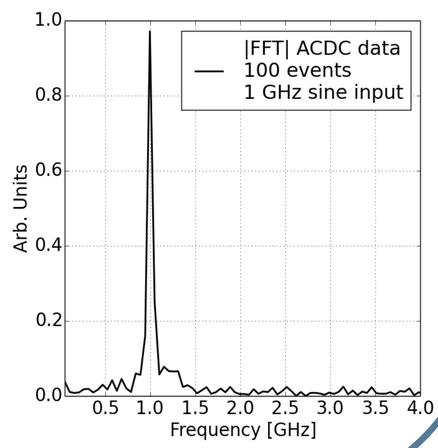


1 V$_{pk2pk}$ signal voltage range[1]



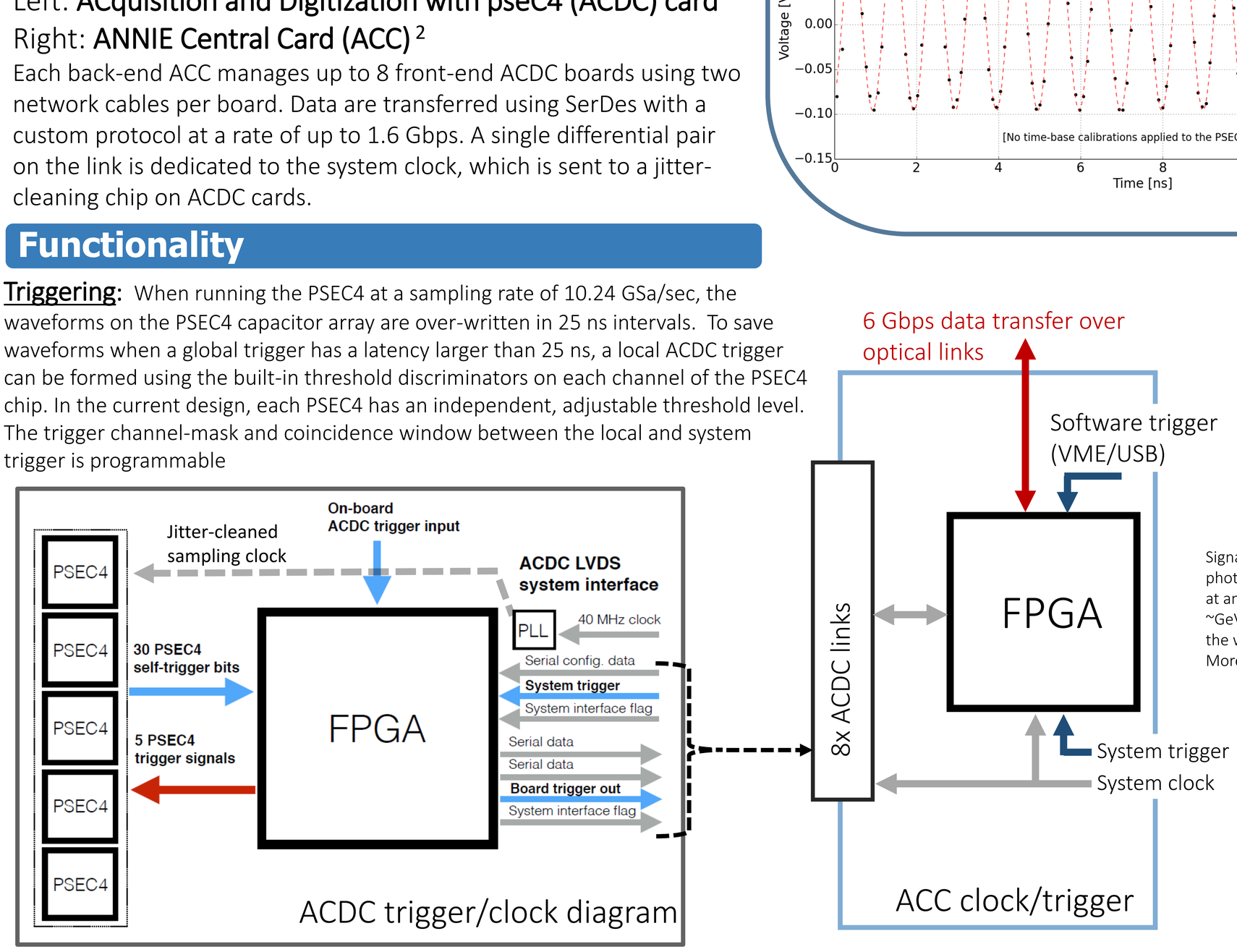
PSEC4 sampling at 10.24 GSa/sec (256 samples per channel):





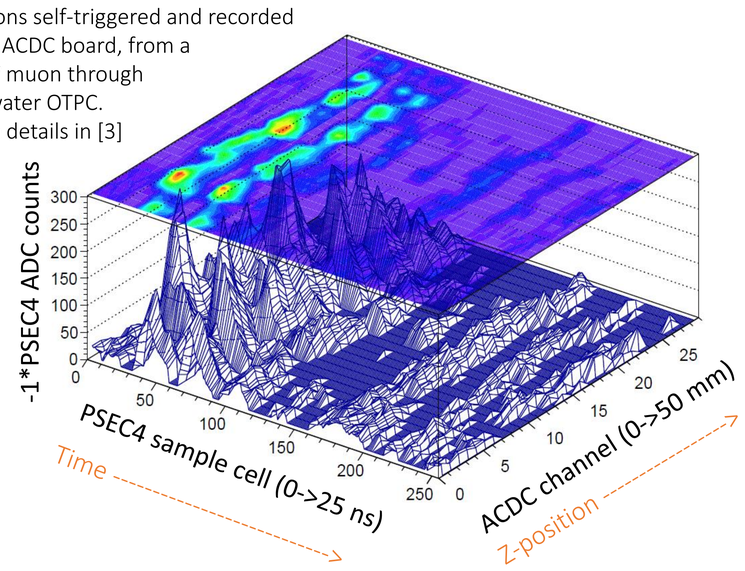
Functionality

Triggering: When running the PSEC4 at a sampling rate of 10.24 GSa/sec, the waveforms on the PSEC4 capacitor array are over-written in 25 ns intervals. To save waveforms when a global trigger has a latency larger than 25 ns, a local ACDC trigger can be formed using the built-in threshold discriminators on each channel of the PSEC4 chip. In the current design, each PSEC4 has an independent, adjustable threshold level. The trigger channel-mask and coincidence window between the local and system trigger is programmable



Test-beam implementation: A 180-channel prototype of this data acquisition system was deployed at the Fermilab test-beam in a water Cherenkov detector using microchannel plate photo-multiplier tubes (MCP-PMT). More details on this experiment, the 'optical time-projection chamber' (OTPC), are found in [3]. The ACDC boards formed level-0 triggers using the trigger bits from PSEC4-discriminated single photon MCP-PMT pulses (~1 ns FWHM). Data were read out from the ACDC cards if a global trigger was registered at the Central Card.

Signal from a number of Cherenkov photons self-triggered and recorded at an ACDC board, from a ~GeV muon through the water OTPC. More details in [3]



References

[1] E. Oberla et al. Nucl. Instrum. Meth. A735 (2014) 452-461

[2] M. Wetstein et al., 'Letter of Intent: ANNIE', arXiv:1504.01480

[3] E. Oberla et al. Nucl. Instrum. Meth. A814 (2016) 19-32

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