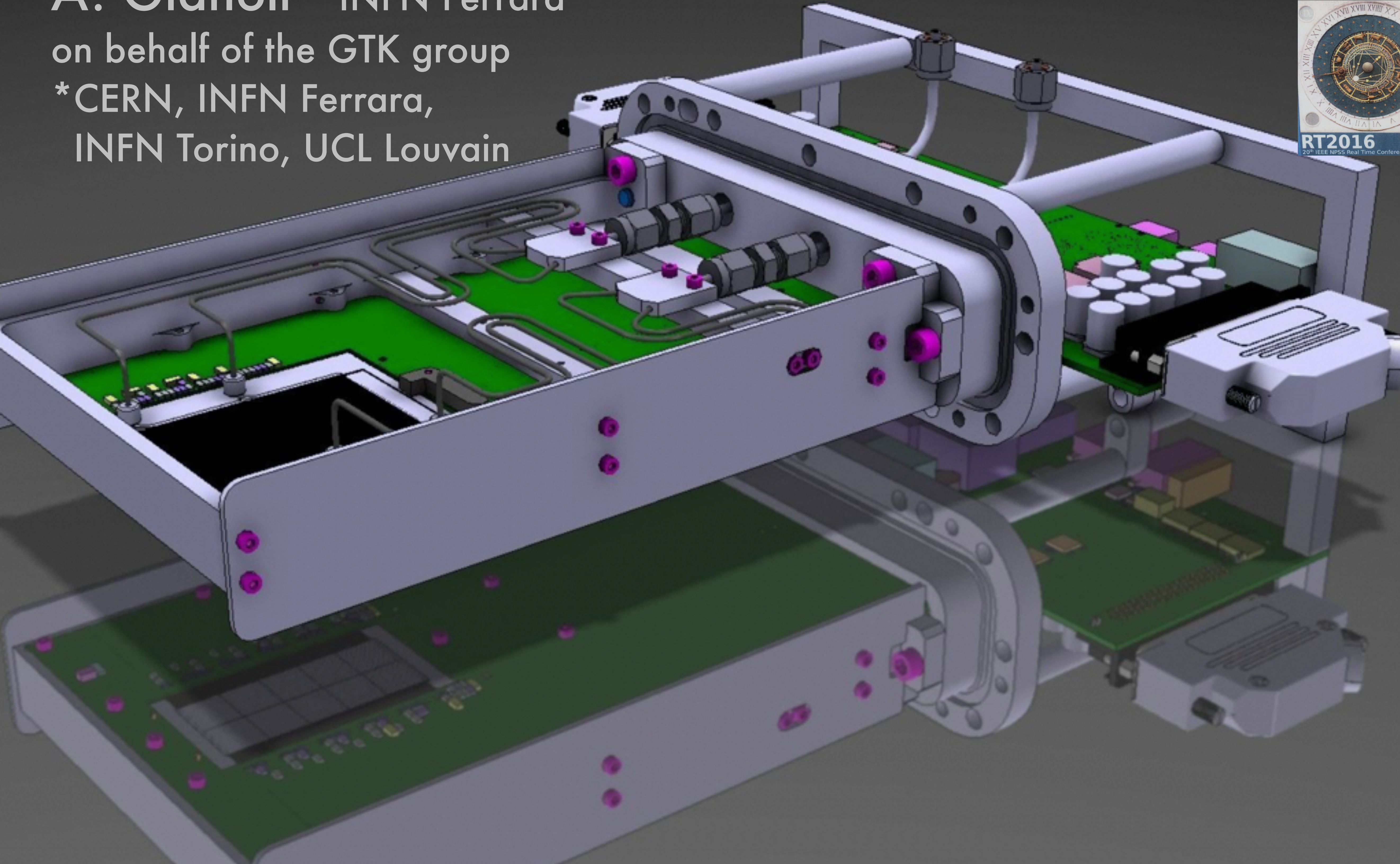
A. Gianoli* INFN Ferrara
on behalf of the GTK group
*CERN, INFN Ferrara,
INFN Torino, UCL Louvain

RT2016, Padua, 9 June 2016



The NA62 GigaTracker detector

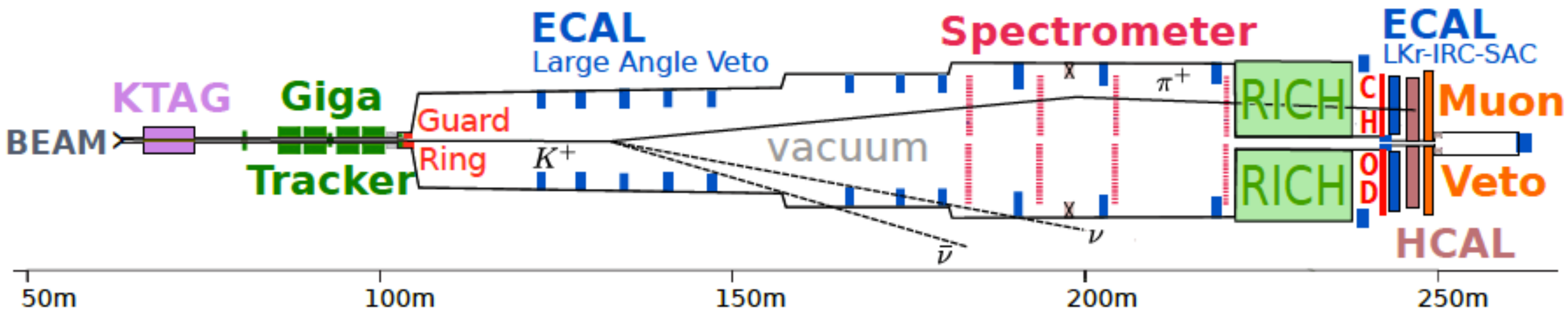
The NA62 experiment

Fixed target experiment: precision kaon physics @Cern SPS

Ultra rare K decays $K^+ \rightarrow \pi^+ \nu \bar{\nu}$

How rare is it? **1 in 10^{10}-10^{11} particle decays**

Aim to get O(100) events in 2-3 years



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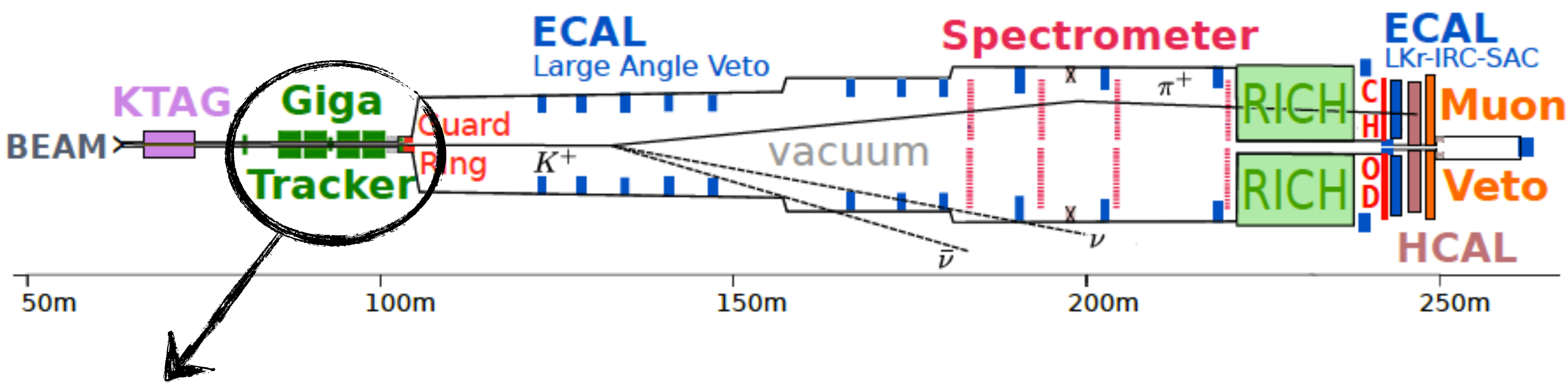

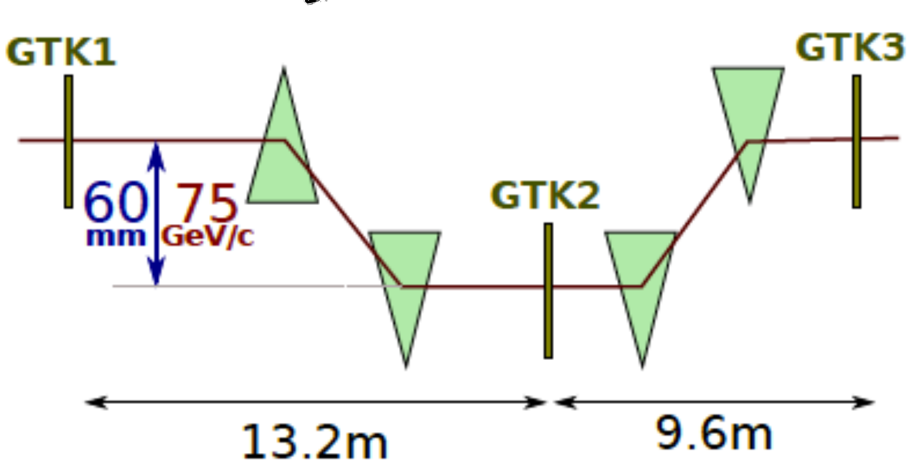

GTK measures initial state kinematics and arrival time

It sees the whole beam!

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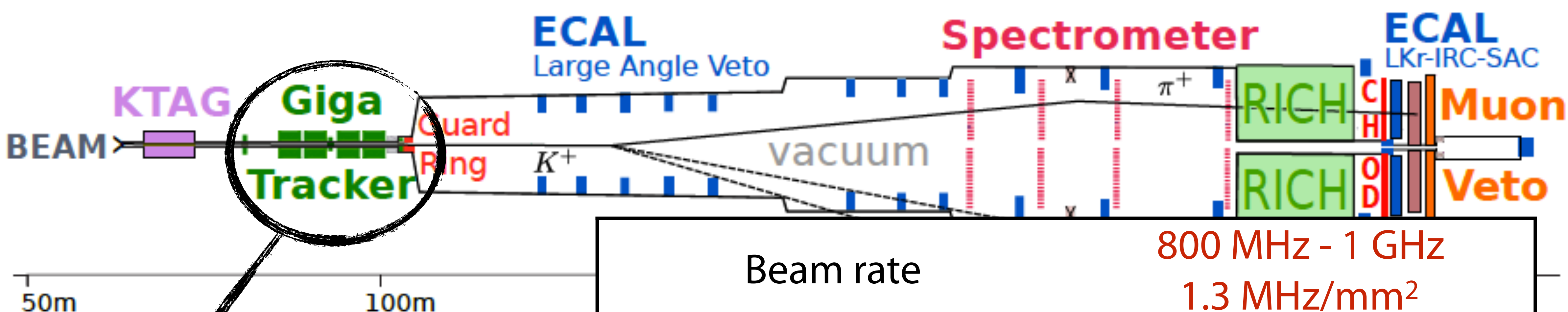
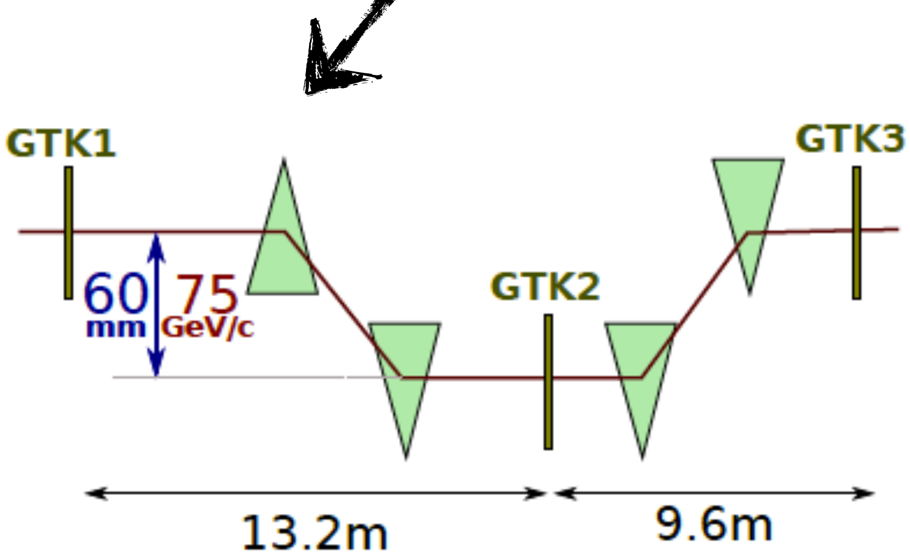
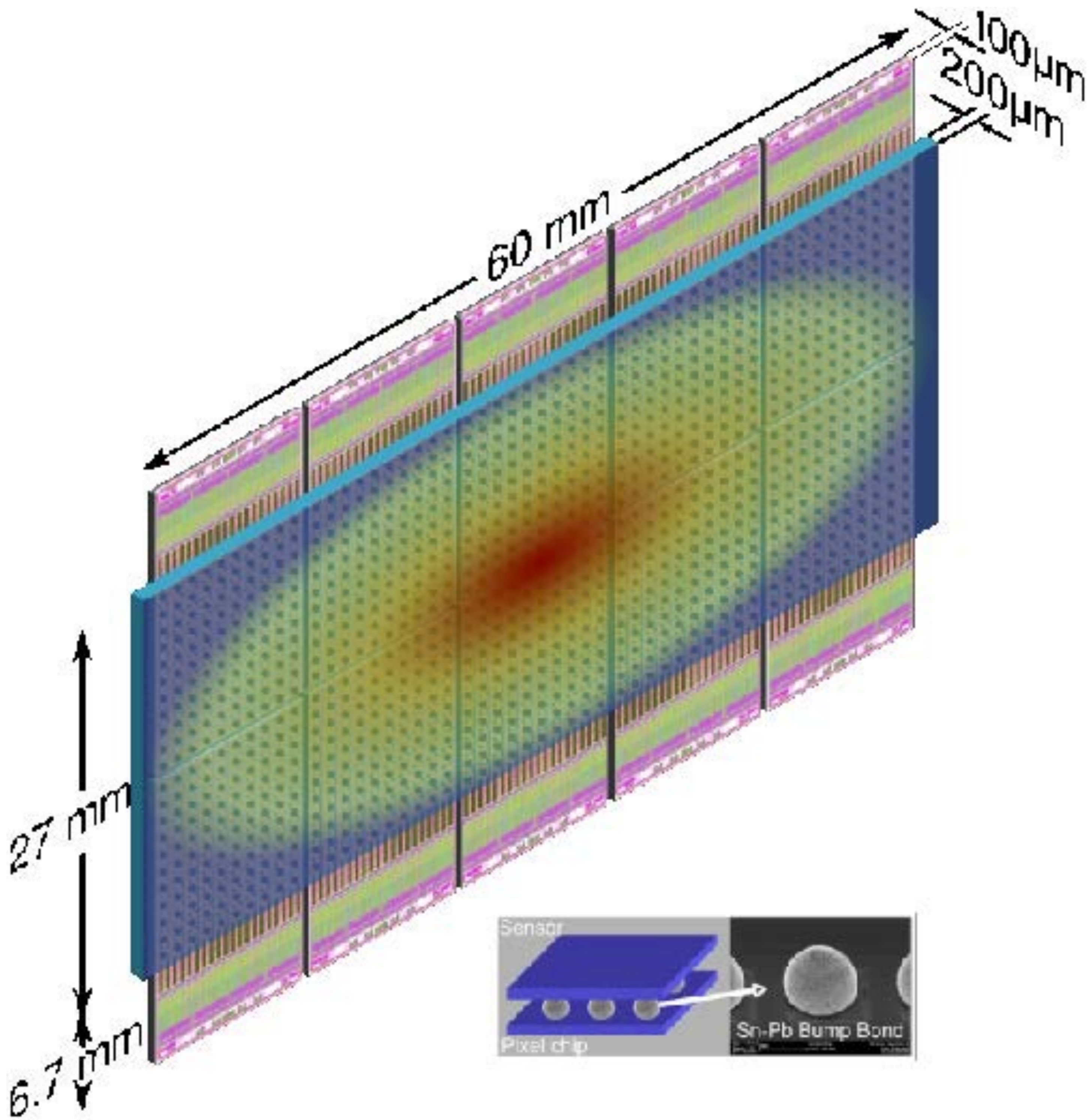




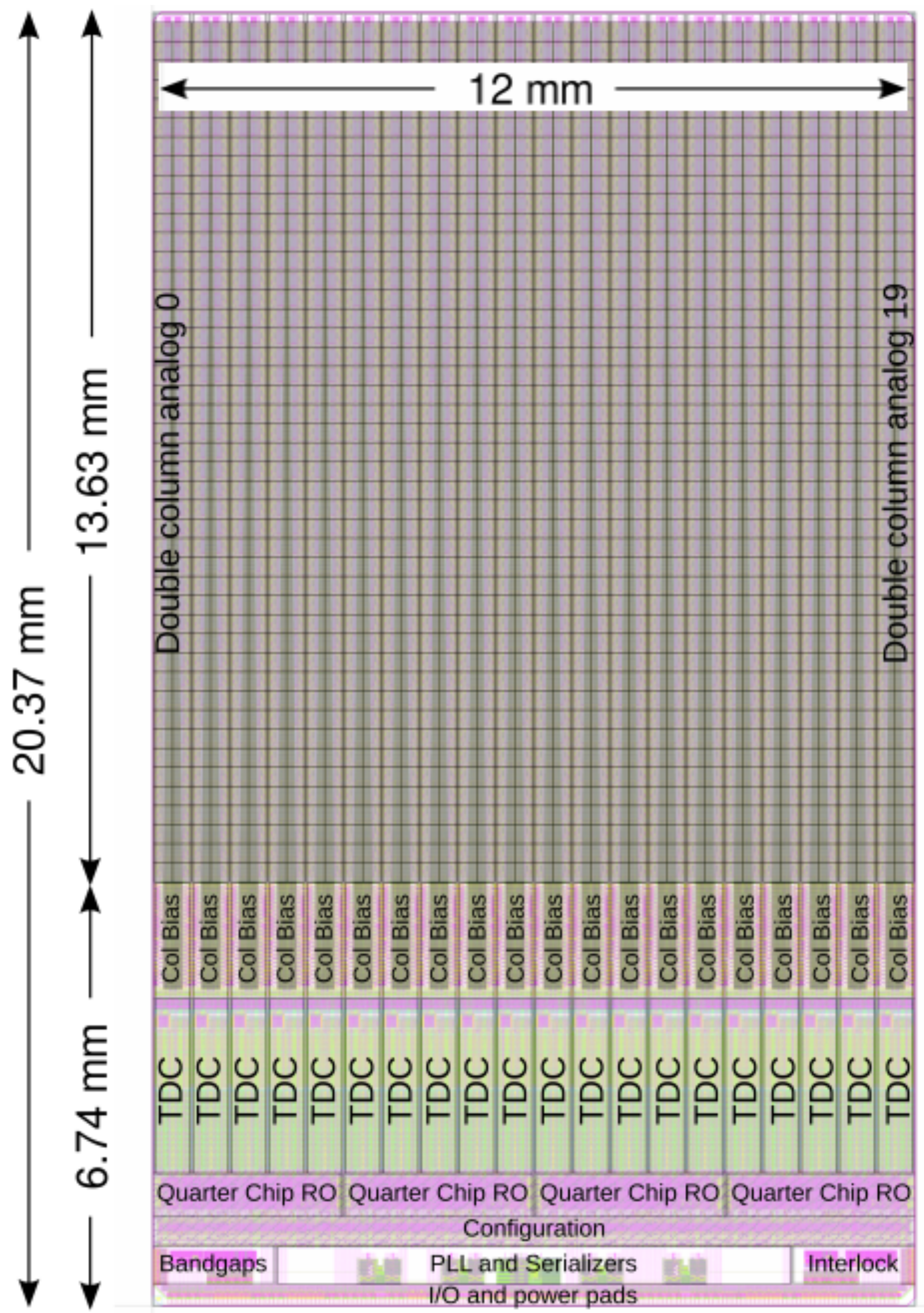
Beam rate	800 MHz - 1 GHz 1.3 MHz/mm^2
Radiation	10^{14} 1MeV eq n/cm^2/y
Efficiency	99%
Momentum resolution	0.2%
Angular resolution	16 μrad
Hit time resolution	200ps RMS
Material Budget	$3 \times 0.5\% X_0$
Detector size	60mm × 27mm

Sensor-Chip Assembly



- Sensor [FBK,CIS]
  Both p-in-n/n-in-p
  Bias: 300 - 600 V
  Thickness: 200 µm
  MPV Charge per MIP: 2.4 fC
- Bump-bonding Sn-PB [IZM]
- 10 TDCPix chips/station: 130 nm CMOS [IBM] thinned at 100 µm
- Detector replaced every 100 days of beam (radiation)

The Front End Chip - TDCPix



- Design by Cern PH-EFE:
  - -1800 pixels (40col × 45pix)
  - -each pixel (300 × 300) μm^2
  - -separate analog-digital: no high freq clock to pixels

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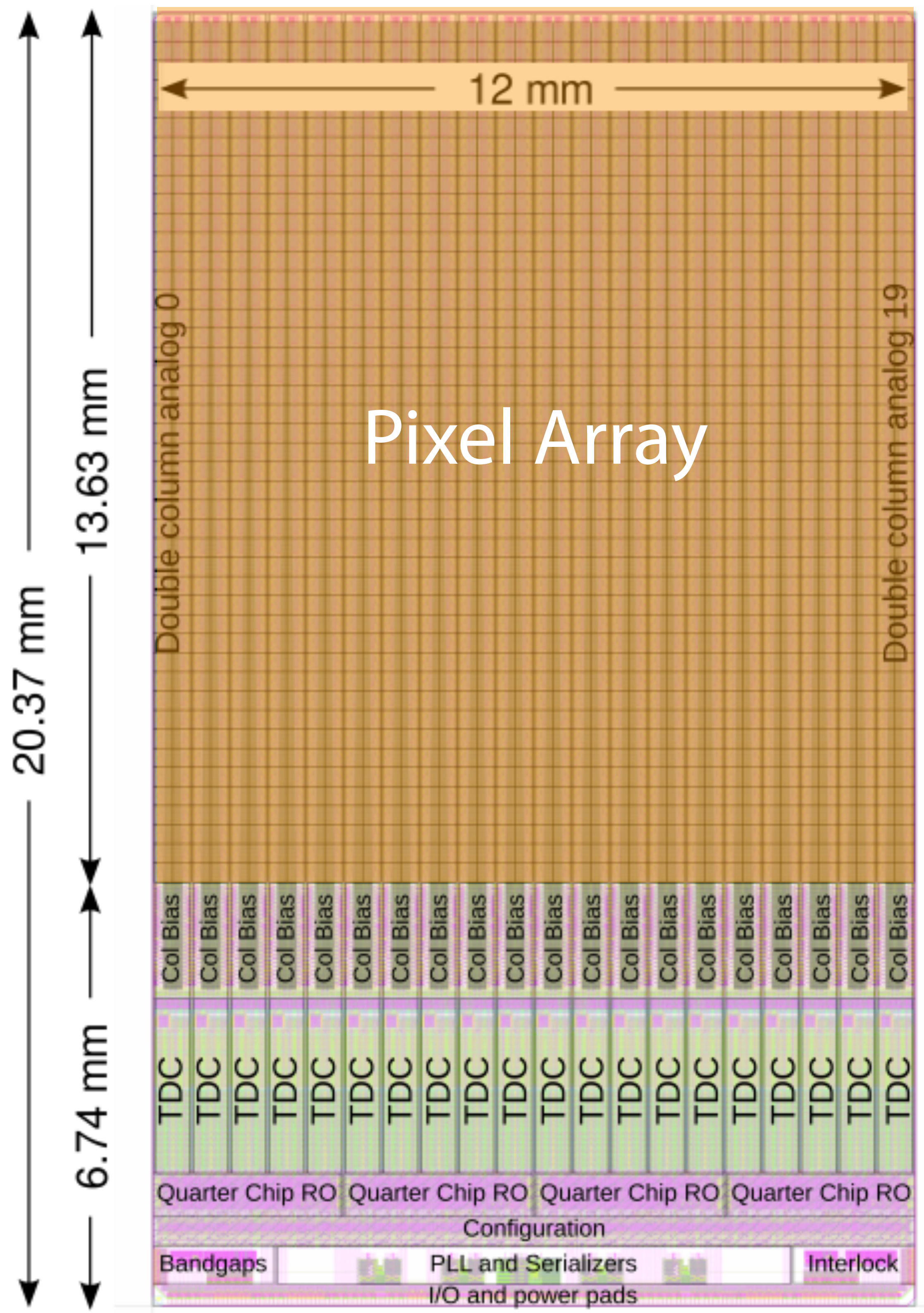

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  - -discriminator
  - -DAC threshold trim
  - -configuration register

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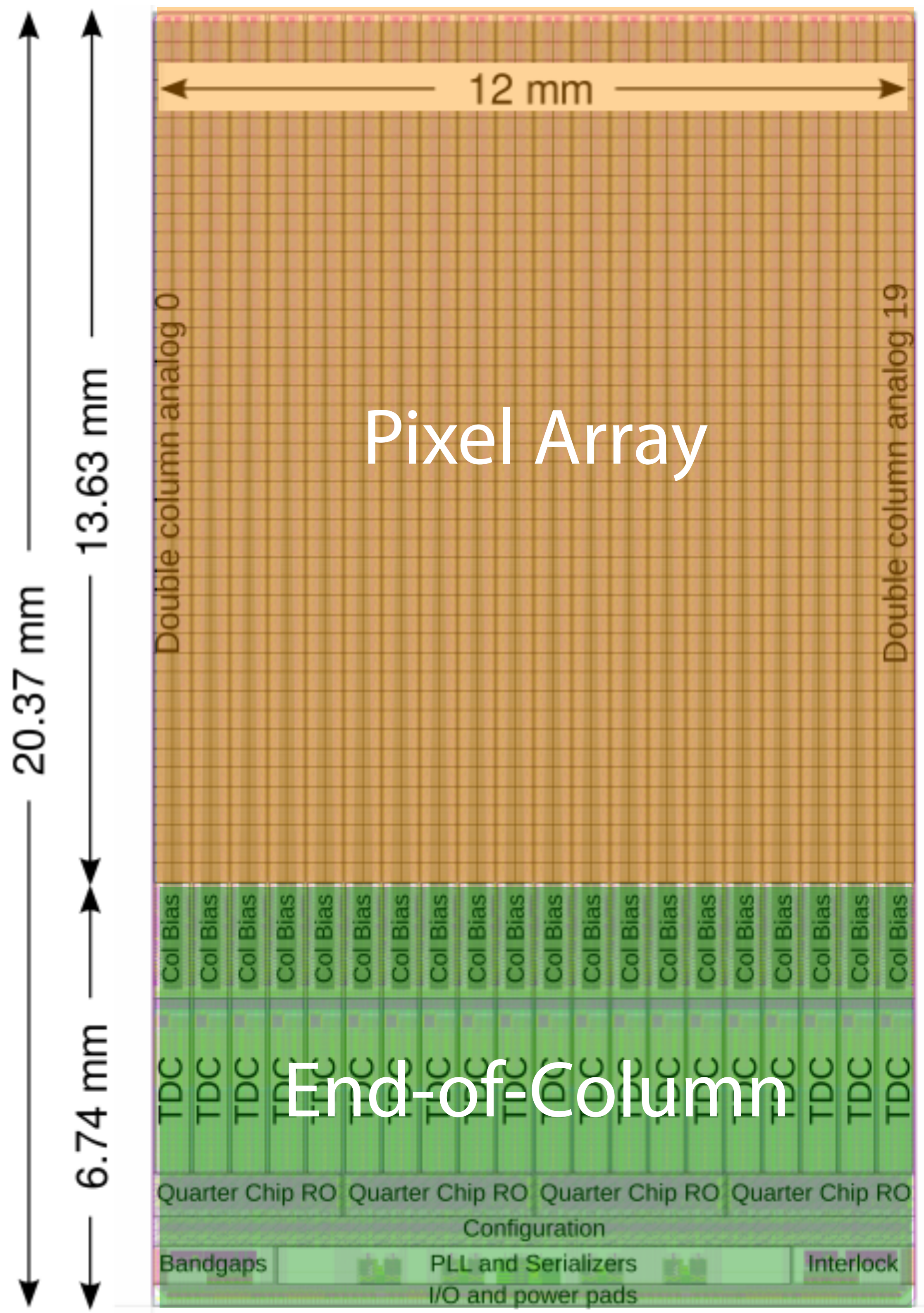

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  - -time-to-digital converters (TDC)
  - -data serializers

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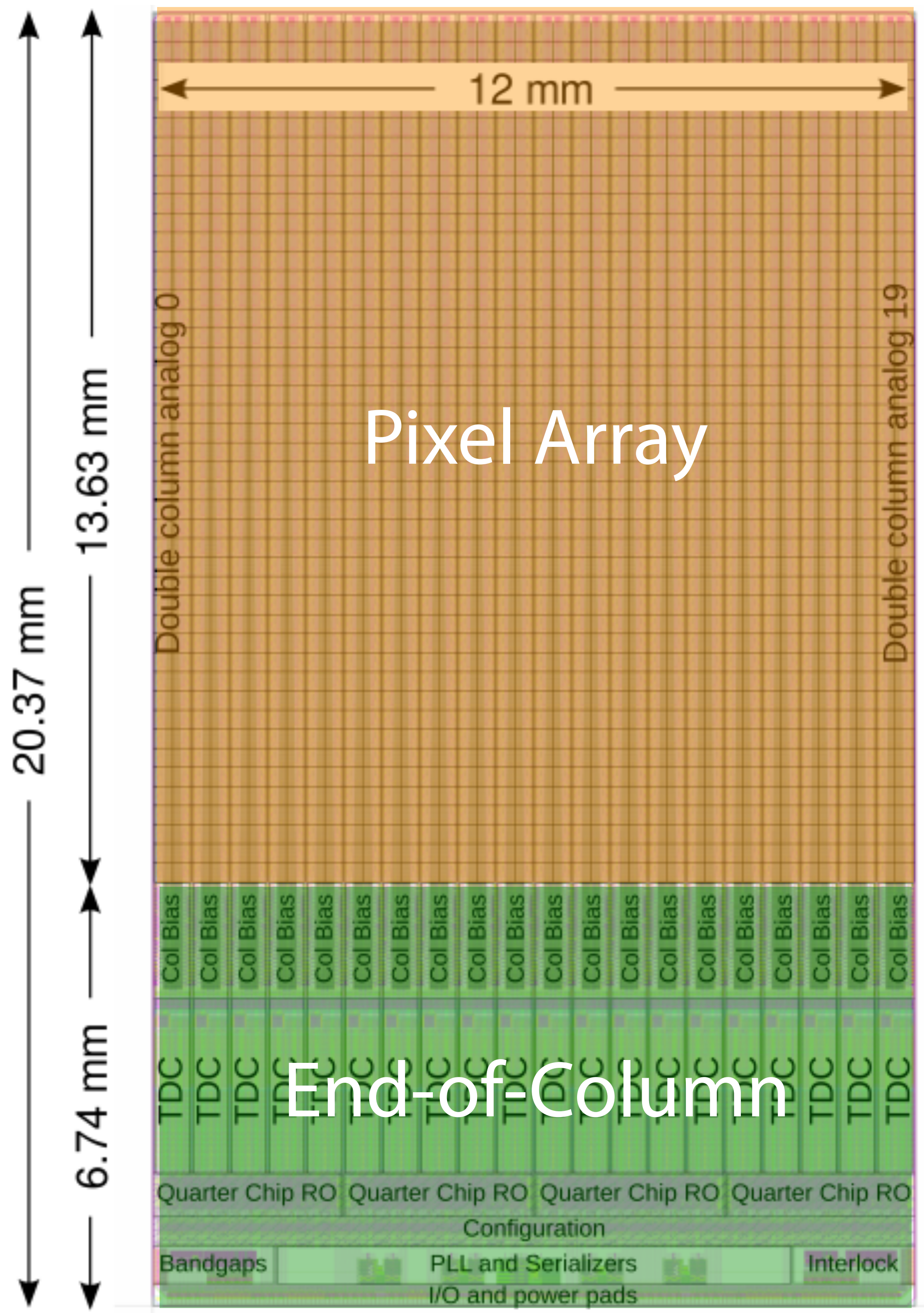

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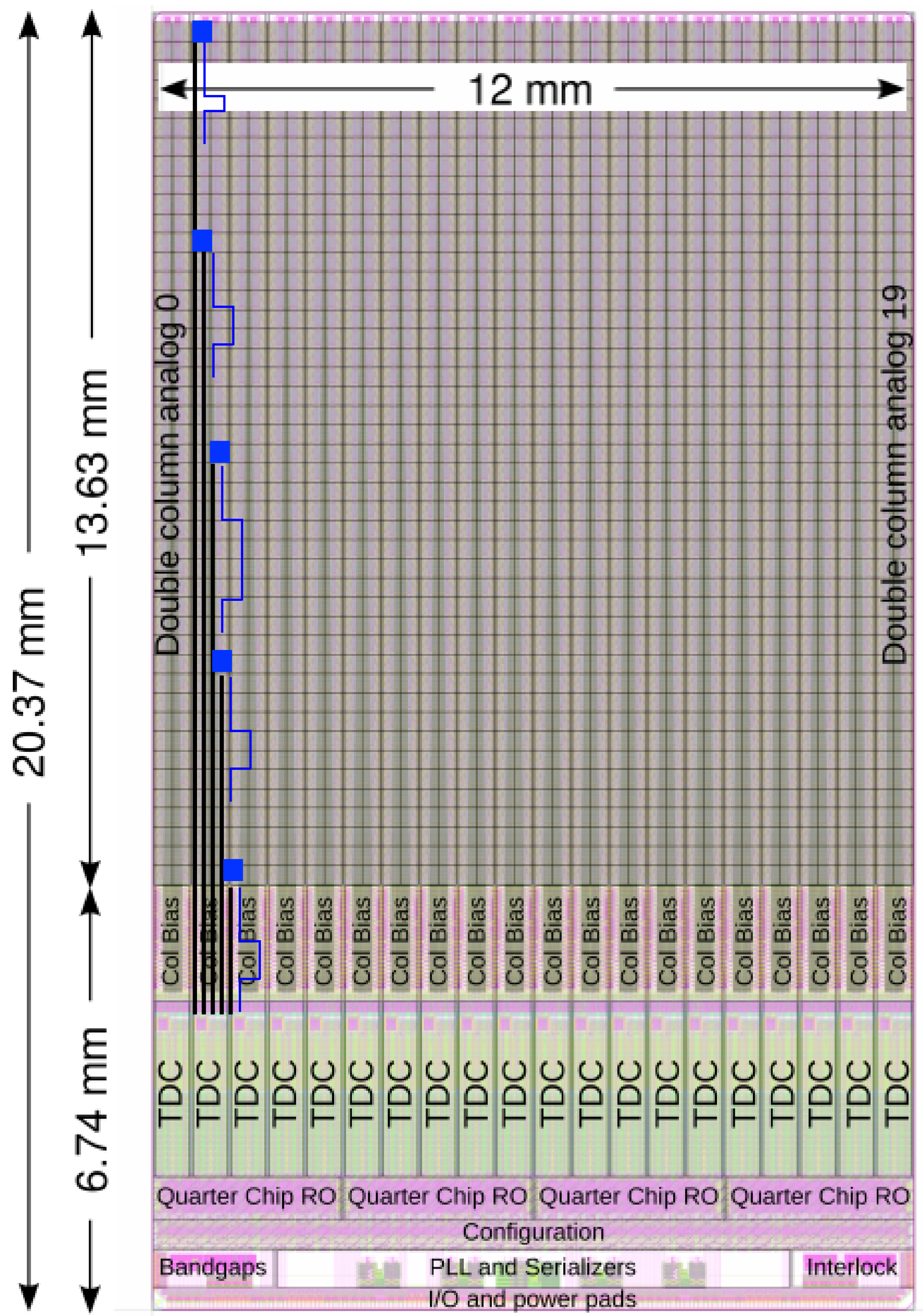
- **Power consumption:** ~3.5W, mostly EoC

TDCPix End of Columns



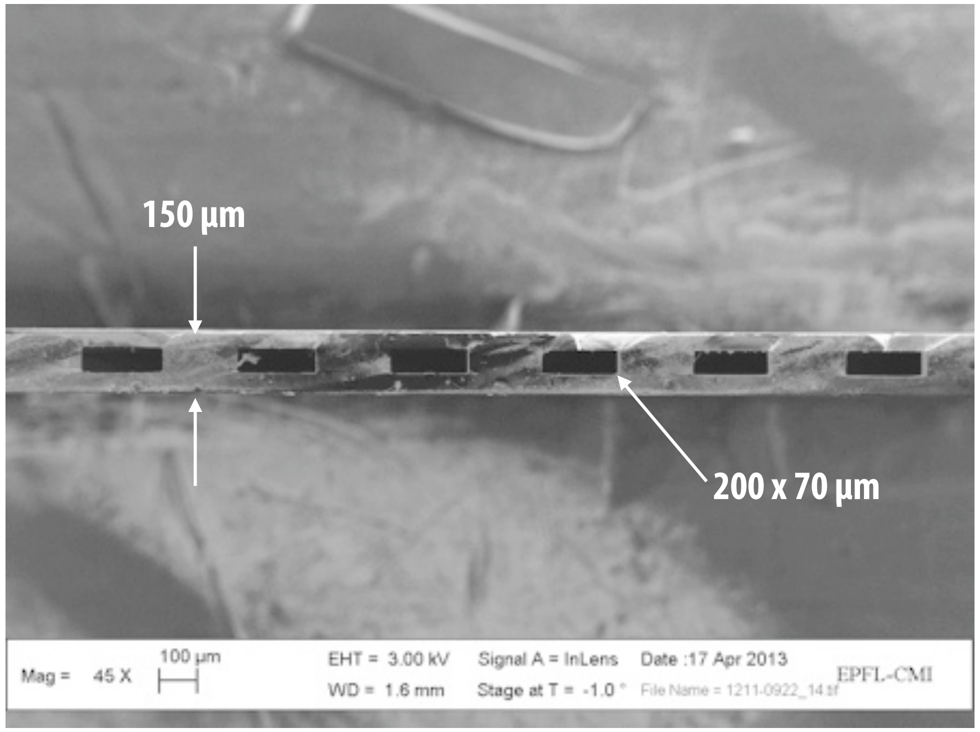
- Signals from 5 non adjacent pixels in a column are sent to a multiplexer (HitArbiter)
- Each HitArbiter has a TDC pair measuring leading and trailing edges → 360 TDC pair/chip
- TDC have 100 ps bins
- Self triggered operation: rate 210 MHits/s
- Data sent out using four 3.2 Gb/s serializers

Microchannel cooling

- Physics performance requires to minimize the material budget
- Detector is in vacuum
- Need to dissipate ~35 W/station

Micro-channel cooling matches the constrains:

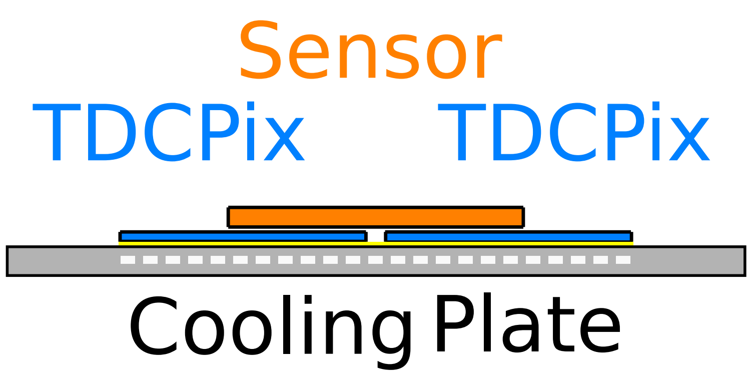
- designed by Cern PH-DT group
- silicon-silicon assembly, (200 × 70) μm^2 channels
- low material budget: 130 μm of silicon (< 0.15% X_0)

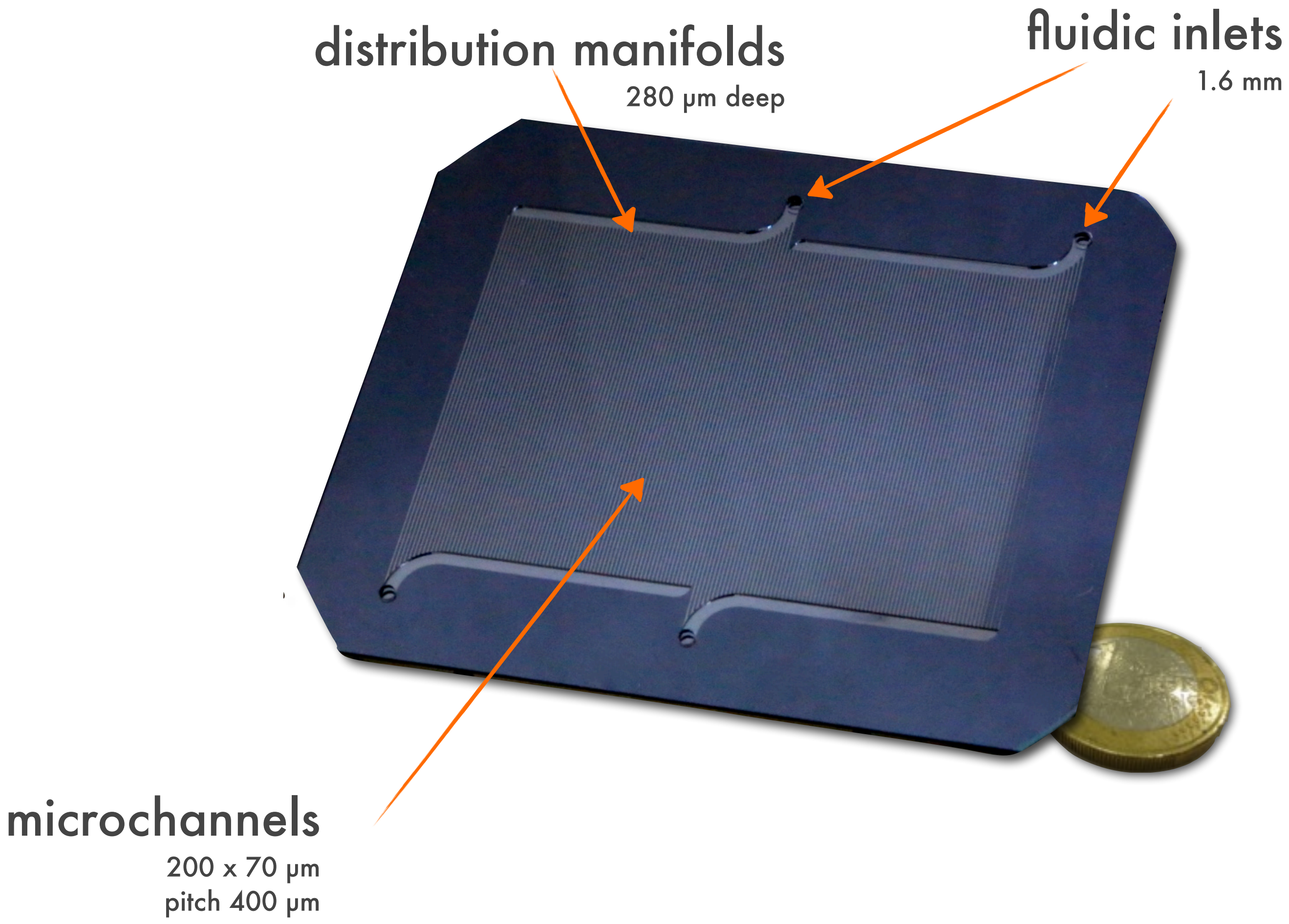


Courtesy: A. Mapelli

Mechanical integration

- Detector glued on 130 µm Silicon Cooling Plate





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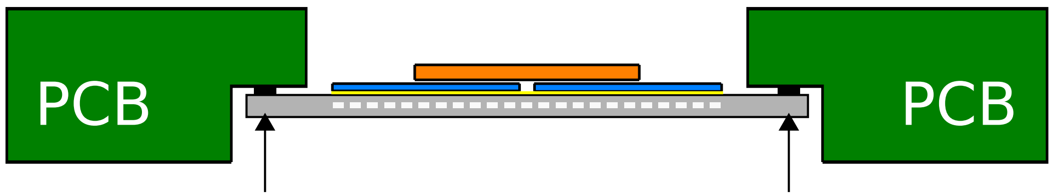

- Cooling plate is clamped onto PCB

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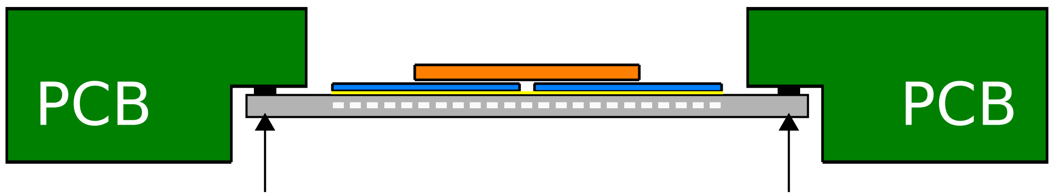
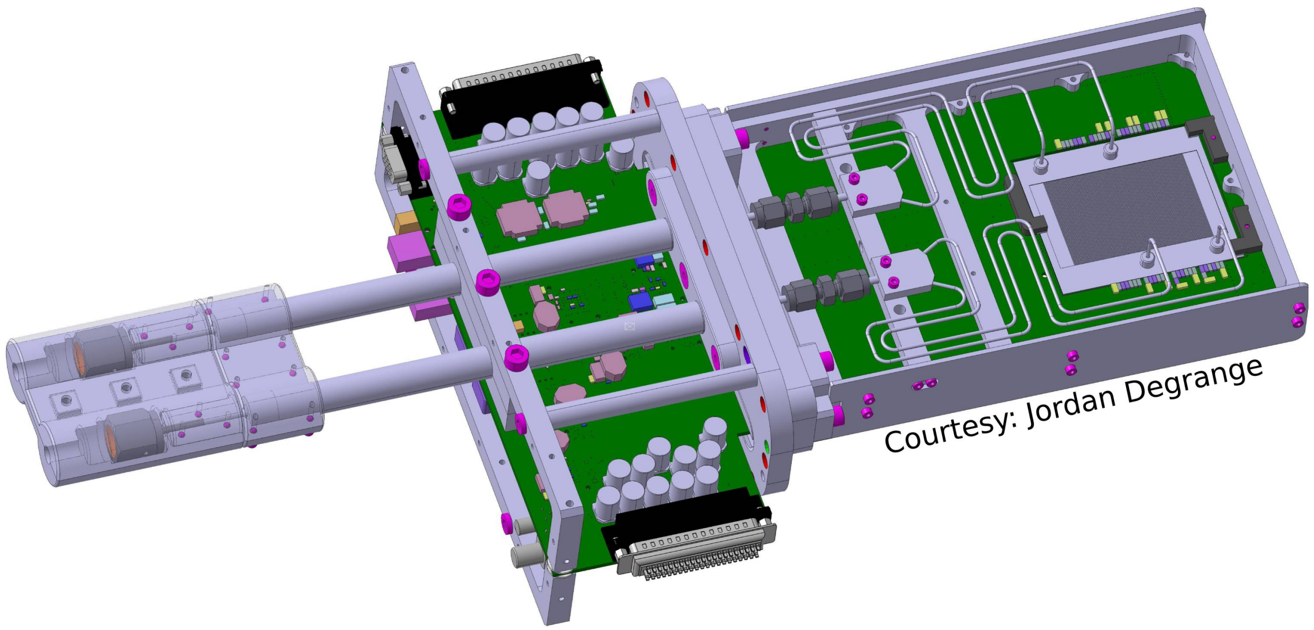


- Cooling plate is clamped onto PCB

- PCB is glued into frame and flange



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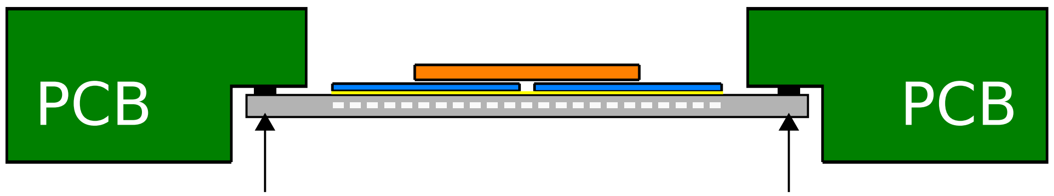

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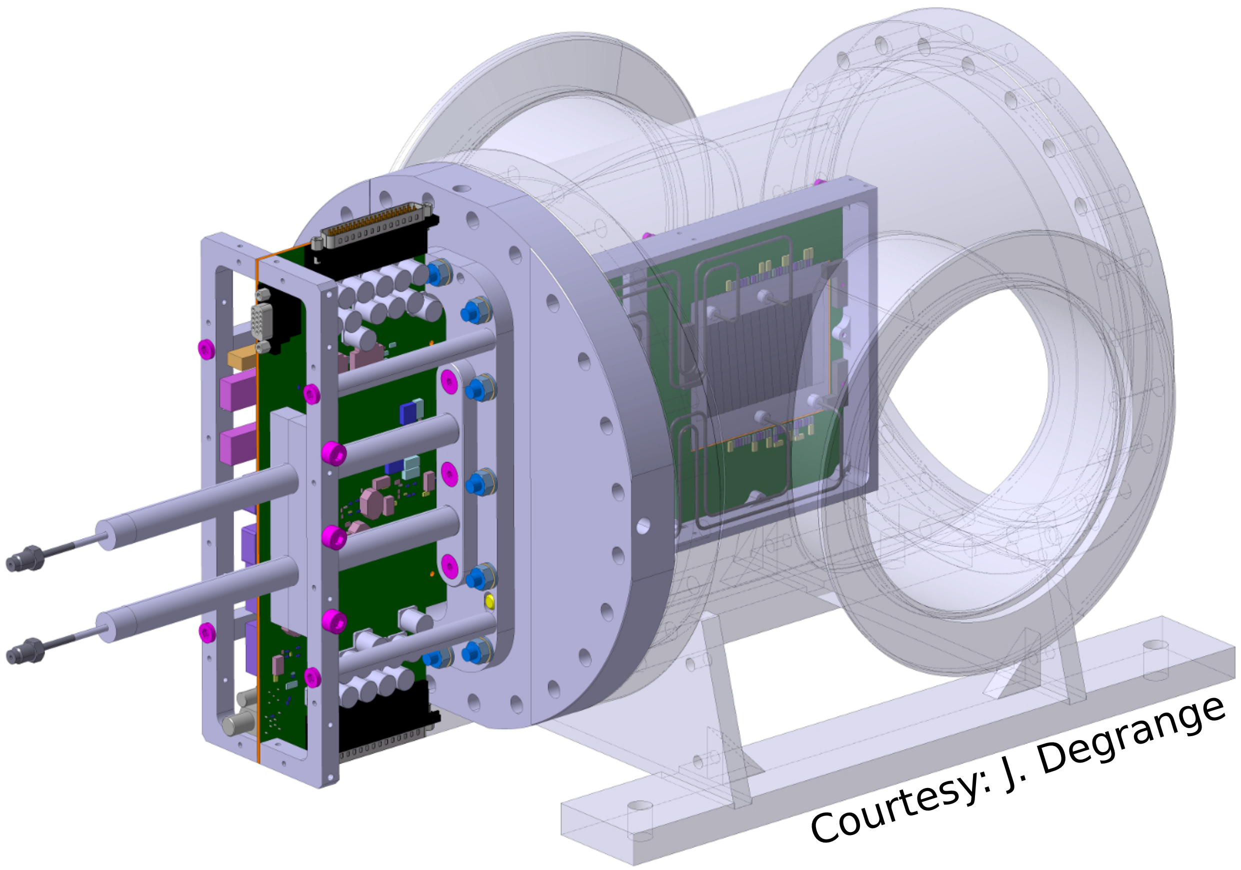
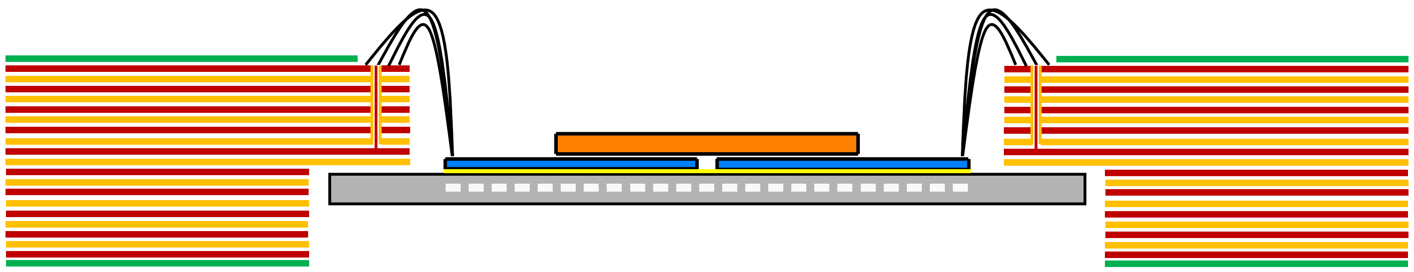
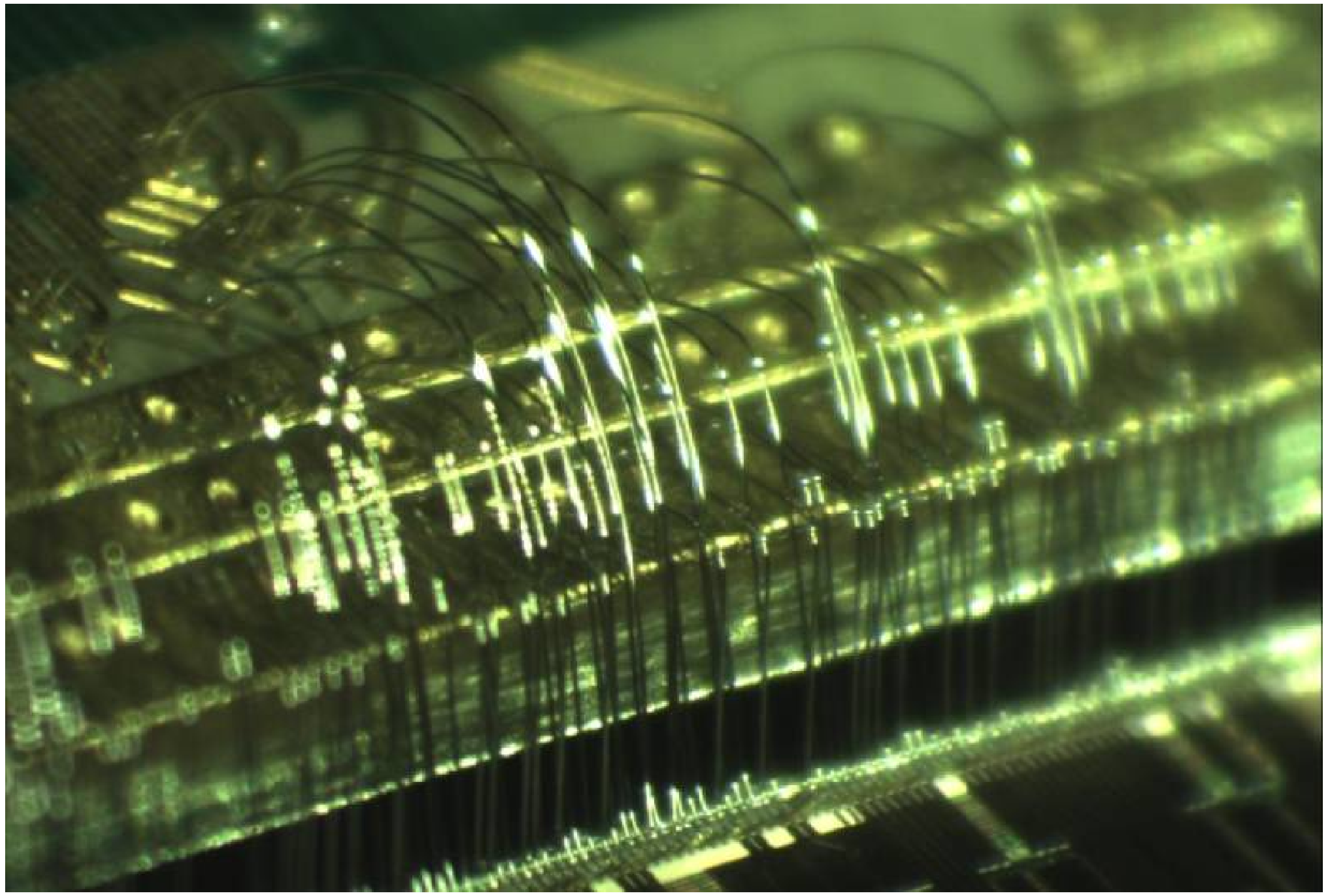


- Flange closes the vacuum vessel

Electrical integration

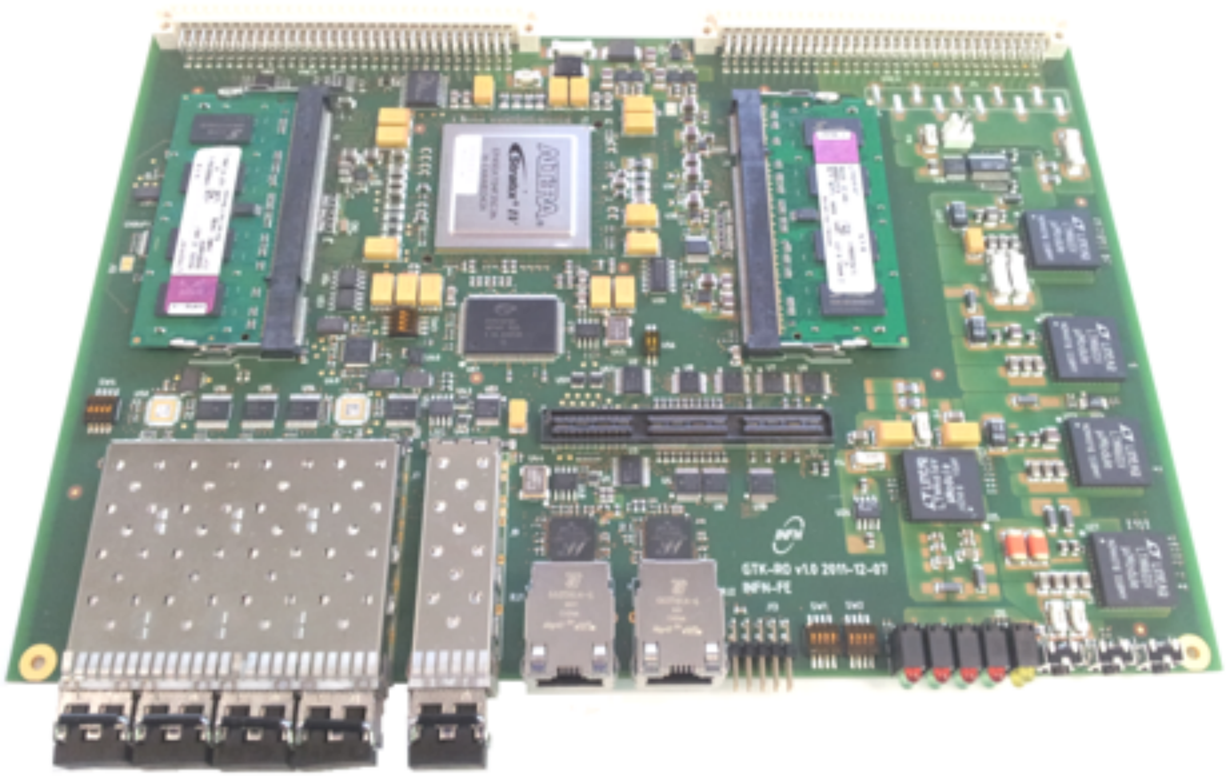
- TDCPix wired bonded to PCB: dense wire-bonding scheme (73 µm pitch on chip)
- PCB routes power, clock, control and signal lines to/from the off-detector electronics
- Complex PCB:
  - 14 layers
  - 40 differential 3.2 Gb/s signals over 30 cm





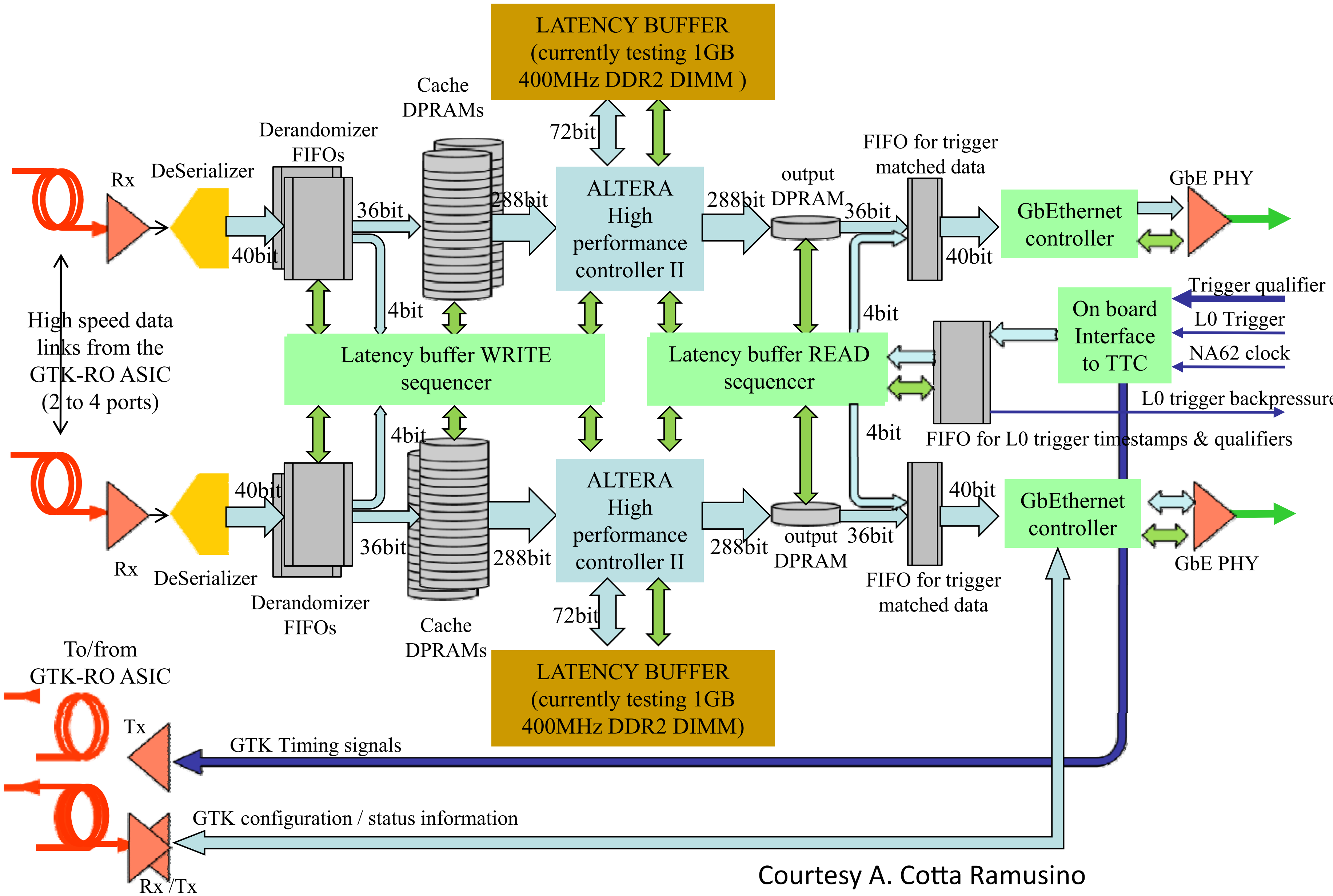
Data acquisition- GTK-RO

- TDCPix sends out every hit: trigger matching needed
- GTK-RO built using FPGA (Altera Stratix GX110)
- Each GTK-RO made of two decked cards: daughter card handles interface with TTC
- Each TDCPix is connected to one DAQ board (GTK-RO) through 4 optical links (one per TDCPix 3.2 Gb/s serializer) + 1configuration link. Transmission is data driven



Data acquisition- GTK-RO

- GTK-RO board must
  - buffer data, waiting for level-0 trigger decision (max level-0 trigger latency is 1 ms)
  - retrieve data in a 75 ns time window upon each trigger request, and send them to the subdetector PC using UDP



Courtesy A. Cotta Ramusino

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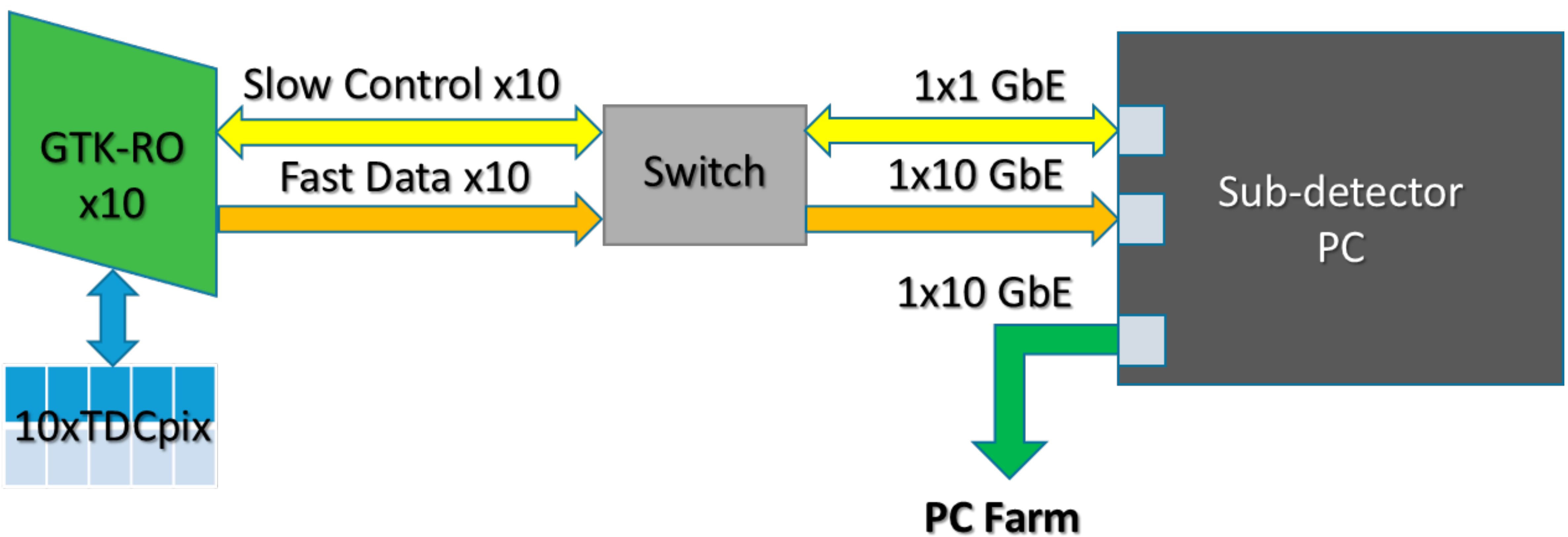


Data acquisition- Detector PC

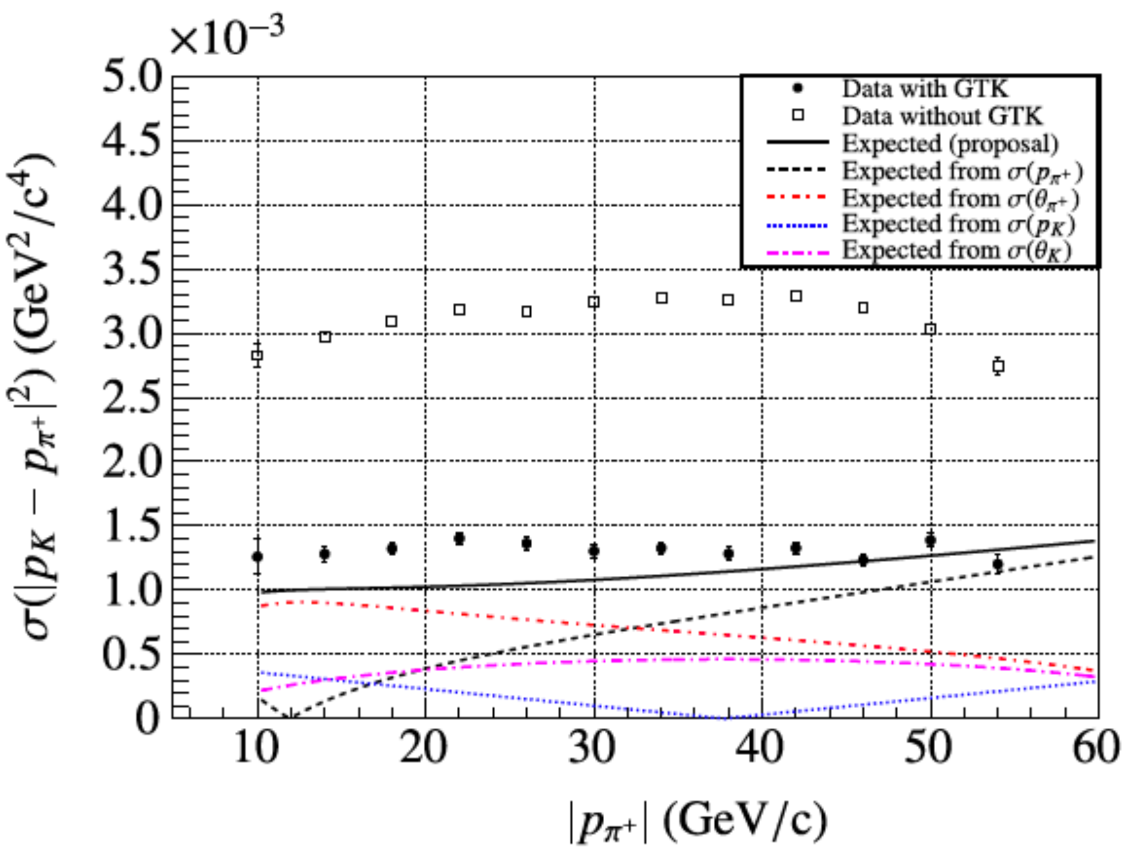
- Assemble data from several GTK-ROs and send it to the online farm
- Plain linux distribution as O.S. with "zero copy" module of PF_RING to reduce memory to memory copy.
- Multiple threads to handle the amount of data (worst case ~82 MB/s from each chip+protocol overhead)

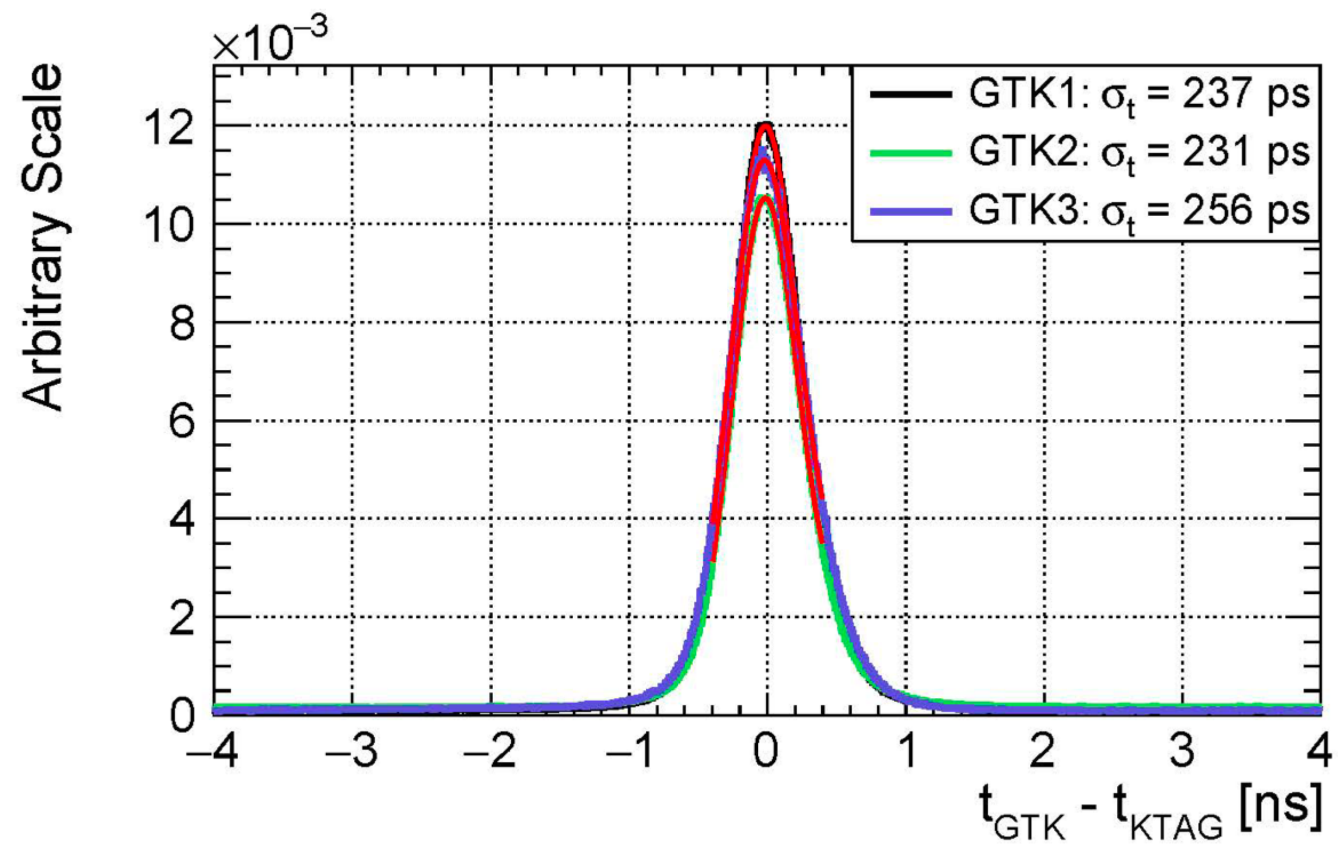
Changes in 2016

- Spikes in instantaneous beam intensity → use 2 PCs/station
- Possibility to become L1-detector: GTK data not used for first sw trigger → readout GTK only in response to L1 triggers

Results

- All stations + infrastructure installed and commissioned in 2015
- GTK cooled at 0 °C (2 g/s of C_6F_{14} at 3 bar), thresholds set to 0.7 fC, bias voltage ~300V
- time resolution ≃ 215 ps @ 300V





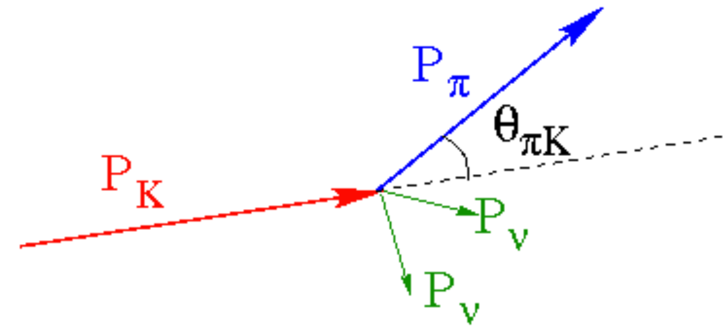
ktag $\boldsymbol{\sigma}_t$ ≃ 80 ps

Thank you for your attention

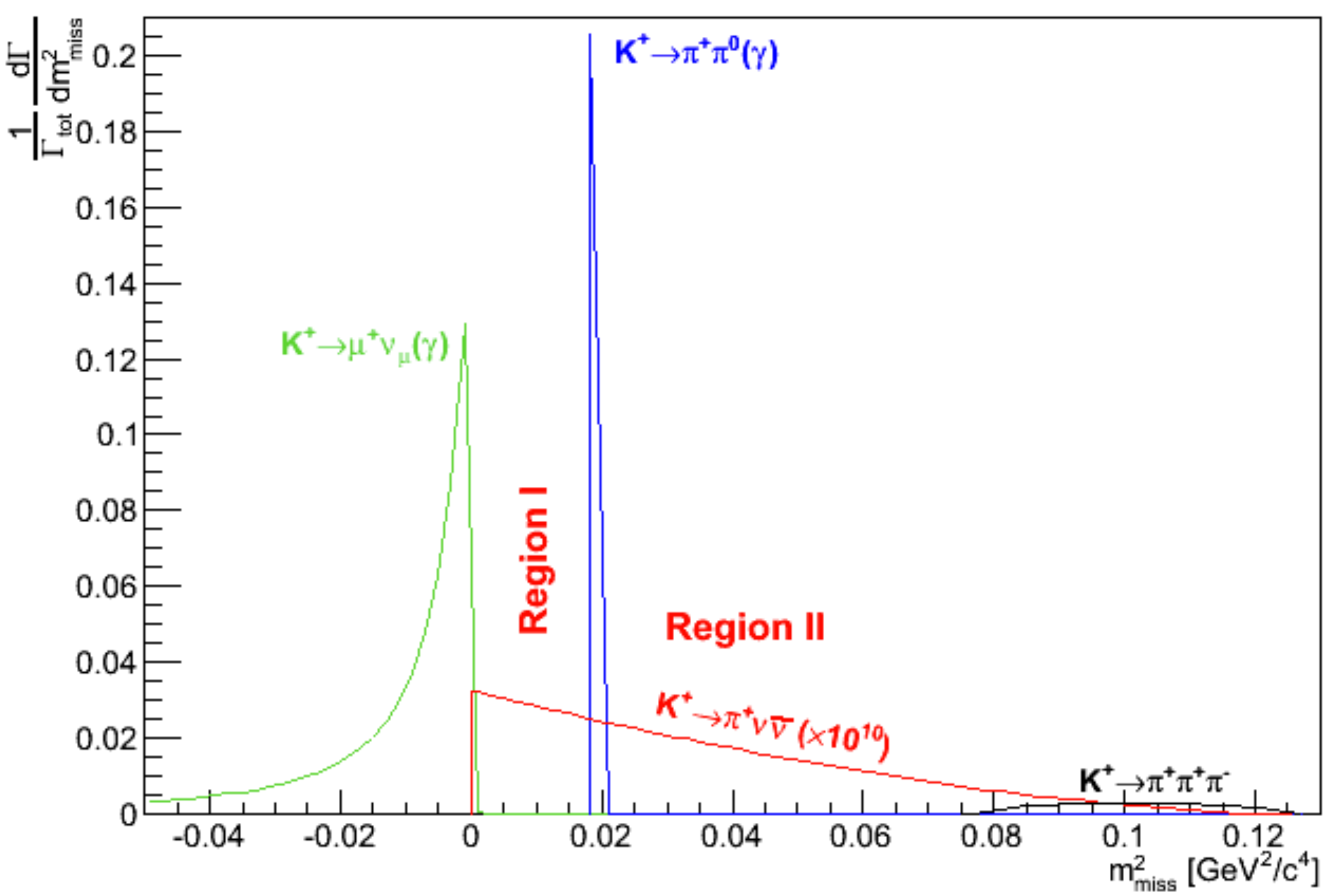
SPARES

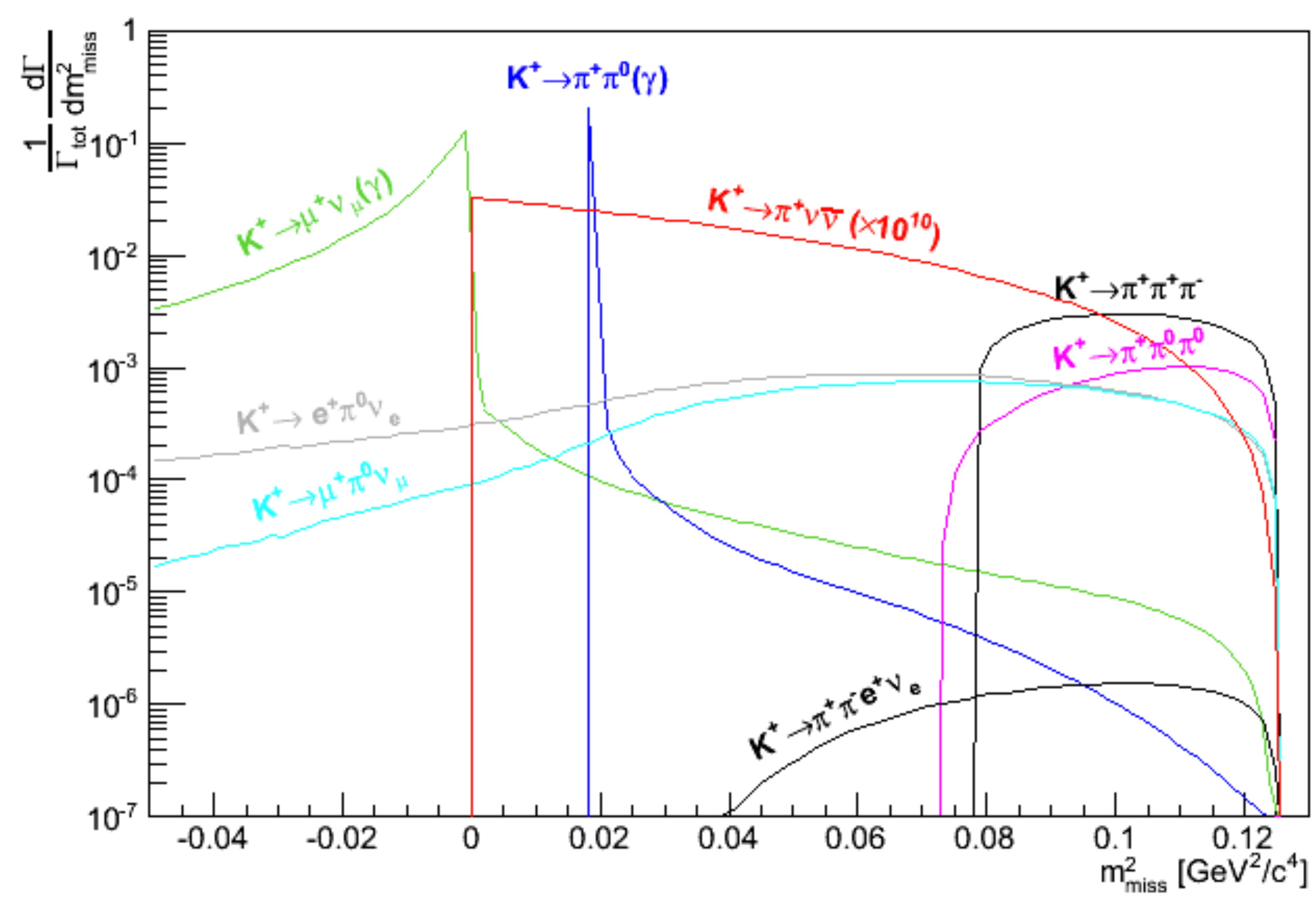
NA62 signal and background

- Signal: $m^2_{miss} = (P_K - P_\pi)^2$

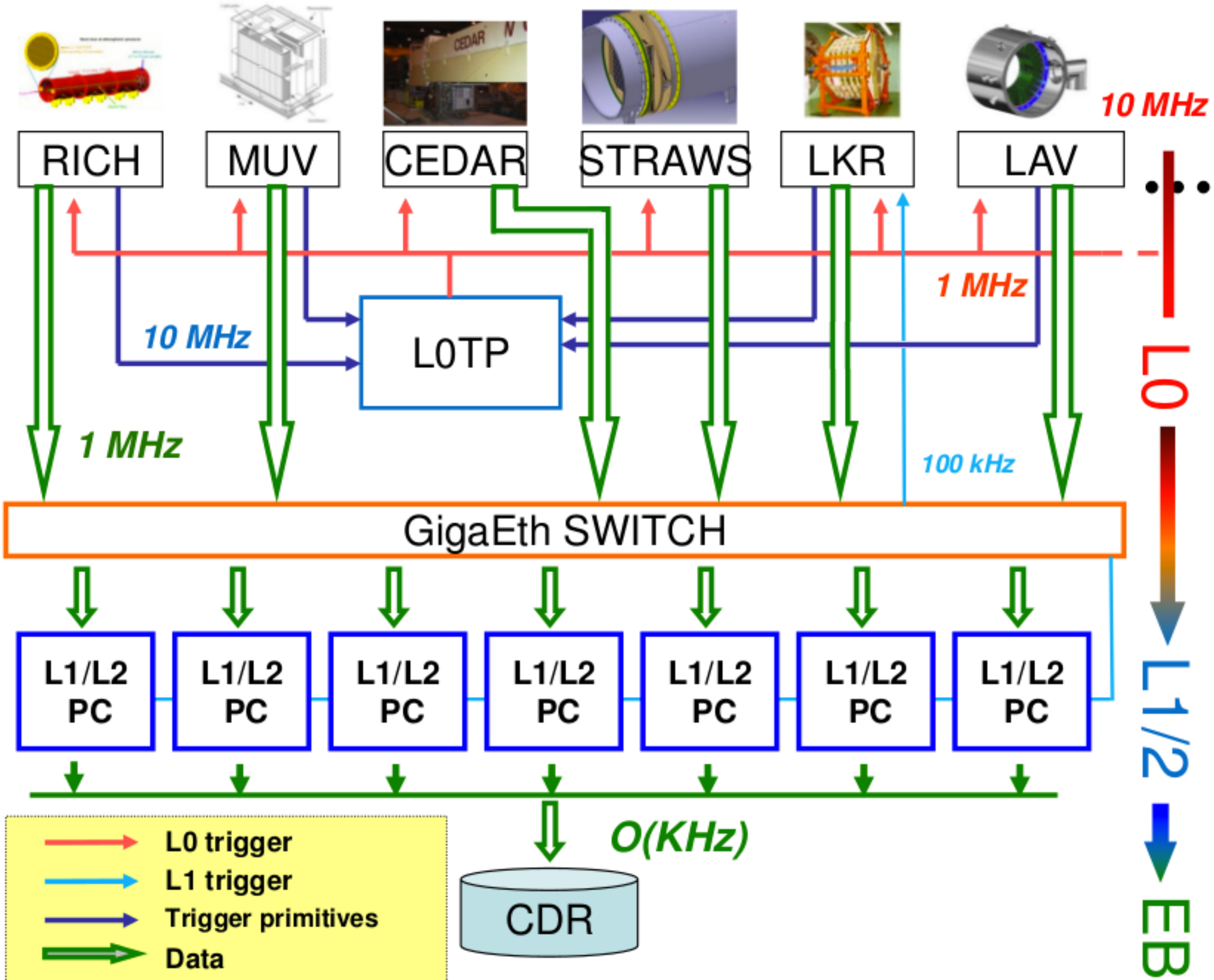


- Background:
  - a) K^+ decay modes
  - b) accidental single track matched with K-like one





Trigger and Data Acquisition (TDAQ)

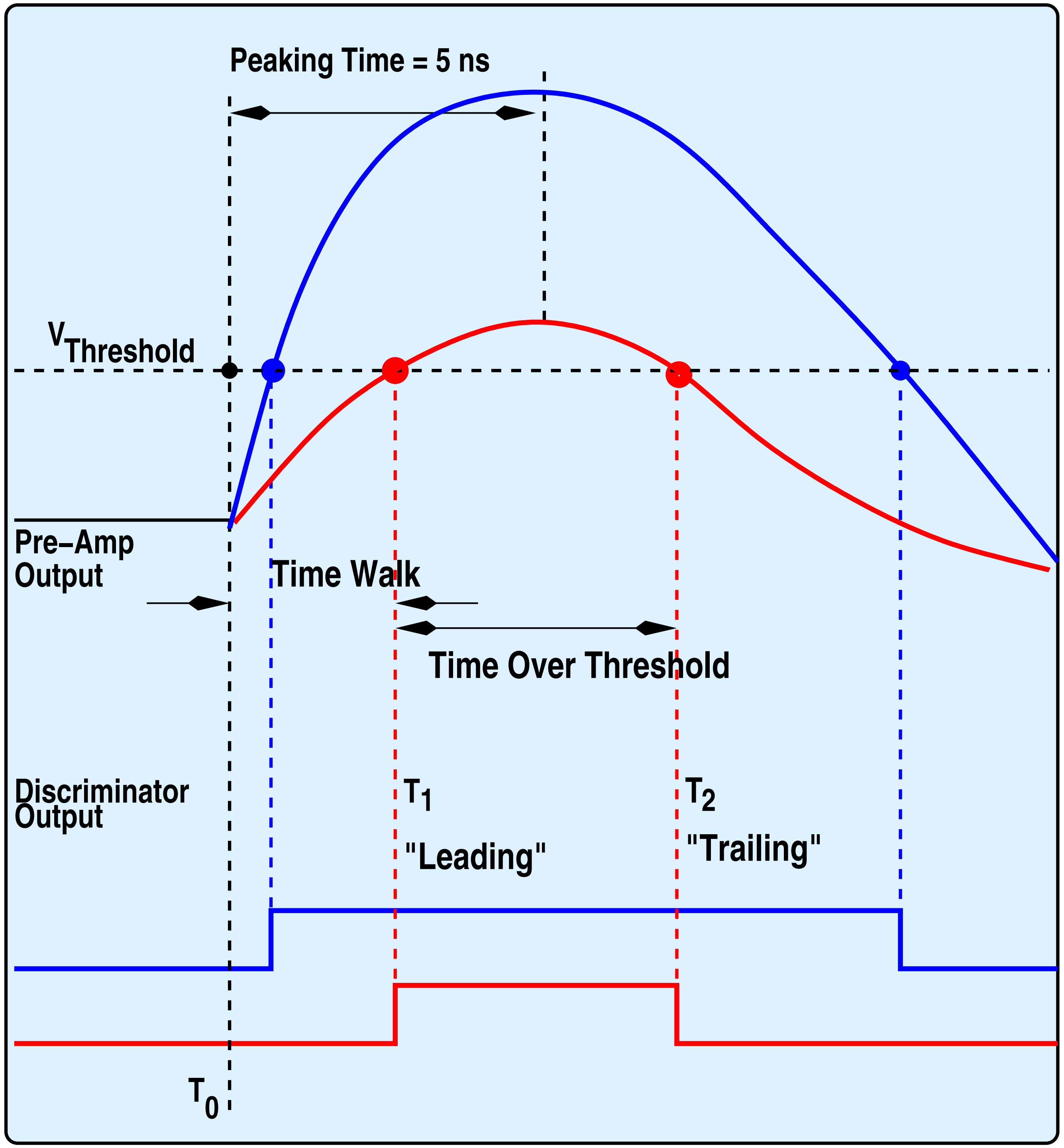


L0: **hw synchronous** level.
10 MHz to 1 MHz
Max latency 1 ms

L1: **sw level.**
"Single detector".
1 MHz to 100 kHz.
Max latency O(1s)

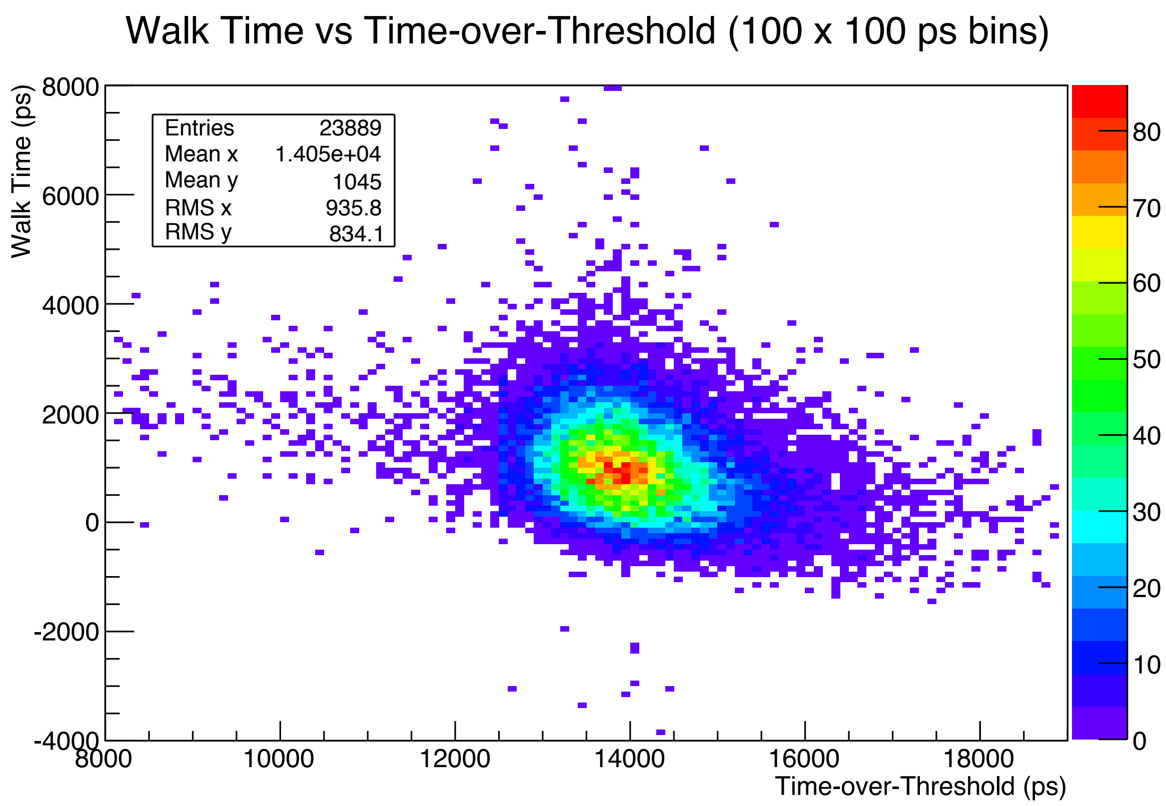
L2: **sw level.**
"Complete information".
100 kHz to 10 kHz.
Max latency O(30s)

Time-over-threshold - Time-walk correction

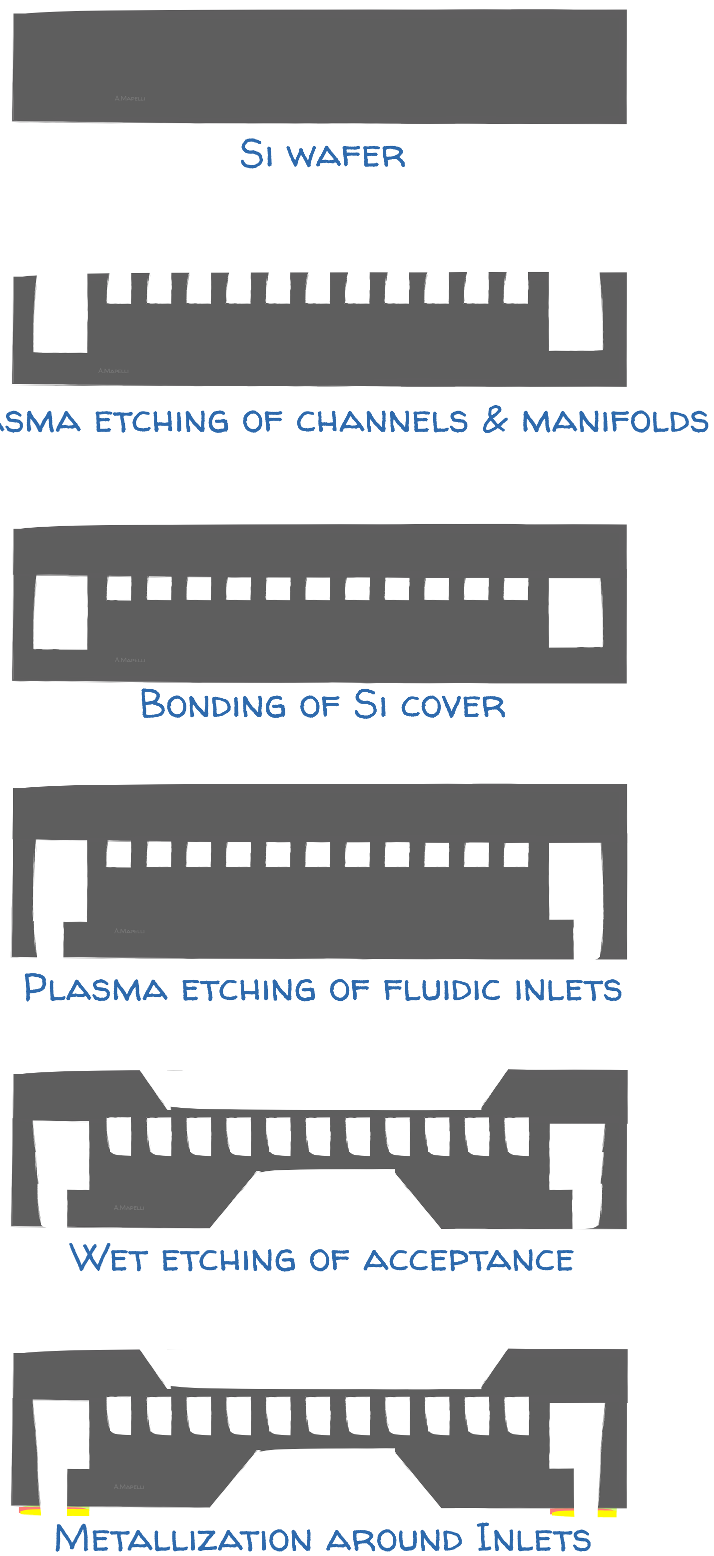


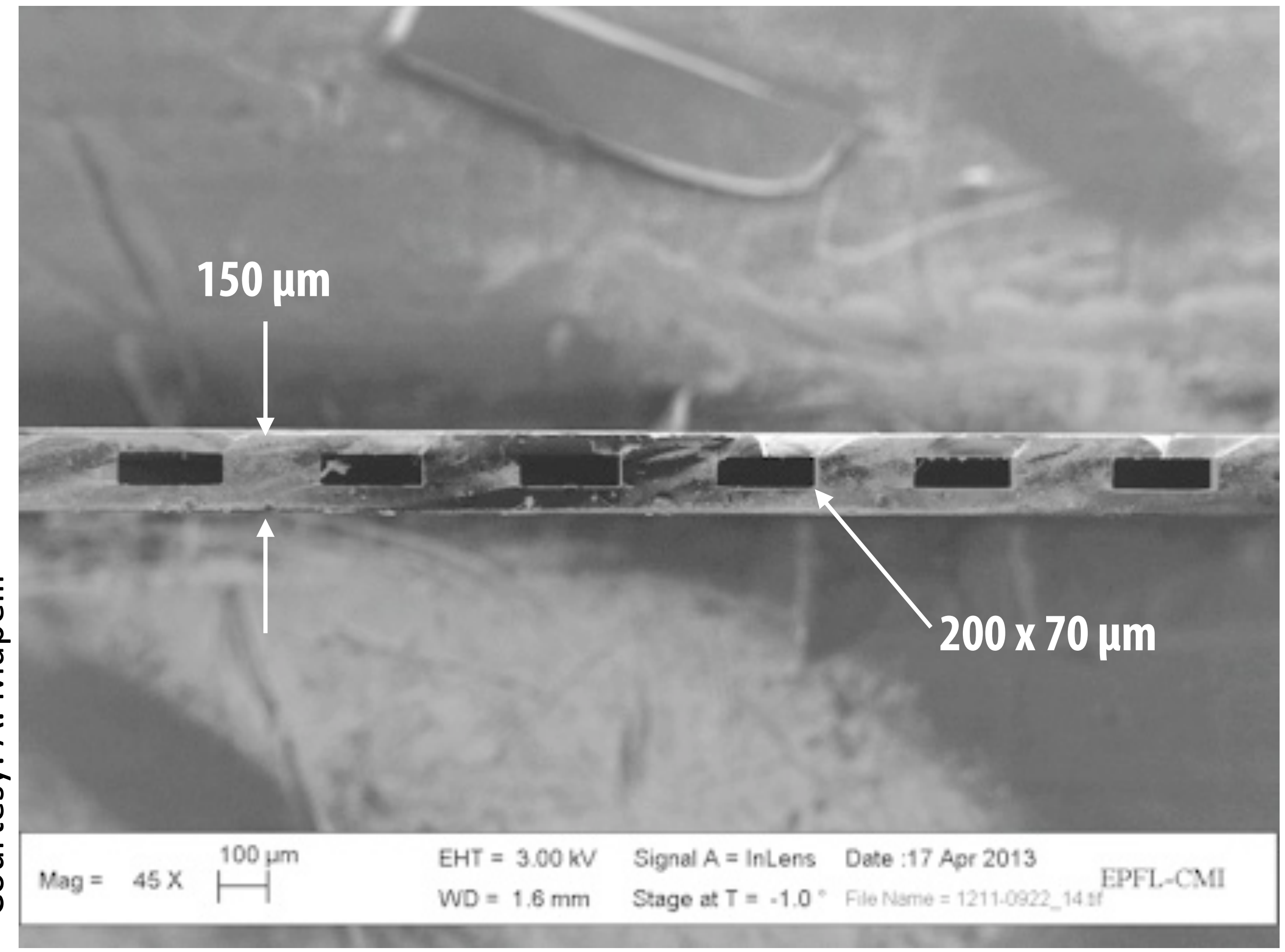
Time walk correction takes advantage of the relation between time walk and time-over-threshold.

Essential to meet the hit time resolution requirement



Microfabrication of the cooling plates





Courtesy: A. Mapelli

- Design by CERN PH_DT
- Fabricated by CEA-Leti on 8" wafers