Multiple Fast Controller Synchronization for ITER Control System Model

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Control Model infrastructure

4x network switches

Grandmaster clock

2x Hypervisors
with 70+ virtual servers

Storage server

Access point

2x PICMG casings
with 8 Fast Controllers

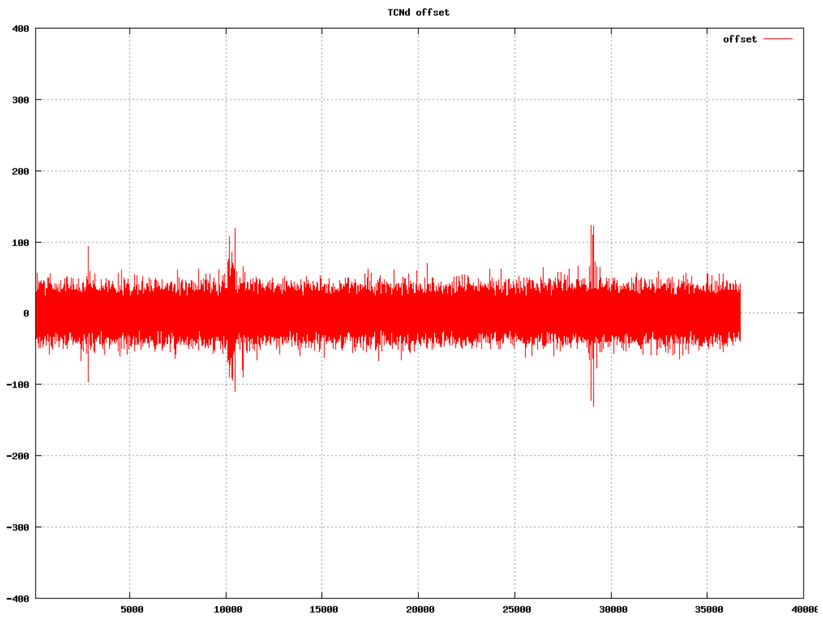
- Full-scale simulation of CODAC (ITER control system) without any physical I/O
- Standard server configuration and CODAC software
- Following all CODAC naming conventions
- Servers connected over physical networks and their dedicated switches to simulate real-world performance
- Fully automated deployment procedure without any manual configuration of individual servers

Real-Time infrastructure includes:

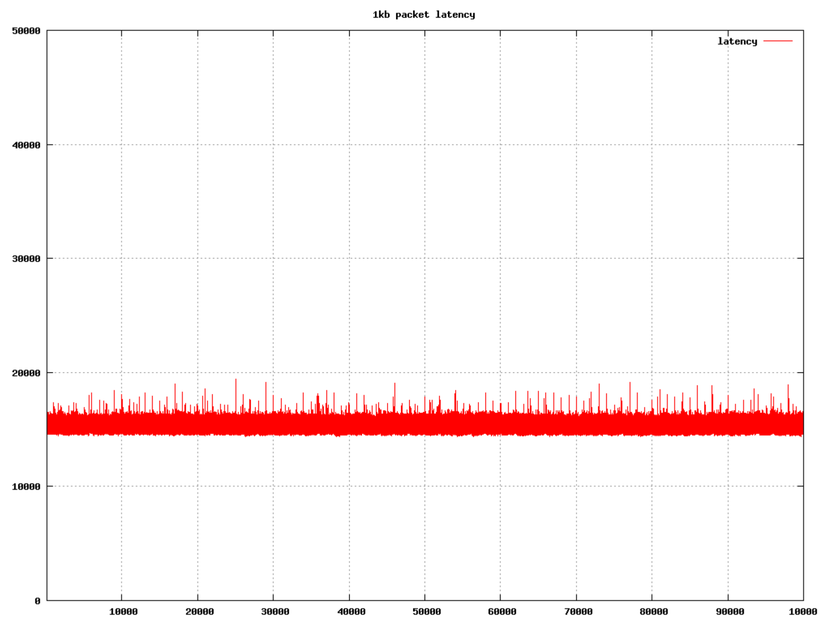
- 8x Fast Controllers (2x Xeon E3, 3x Xeon E5, 3x Core i7)
- 8x T420-CR Chelsio 10GbE network adapters
- Grandmaster clock and a dedicated switch using IEEE 1588-2008 standard over UDP/IP (synchronizing via PTPv2 protocol), which represent ITER Time Communication Network (TCN)
- Multicast capable cut-through high performance switch over UDP/IP for simulating ITER Synchronous Databus Network (SDN)

Real-Time configuration

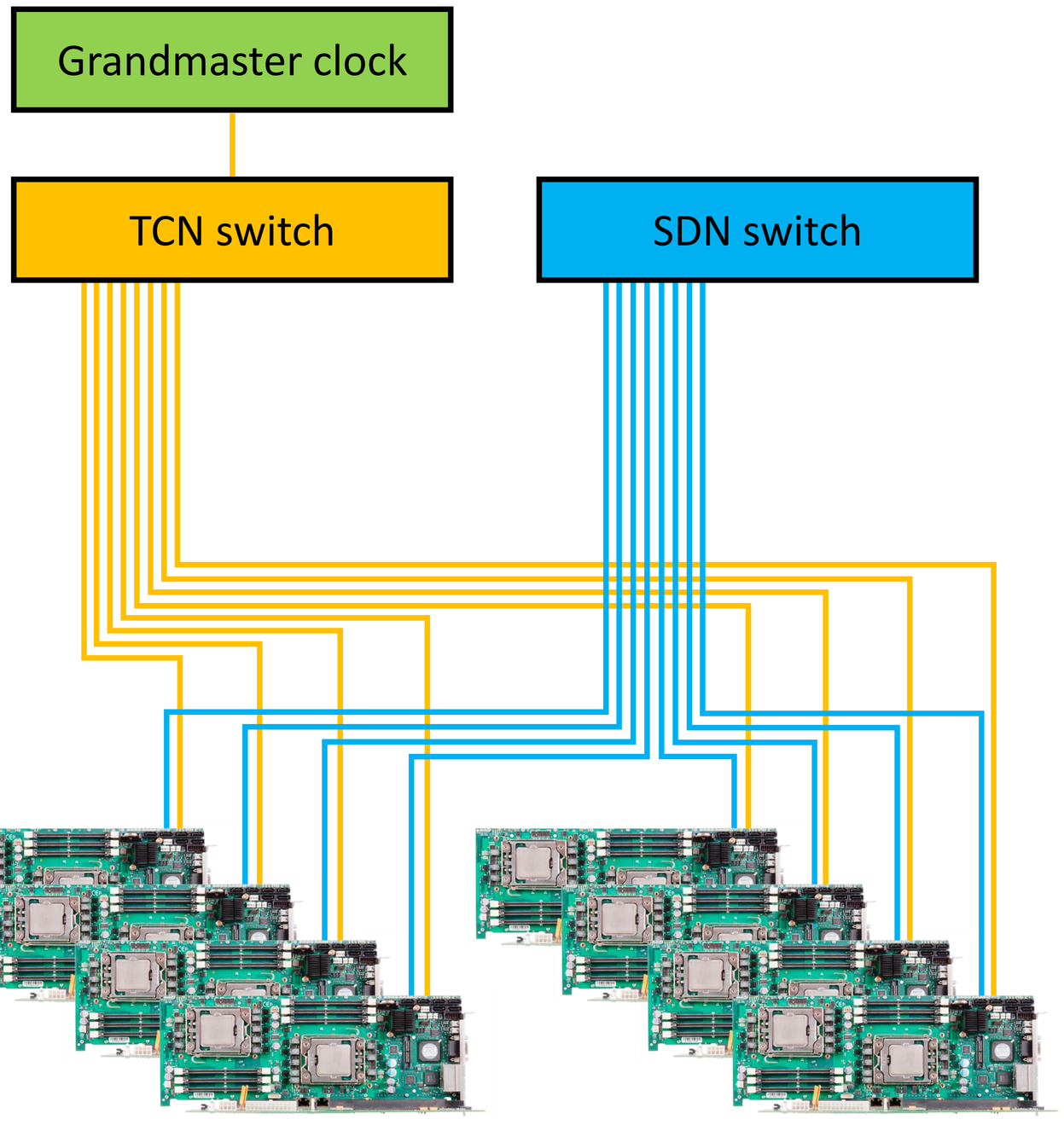
- System clock synchronization as low as 20 ns rms*



- 1KB packet transfer latency as low as 15 µs*



*optimization still in progress



- 2x Intel Xeon E3-1275
- 3x Intel Xeon E5-2428L
- 3x Intel Core i7-4790S

All paired with a 10 GbE T420-CR Chelsio adapter