Modular Software for MicroTCA.4 Based **Control Applications**.

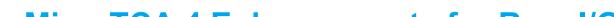
N. Shehzad, M. Killenberg, M. Heuer, M. Hierholzer, L. Petrosyan, C. Schmidt, T. Kozak, G. Varghese, M. Viti (DESY, Germany), S. Marsching (aquenos GmbH, Germany), M. Mehle, T. Sušnik, K. Žagar (Cosylab, Slovenia), A. Piotrowski (FastLogic, Poland), P. Prędki, J. Wychowaniak (Łódź University of Technology, Poland), A. Dworzanski, K. Czuba (Warsaw University of Technology, Poland)



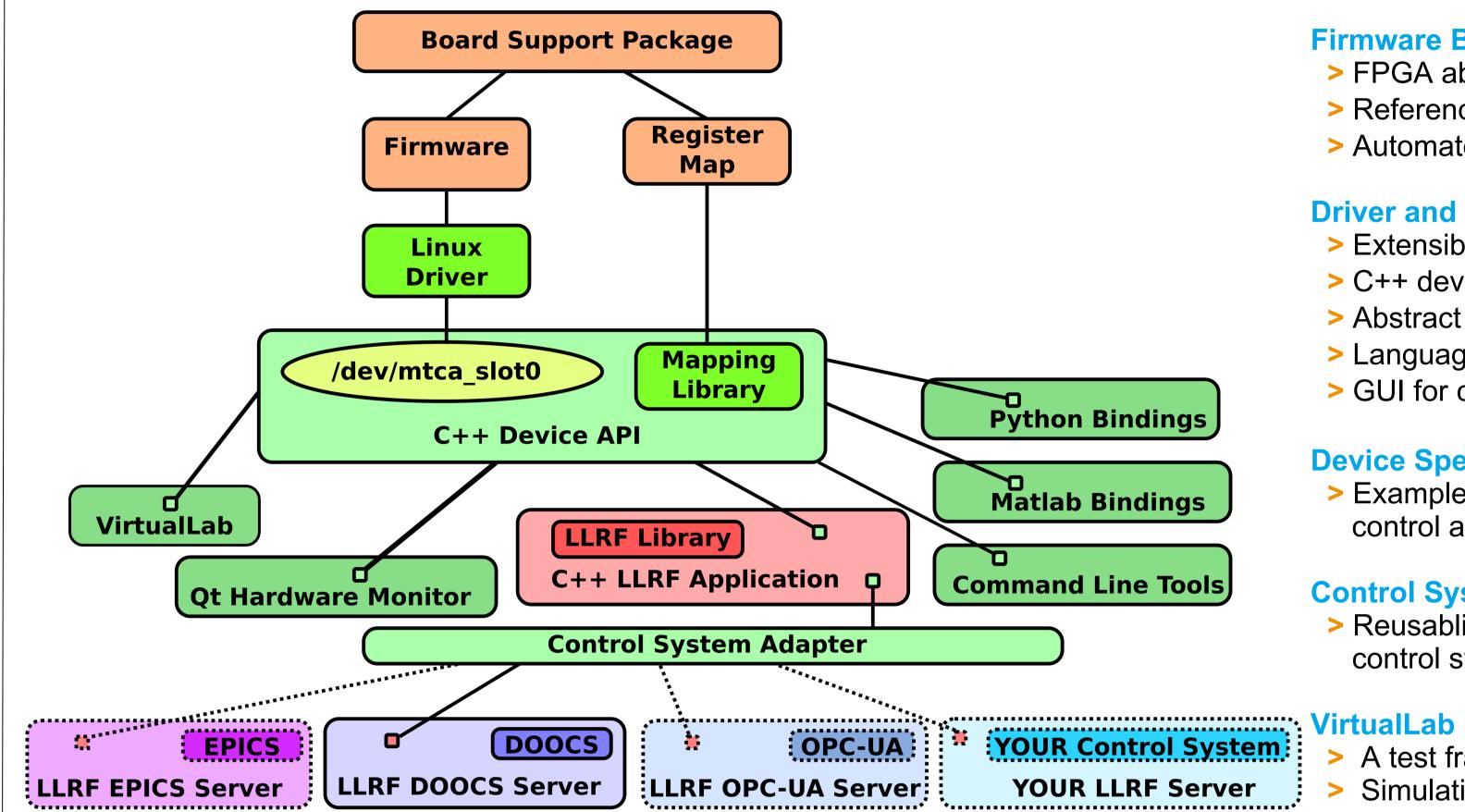
MicroTCA.4 Technology

Based on Advanced Telecommunications Computing Architecture (ATCA) Widespread use in telecommunications since 2005

- > High speed serial bus topology
- > High modularity due to Advanced Mezzanine Cards (AMCs)
- > High availability due to redundancy
- > Reduced down-time due to hot-swap capability



The DESY MicroTCA.4 User Tool Kit (MTCA4U)



Firmware Board Support Package

- > FPGA abstraction layer
- > Reference firmware with demo application code
- > Automated generation of register map

Driver and Basic Tools

- > Extensible universal driver
- > C++ device API
- > Abstract back-end interface
- Language bindings to Matlab and Python



- > Definition of Micro Rear Transition Modules (µRTMs)
- > Definition of AMC-µRTM connection
- > Radial clock lines for precision timing
- Low latency point to point serial I/O
- > Advanced shelf management
- > High signal integrity by separation of analog and digital processing

> GUI for convenient register monitoring/setting

Device Specific Applications

> Example: Low Level Radio Frequency (LLRF) control application for accelerators

Control System Adapter

> Reusablity of application code with multiple control systems

- A test framework to ensure software quality
- Simulation and testing without hardware

Use Case: Low Level Radio Frequency Control at the European XFEL and FLASH

- > Digital low level radio frequency (LLRF) control based on MicroTCA.4
- > Superconducting accelerators provide multi-GeV electron
- > Pulsed operation (10 Hz)



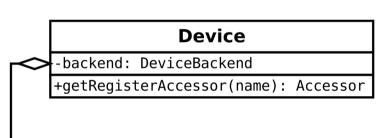
A MicroTCA.4 LLRF installation in the FLASH accelerator tunnel

MTCA4U → ChimeraTK

- > The tool kit has evolved to support devices beyond the scope of MicroTCA and MTCA4U has been renamed to ChimeraTK
- > All software is avialable under GNU General Public License or GNU Lesser General Public License
- > GitHub Repository: https://github.com/ChimeraTK.



The C++ Device API

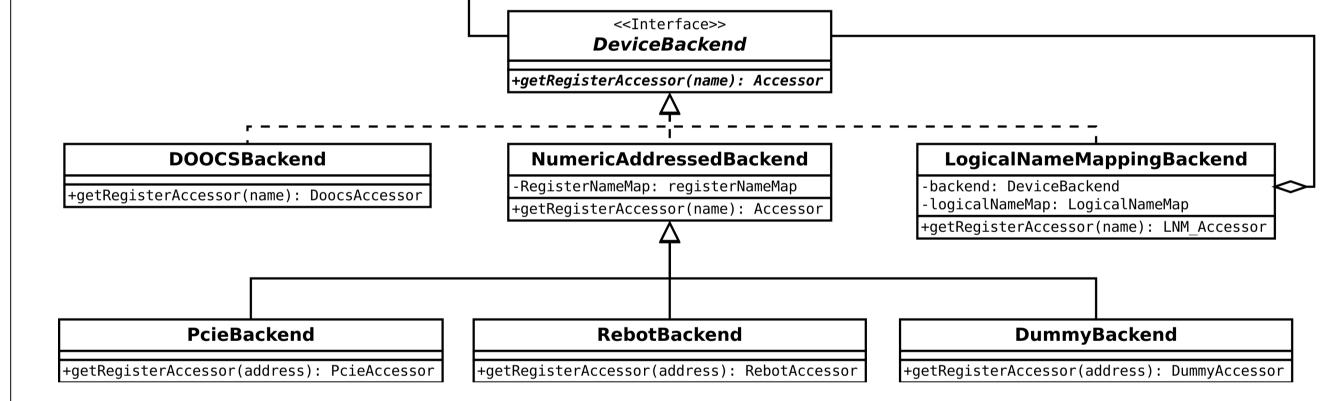


Register Name Mapping

> Access registers by name for NumericAddressedBackends

Qt Hardware Monitor

🛞 🖸 QtHardMon			
File Plugins Set	tings Help		
Devices:	Modules/Registers:	Register properties	Options
DUMMY1	→ BOARD WORD_FIRMWARE WORD_COMPILATION WORD_STATUS	Register name	□ Continuous read (250 ms)
DUMMY2			Read after write
DUMMY3		AREA_DMAABLE_FIXEDPOINT16_3	
DUMMY4		Module	Show plot window



DeviceBackend

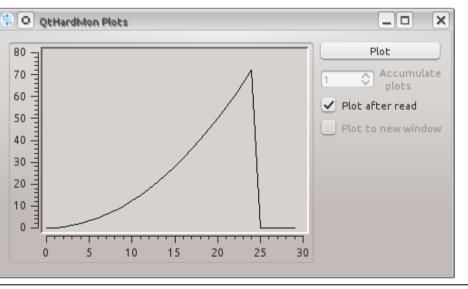
- > Abstract interface
- > PCI Express
- > Back-ends beyond MicroTCA.4 devices
- Register-based over TCP (ReboT)
- > Control system middleware access

Back-End Factory

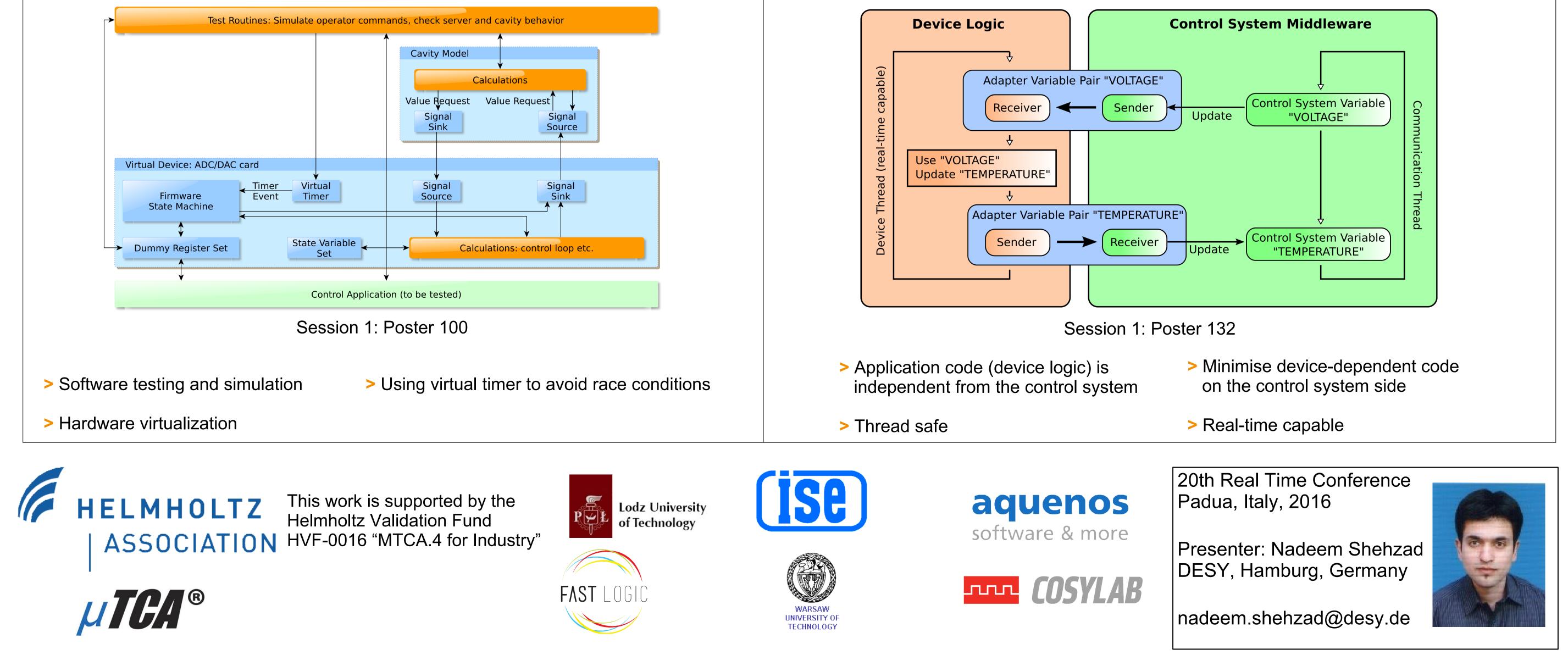
- > Automatically determine the back-end type
- > Plugin mechanism
- add new back-ends at run time
 - - ups

)ummy	/Backend
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- > Simulate I/O address space in RAM
- > Callback functions on read/write
 - implement firmware mock-
- DUMMY5 WORD_USER ADC Operations DUMMY6 ADC Register bar Fixed Point Interpreration WORD_CLK_CNT Read WORD_CLK_CNT_0 Register width Write Register address WORD_CLK_CNT_1 WORD_CLK_MUX Write to file **Fractional bits** WORD_CLK_MUX_0 Number of elements Read from file WORD CLK MUX 1 1024 WORD CLK MUX 2 Sign bit Total size WORD CLK MUX 3 WORD_CLK_DUMM Device status NORD_CLK_RST ∕alues Device is open. Close WORD ADC ENA raw (dec) araw (hex) double AREA DMAABLE 0.0000 0×0 Device properties AREA_DMA_VIA_DMA 0.1250 0x1 AREA_DMAABLE_FIXEDPOINT10_1 Device name 0.5000 AREA DMAABLE FIXEDPOINT16 3 0x4 DUMMY2 0x9 1.1250 TESTING Device file MOTOR 0x10 2.0000 /dev/mtcadummys1 WORD_SPI_WRITE 3.1250 0x19 WORD_SPI_READ Map file 0x24 4.5000 WORD_SPI_SYNC ./mtcadummy.map 0x31 6.1250 49 DESY 8.0000 0x40 Load Boards Autoselect previous register
- > Lists all hardware registers
- > Register names and properties
- > Read and modify register content
- > Basic plotting functionality



VirtualLab



Control System Adapter

