Upgrade of the TOTEM data acquisition system for the LHC's Run II

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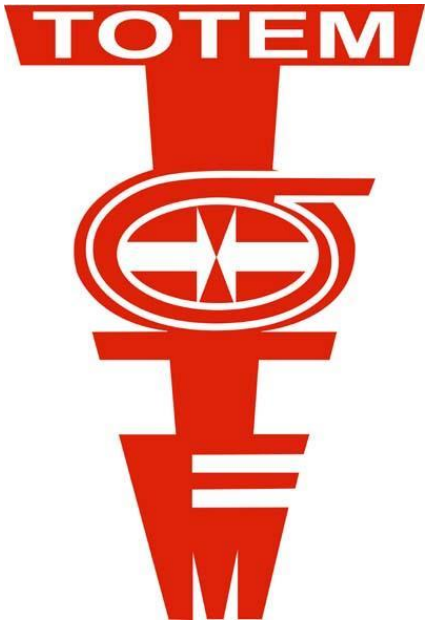
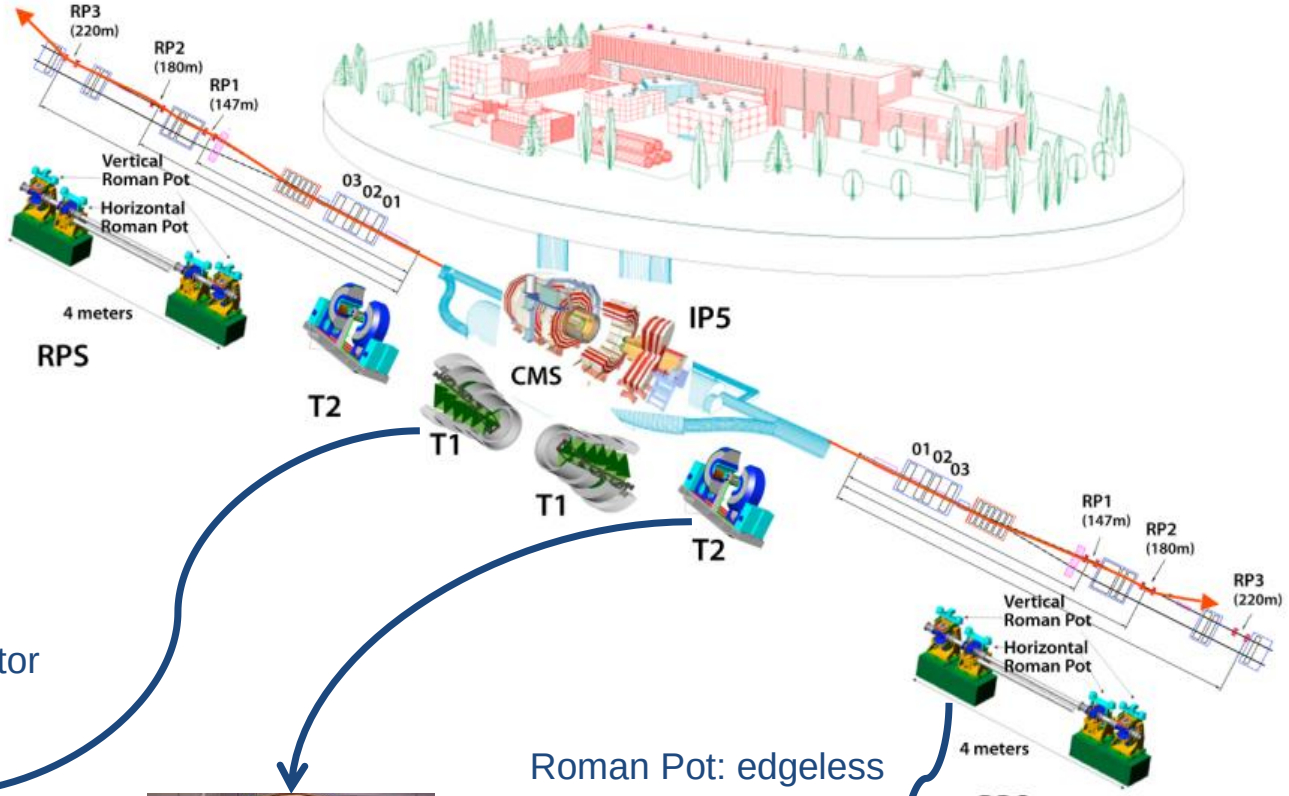


Contents

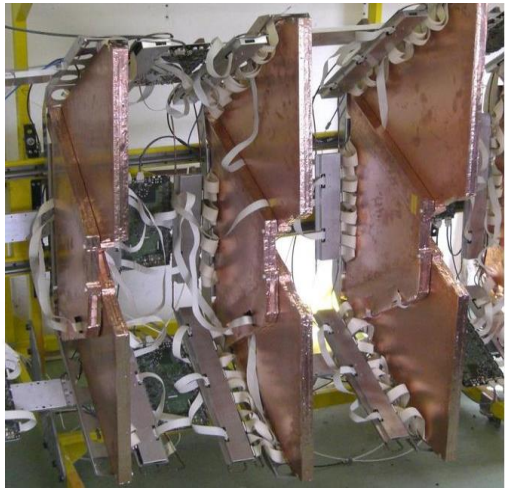
- The TOTEM Experiment at the LHC
- The TOTEM upgrade program for Run II
- The TOTEM DAQ system
  - The new DAQ system architecture
  - Firmware simulation environment
  - Online data processing
  - System operation and results
- Conclusions

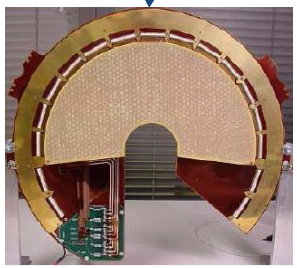
The TOTEM Experiment at the LHC

- TOTEM measures total p-p cross section at the LHC energies and studies diffractive processes.
- TOTEM adopts three detectors symmetrically placed at the Interaction Point 5 (T1, T2, Roman Pot).
- All TOTEM detector adopt common readout and trigger electronics. The VFAT chip provides readout and trigger capabilities.



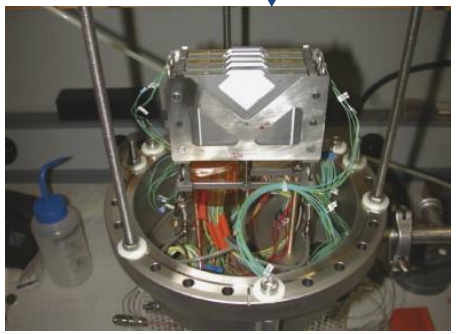
T1: Cathode Strip Chamber detector



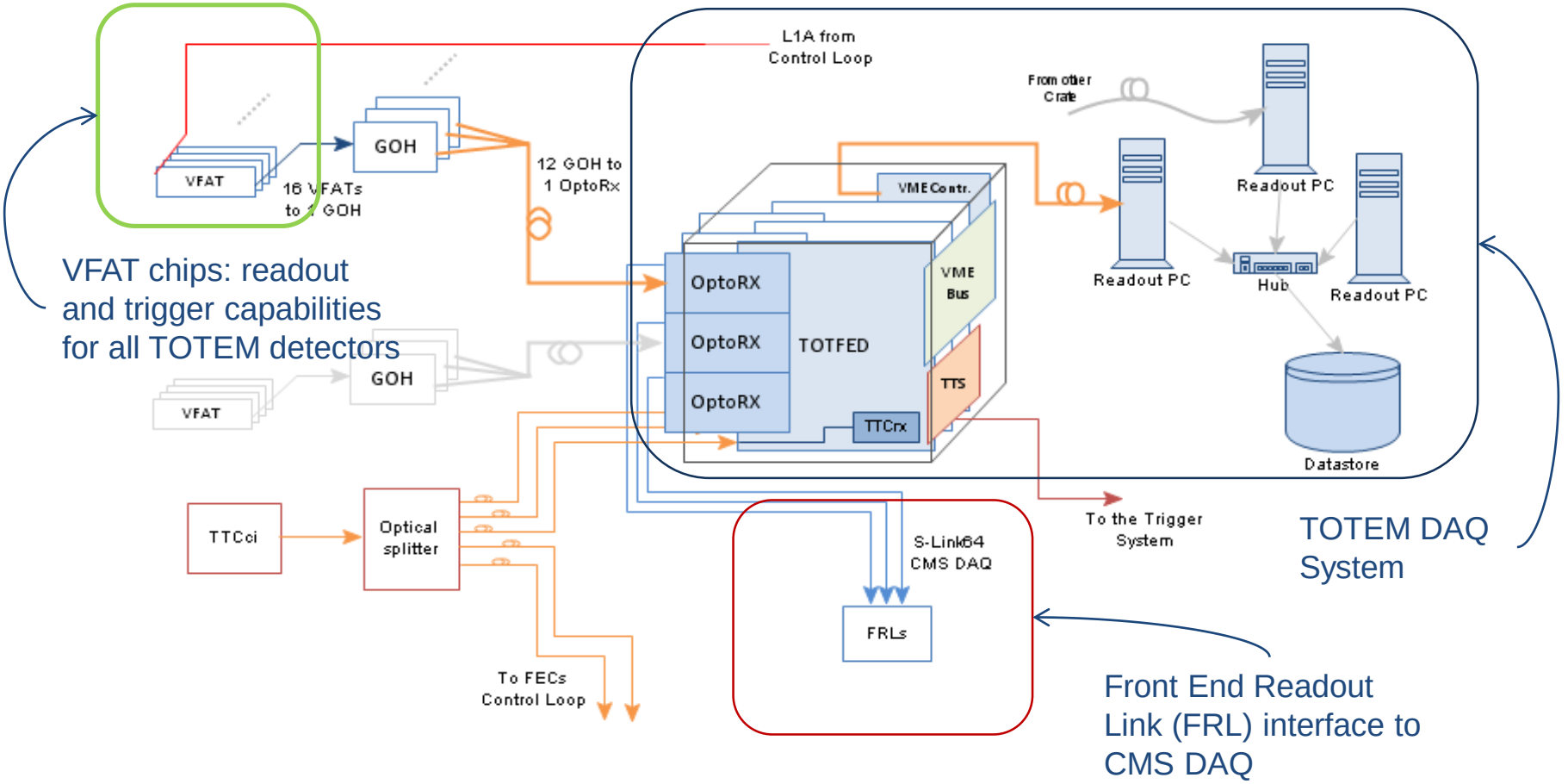


T2: triple GEM detector

Roman Pot: edgeless silicon detector



The TOTEM DAQ system architecture during Run I



VFAT chips: readout and trigger capabilities for all TOTEM detectors

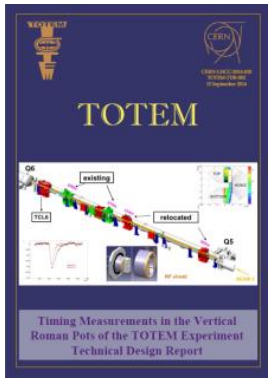
TOTEM DAQ System

Front End Readout Link (FRL) interface to CMS DAQ

- In the TOTEM standalone configuration, the VME bus bandwidth limits the trigger rate to 1kHz.

The TOTEM upgrade for Run II

- **Timing Measurements in the Vertical Roman Pots of the TOTEM Experiment**
  - **High beta* (90 m), special runs, low luminosity**
  - Integrated Luminosity of the order of 1-100 pb^{-1}
  - RP Strip detector complemented with timing detector
  - Common data taking with CMS
  - The DAQ system has to cope with up to 100kHz trigger rate either in stand alone configuration or fully integrated with CMS -> **the DAQ system needs to be upgraded**



- **Scientific objectives**:
  - Exclusive central diffraction
  - Low mass resonances and glueball states
  - Exclusive charmonium state
  - Search for missing mass and momentum candidates
  - Exclusive jet production

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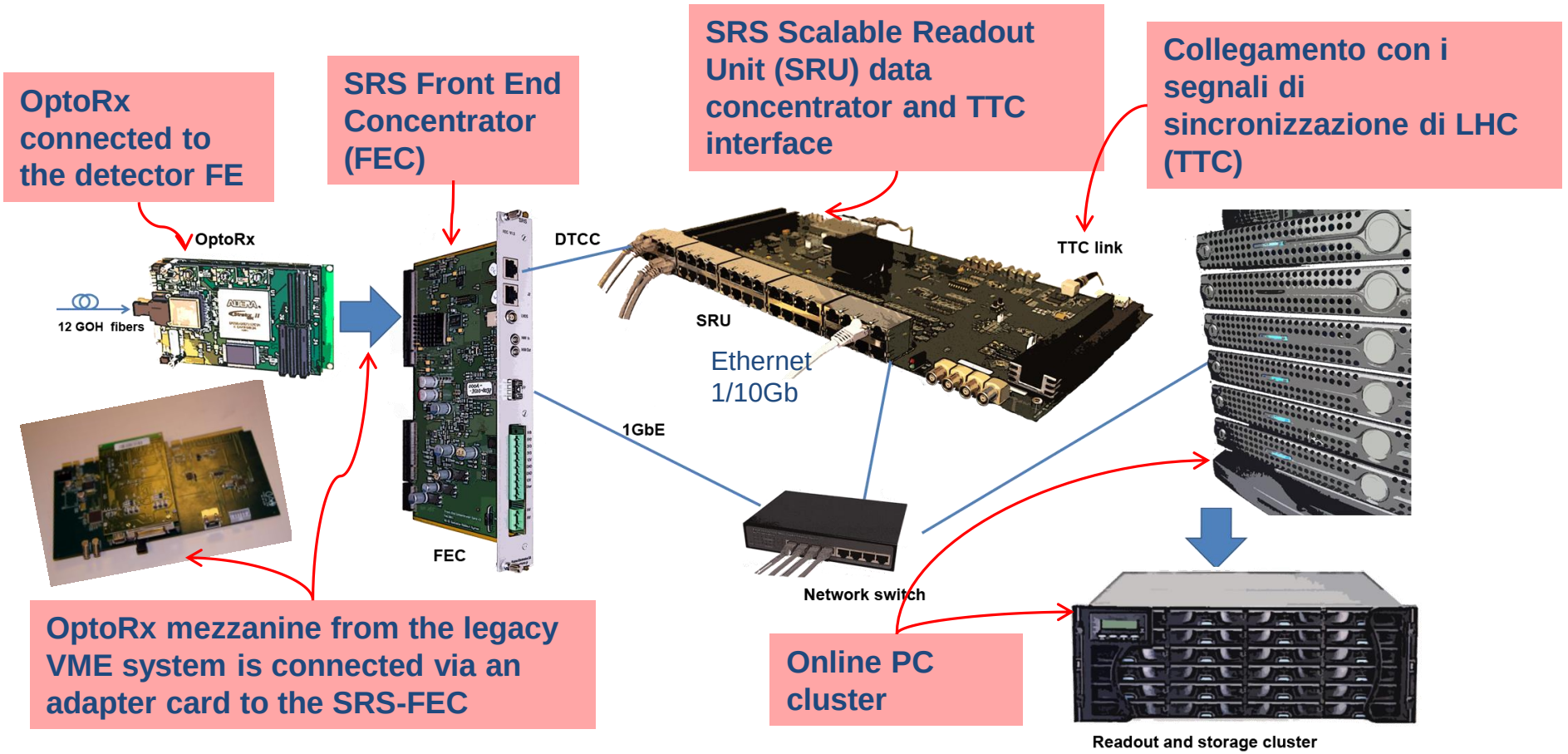
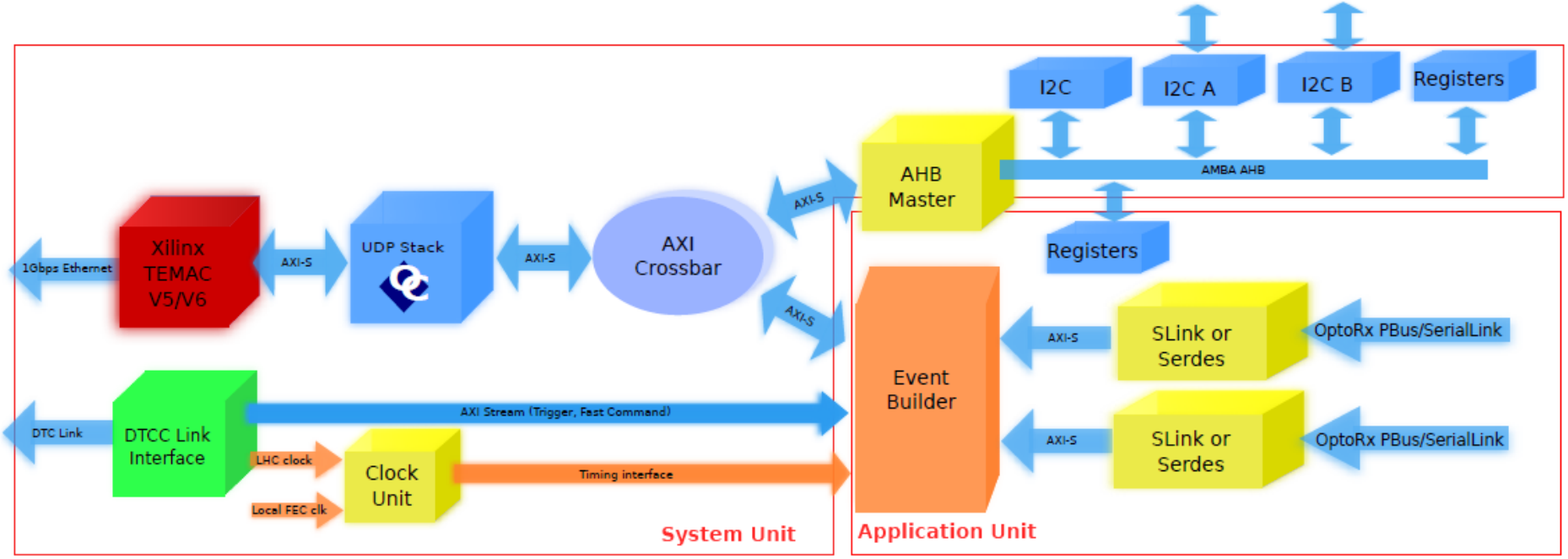
The new DAQ system architecture



- Based on the SRS platform developed in the RD51 community
- Improved system scalability
- Improved data throughput 120MB/s per OptoRx w.r.t. ~10MB/s on VME bus
- FPGA resources available at different levels to implement data processing

Firmware architecture desing



- Mixed language design VHDL, Verilog and SystemVerilog adopted for synthesis
- Standard interconnection bus used AXI Stream AMBA-AHB
- Standard interfaces such as I2C, Ethernet are based on open source cores customized ad-hoc
- Separation in two blocks:
  - System Unit: services and connectivity
  - Application Unit: user algos

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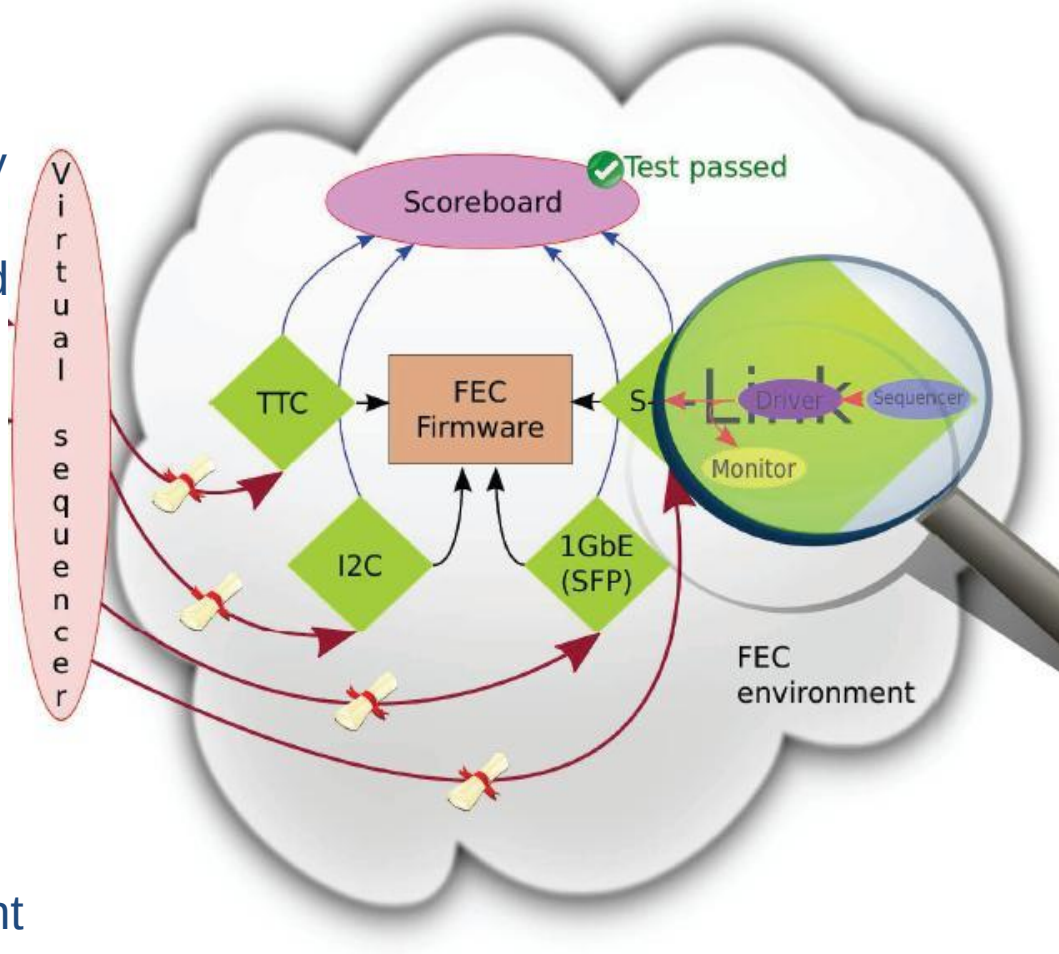
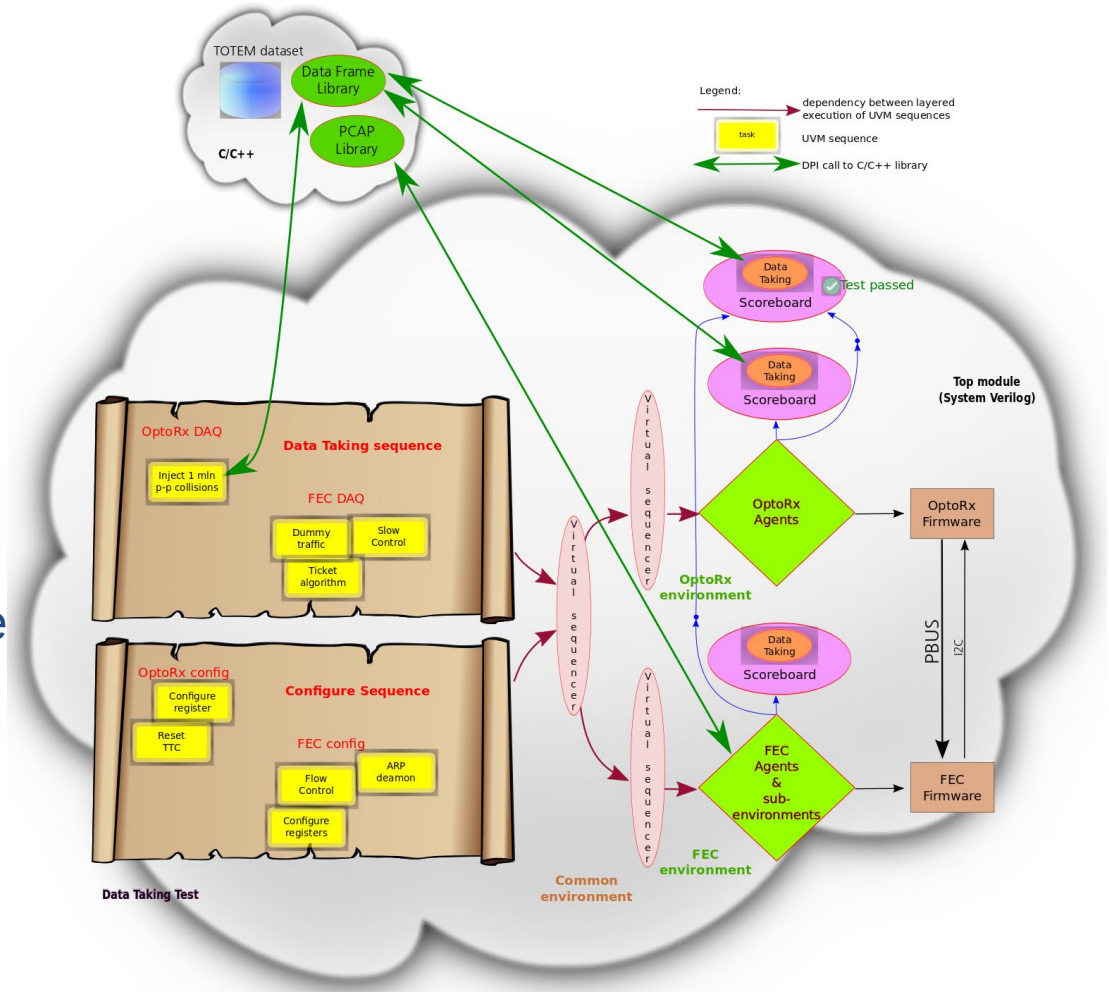
Simulation environment

- SystemVerilog simulations have been implemented to verify the full firmware design
- Universal Verification Methodology UVM is exploited
- Each bus or interface is driven and monitored:
  - Verification IP (VIP) from Mentor Graphics are used for standard interface (Ethernet, I2C)
  - Custom IPs have been developed for custom interfaces (SLink)
- Simulation follows verification plans, dedicated tests are integrated in the same environment



Simulation environment

- SystemVerilog OO and UVM allow to model and simulate very large system
- Combined simulation with multiple Device Under Tests (DUTs) is possible
- DPI library are used to interface with the offline libraries written in C++
- Physics data can be injected into the test bench to emulate the data stream from the real detector



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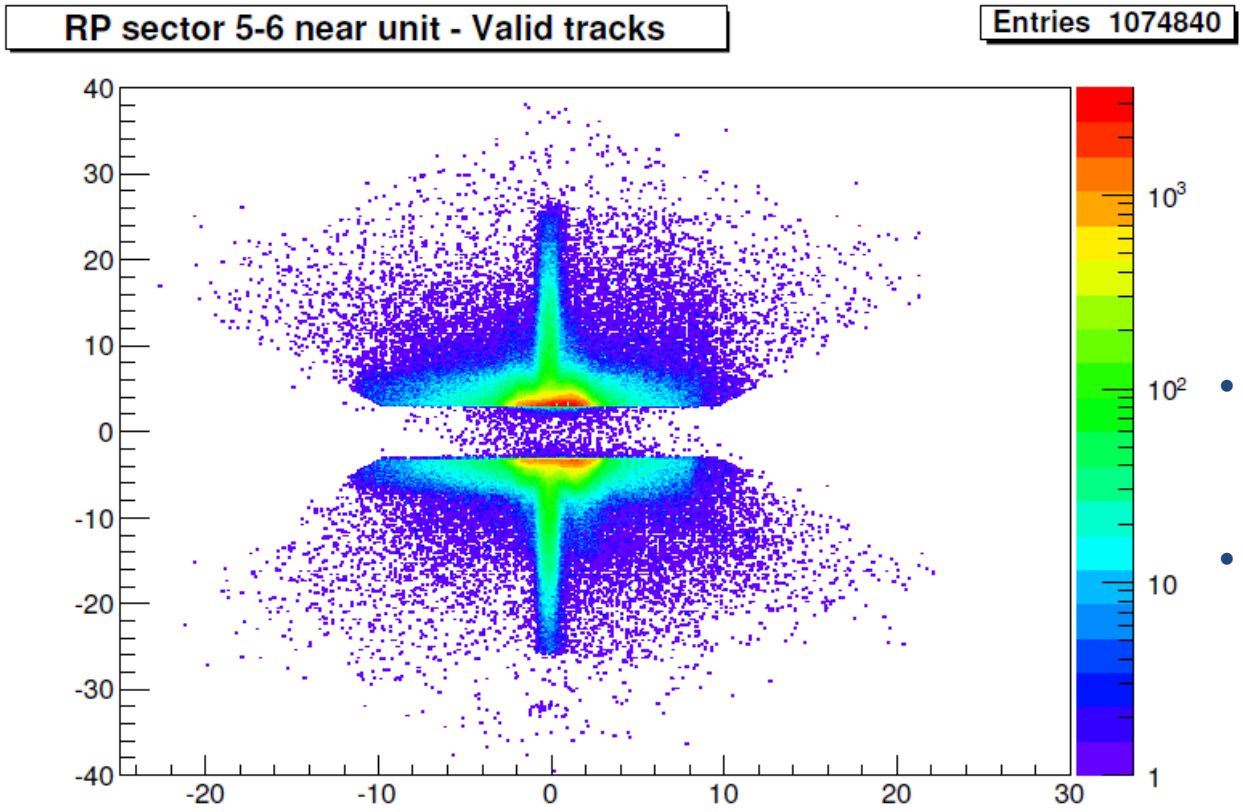
Event topology at the Roman Pot

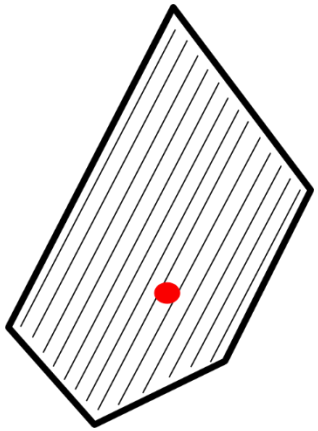


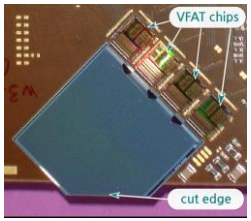
TOTEM data from special runs (Run I)

- Track hits reconstructed by the off-line algorithms
- Only 30% of the total number of events has a track candidate

Off-line event reconstruction

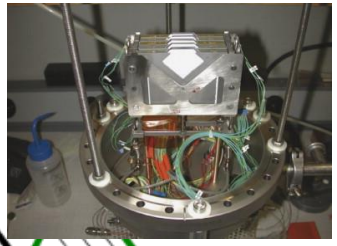
Step 1: Cluster recontruction by grouping firing neighbour strips





Step 1: reduces data size up to 20%

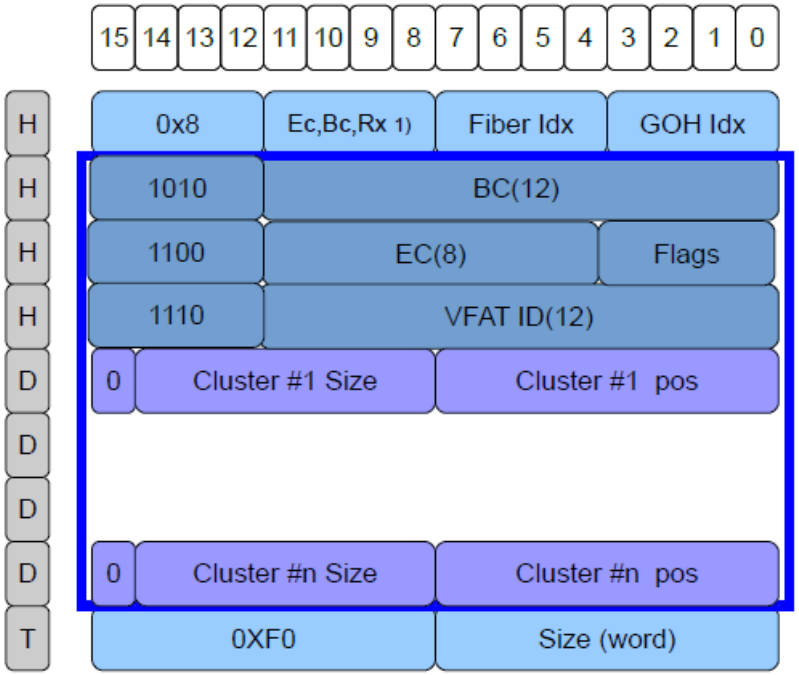
Step 2: Reconstruct e track segment within the detectors planes



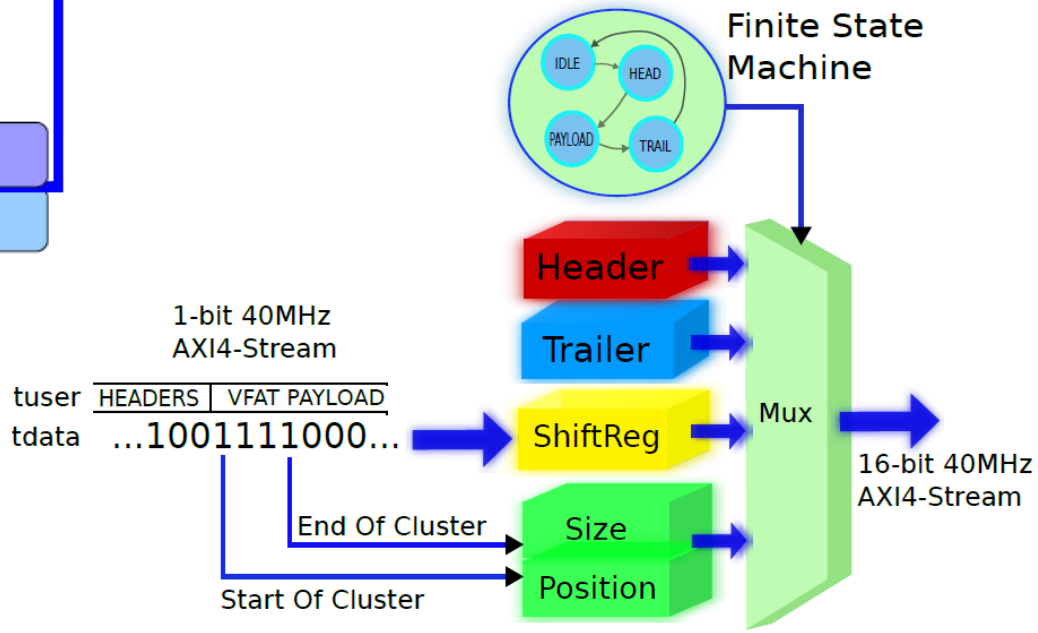
Step 2: on-line tracking allows 2nd level trigger

Much higher rates can be achieved by moving part of the off-line data processing into the on-line domain

Cluster reconstruction



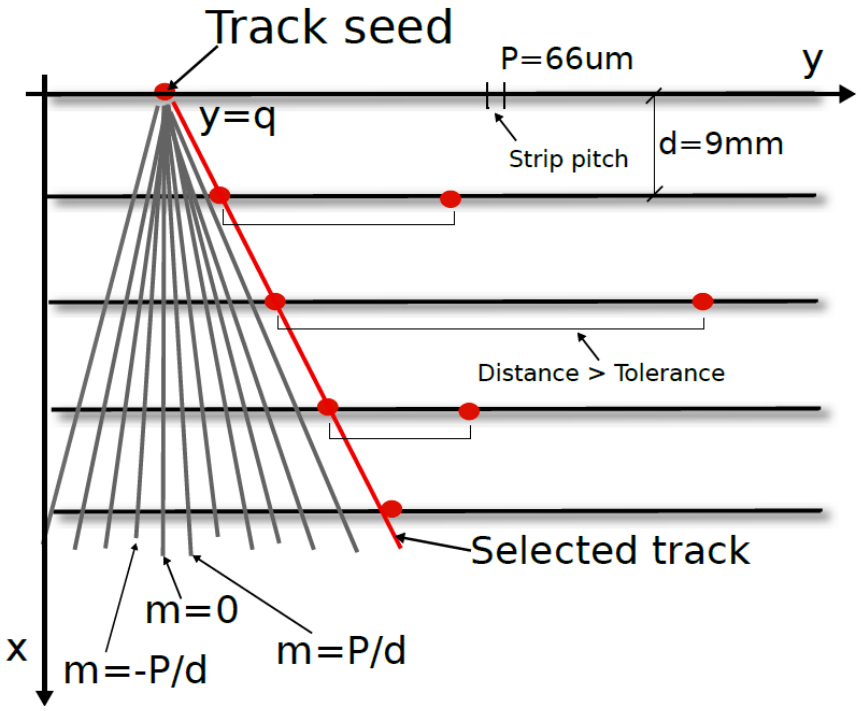
The hits registered by the detector are trasformed into clusters

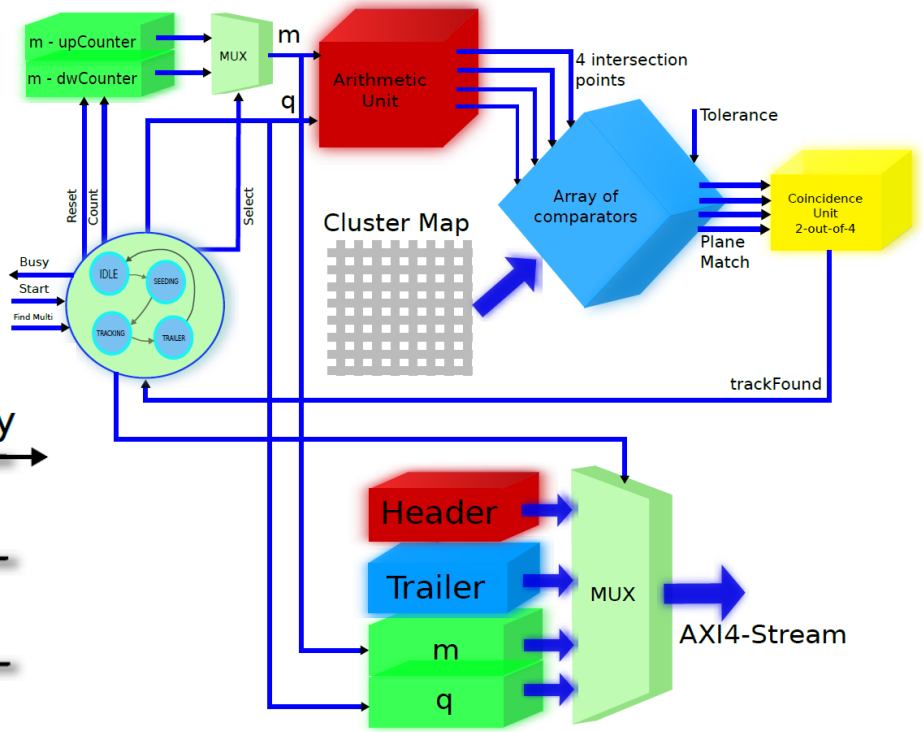


Event size is reduced up to a factor 5

On-line tracking

Algorithm based on track *template matching*
Simple implementation with two parameters:
- ✓ **Max slope**
- ✓ **Tolerance**





Second level trigger possible in hardware merging data from several Roman Pot

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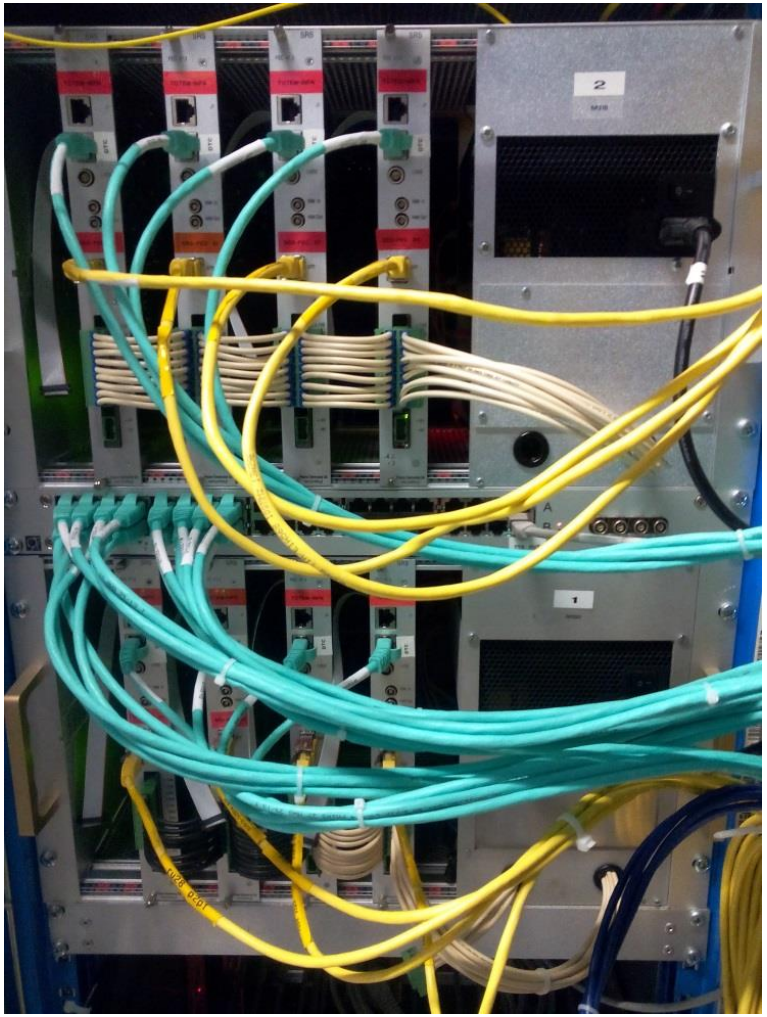
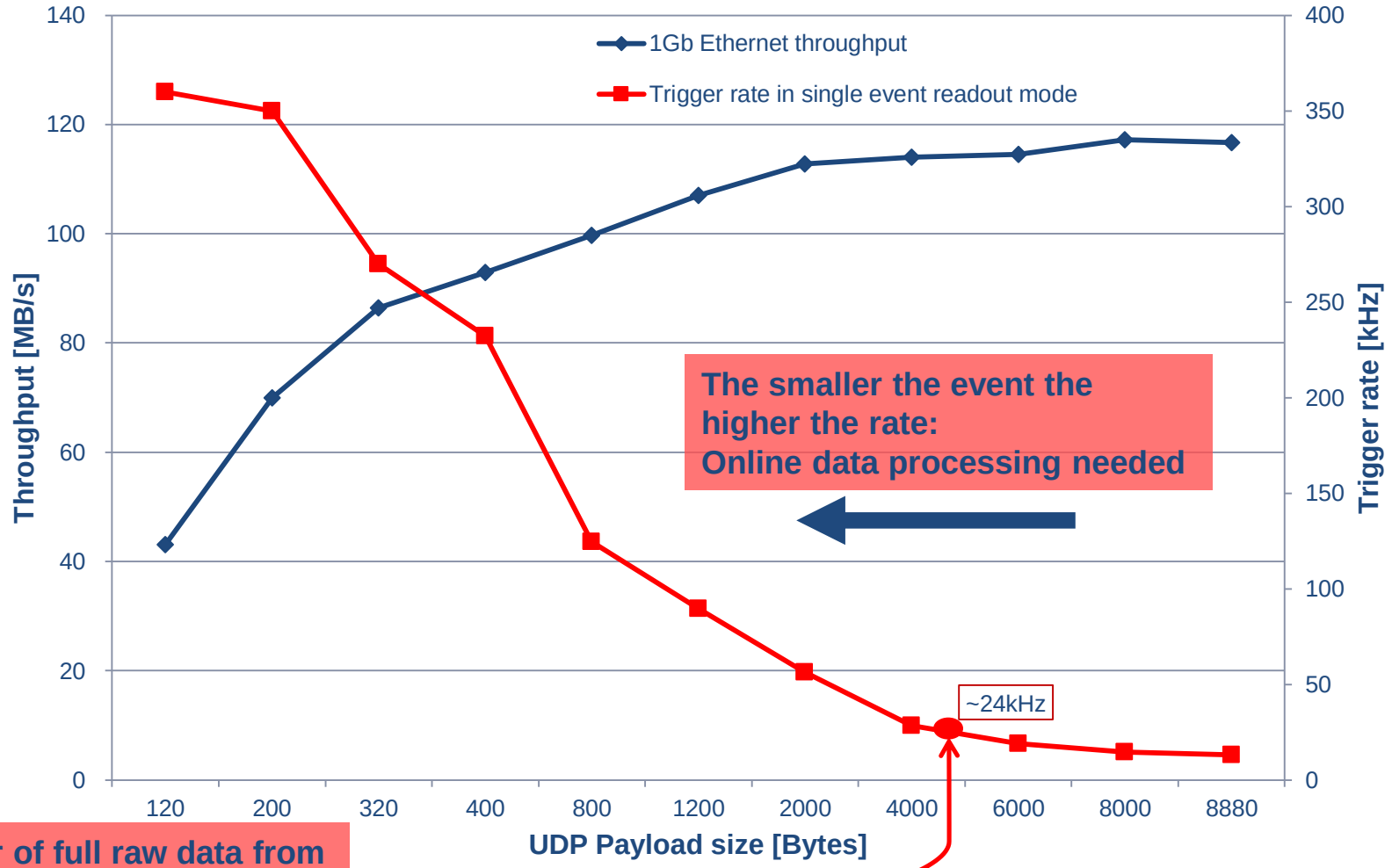
System installation at P5

- 16 SRS-FEC + OptoRx deployed to readout all TOTEM detectors
- 2GB/s data flow on 1Gb/10Gb Ethernet network
- Full data throughput stored to disk
- ~400TB storage available on site, enough for special run campaigns



System performance



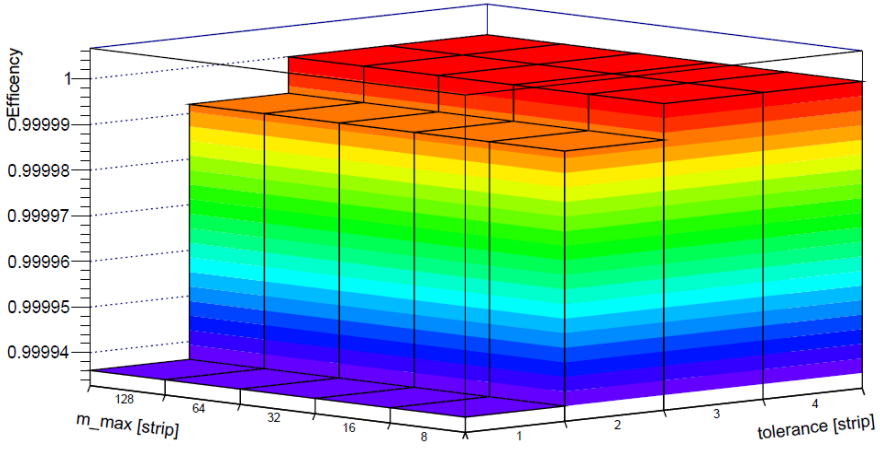
Transfer of full raw data from three RP detector connected to an OptoRx ~5kB/event

System performance

- Raw transfer mode is limited by the 1Gb Ethernet bandwidth
- Cluster mode exploits cluster reconstruction

Mode	Trigger rate
Raw	24kHz
Cluster	70kHz

Preformance achieved during 2015' special runs



- On-line tracking offers the prospect to exploit online 2nd level trigger
- The algorithm in hardware shows a good efficiency w.r.t. the off-line algorithms

Conclusions

- The new TOTEM data acquisition system has been installed and commissioned during the Long Shut Down 1
- Novel FPGA design and verification techniques exploited:
  - SystemVerilog
  - Full UVM simulation injecting real Physics data
- The system has been operated smoothly during the 2015 high beta special runs
- Collected luminosity improved by up to two order of magnitude

Thank you for your attention!