Readout electronics and data acquisition for gaseous tracking detectors

M. Idzik, G. Korcyl, D. Przyborowski, P. Salabura, J. Smyrski, P. Strzempek

Abstract– A complete solution for collecting and processing data from gaseous tracking detectors has been developed. The readout chain consists of Front-End Modules (FEM) equipped with PASTTREC2 ASIC chips and Trigger Readout Board v3 (TRBv3) as a readout platform, together with control and monitoring mechanisms and data quality assessment software.

The entire system has been evaluated in the laboratory as well as in-beam experiments. The results show drift time measurement and Time-over-Threshold time precision measurement below 1 ns and a high counting rate performance per channel. Measured PASTTREC2 operation characteristics as well as the TRBv3 platform used for readout allow to adapt and integrate the system under discussion to the existing HADES spectrometer and the PANDA detector, an experiment under construction, both located at FAIR facility in Darmstadt.

I. Introduction

Charged particle passing through a gaseous detector ionizes gas leading to production of clusters of electrons and ions. The electrons drift in applied electric field towards the anode wire and in the strong field close to the anode they are multiplied giving rise to creation of a large number of electron-ion pairs. Movement of positive ions towards the cathode gives the main contribution to creation of a detector signal. Consequently, this signal has a long tail extending to several hundreds of microseconds.

The presence of the tail can lead to pile-up of several pulses spoiling the time and amplitude measurement of the pulses. Therefore, for applications of gaseous detectors in high rate experiments, a critical issue for the read-out electronics is a perfect cancelation of the ion tail.

In the gaseous drift detectors like the straw detectors, measurement of the drift time of electrons to the anode wire is used for determination of a track distance to the wire. In turns measurement of an amplitude or a Time-over-Threshold (TOT) of the detector signals, can be used for determination of ionization which is commonly applied for the particle identification. The drift time measurement as well as TOT measurement require a time resolution of about 1 ns.

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II. General system overview

The presented readout system (Fig. 1) is a complete, stand-alone data acquisition chain consisting of Front-End Modules (FEM) [1], Trigger Readout Board version 3 (TRBv3) [2] boards serving as digitizers and a readout platform together with a software framework for the control and the monitoring as well as data analysis and track reconstruction.

The FEMs are connected to the detector anode either directly or, in case there is a high voltage potential applied, via an additional, passive RC board, equipped with resistors for limiting the wire current and capacitors for the voltage decoupling. The digital outputs of FEM are driven in LVDS standard through twisted-pair cables to the digitizing boards, that is the TRBv3 platform.

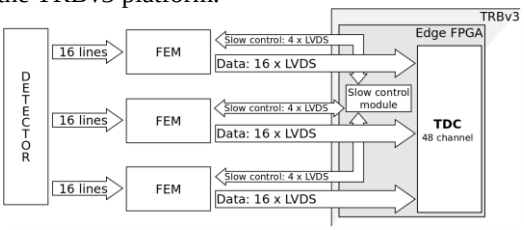

Fig. 1. Schematic view of the readout system.

The TRBv3 platform is a set of hardware, firmware and software for acquisition and processing of digital data. The entire system can be composed of a single or multiple nodes by interconnecting base boards together. Such approach assures scalability of the system and allows to introduce additional modules at any time, whenever there is need for augmenting the number of input channels or introduce new processing capabilities.

The data collected by the TRBv3 system is transferred to storage and offline analysis by Gigabit Ethernet links and UDP-based protocols, therefore it can be connected to almost any standard network infrastructure or even a single PC.

III. Front-End Electronics

FEM is based on PASTTREC2 chip [3], which is a highly-configurable shaping and discriminating ASIC, developed especially for drift chambers operating with high rates and therefore requiring fast shaping with tail cancellation. Single chip has 8 independent channels on analog part and a shared digital part for slow control.

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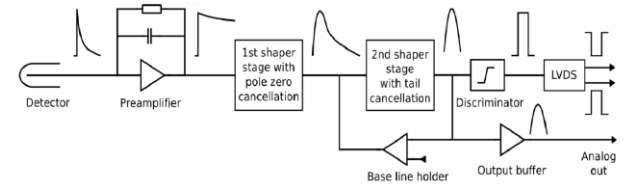

Fig. 2. Schematic view of the PASTTREC2 architecture.

PASTTREC2 consist of is a chain of circuits (Fig. 2) responsible for signal shaping. First one is the charge sensitive preamplifier with a configurable gain which is realized with a feedback capacitance. Amplified signal enters a first stage shaper (CR-RC circuit) which works together with a Pole Zero Cancellation (PZC) for the reduction of the undershoot introduced by the shaping stage. The first stage shaper defines the peaking time and is configurable as well, providing 4 values in the range of 15 to 40 ns for the input delta pulse. A dedicated tail cancellation circuit is introduced, which together with a 2nd stage shaper, can efficiently trim the tail of the signal. The parameters of the 2nd stage shaper can also be configured to adapt to various signal shapes.

For applications requiring Time-over-Threshold, where the threshold has to be precisely applied at the same level, a baseline holder loop has been applied with an additional, individual for each channel, DACs for fine-tuning.

Shaped by all of the elements described above, signals are discriminated by the application of a common threshold level to all 8 channels. The outputs are driven by LVDS transmitters out of the Front-End module.

Single PCB board, equipped with two such chips, provides a total of 16 input channels through a pin header connector. Digital, differential signals are transmitted through the KEL 8930E 40-pin connector which provides additional lines for the slow control (4 LVDS pairs). Two additional MMCX connectors are used for test and calibration purposes. Test signals can be injected via these connectors through PASTTREC2 internal capacitors directly at the inputs of the charge sensitive preamplifiers.

Configuration of all the parameters available in the PASTTREC2 chips is realized through the serial SPI interface, which uses available LVDS lines in the same connector as the discriminator outputs.

IV. Digitizing and Readout Platform

The TRBv3 system is composed out of base boards, each having 5 FPGA devices. One FPGA device is the controller and four can be configured with various firmware as TDC [4], data concentrators or any other data providers.

On logical level [5], the system consists of endpoints and hubs. The endpoints are data sources and the hubs concentrate data streams from several endpoints. The system is arranged in a tree-like, hierarchical architecture, therefore one hub from lower layer is treated as an endpoint for a higher layer hub. Such approach assures scalability and allows to construct large setups out of the interconnected base modules. Flexibility in the configuration is given by the fact that the functionality is provided by the firmware. One FPGA device can be configured as a hub in case one needs to extend the number of endpoints or as a digitizer and a data source, which is a terminal endpoint.

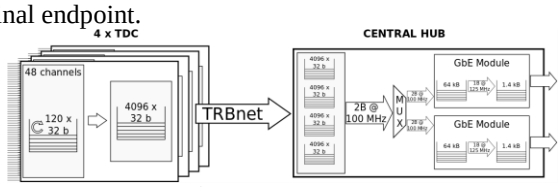

Fig. 3. Block diagram of the TRBv3 base module with TDC endpoints.

The communication in the system employs two types of protocols. A dedicated TrbNet [6] protocol, which is a core component of the TRBv3 platform as a system, is used for internal data exchange between modules. Its significant feature is the sharing of one physical link between three logical channels: distribution of readout requests with deterministic latency, readout data stream and slow control. Data from the endpoints collected by the hubs exits the system via Gigabit Ethernet links in the form of UDP packets, sent through standard networks to PCs. Synchronization of the system is realized twofold: precise time synchronization through dedicated reference time distribution to the TDC and event synchronization via readout request messages.

V. System Evaluation and Conclusions

The readout system has been tested on a straw tube tracking detector prototype under proton beam provided by the COSY at Juelich facility. The 96 straws, organized in 3 double layers were read out by 6 Front-End Modules and a single TRBv3. The resolution of the system in terms of position and energy loss have been determined a full track reconstruction. The obtained TOT resolution (Fig. 4) amounts to 5.6%, 5.3%, 7% and 10.1% for the beam momenta: 3 GeV/c, 1 GeV/c, 750 MeV/c and 550 MeV/c respectively. The spatial resolution (Fig. 4) amounts to 156 µm.

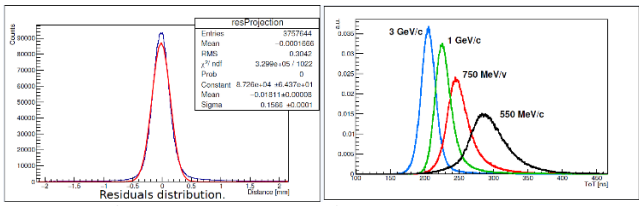

Fig. 4. Left: Residual distribution of reconstructed tracks recorded with straw tube detector. Right: Mean TOT value for different beam momenta

Investigations of the system readout performance show accepted hit rate per channel at level of 56 kHz with 1.5 kHz readout request rate. Those values (Fig. 5) are derived from TRBv3 internal communication and buffering mechanisms which guarantee no data loss.

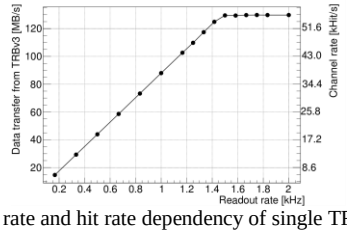

Fig. 5. Data rate and hit rate dependency of single TRBv3 module

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REFERENCES

[1] P. Strzempek et al. “PANDA Straw Tube Detectors and Readout”, Nuclear Instruments and Methods in Physics Research Section A, vol. 824, pp. 359-361, Jul. 2016.

[2] M. Traxler et al., "A compact system for high precision time measurements (< 14 ps RMS) and integrated data acquisition for a large number of channels", JINST vol.6 C12004, Dec. 2011.

[3] D. Przyborowski et al. “Development of a dedicated Front-end Electronics for Straw Tube Trackers in the PANDA Experiment”, submitted for publication in JINST, May 2016.

[4] C. Ugur, G. Korcyl, J. Michel, M. Penschuk, M. Traxler “264 Channel TDC platform applying 65 channel high precision (7.2 ps RMS) FPGA based TDCs”, IEEE Nordic-Mediterranean Workshop on Time-to-Digital Converters (NoMe TDC), pp. 1-5 Oct. 2013

[5] G. Korcyl “A novel data acquisition system based on fast optical link and universal readout boards”, CERN-ACC-2015-0142, June 2015.

[6] J. Michel et al. “The HADES DAQ System: Trigger and Readout Board Network”, IEEE Transactions on Nuclear Science. 58, Vol. 4, pp. 1745-1750. 2011.