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A new preprocessing and control board for the phase 2 electronics of AGATA experiment.

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The electronics of AGATA HPGe segmented gamma ray detector faces a new challenge in the search of a bigger integration and cost reduction for the phase 2 of the experiment going beyond 45 crystals. This opportunity can be used to introduce a new architecture based on commercial standards while keeping backward compatibility with current electronics. In this sense, new FPGA devices and fast Ethernet links can be used to ease the preprocessing and control task and allowing for processor farms to distribute the processing load. At the same time, modularity should be a key feature of the design in the aim to make it upgradable in time and technology.

For only one crystal, current electronics is based on electronic digitizing and preprocessing involving 3 different types of electronics cards: one for the digitizing of the 38 signal channels corresponding to 36 segments plus two core channels, one for slow control and clock distribution and one for the preprocessing of the digitalized data. The throughput of data after the digitalization is about 2 Gbps per channel summing up a total aggregate bandwidth of 72 Gbps per crystal and after preprocessing, data are sent to servers through dedicated PCI express link.

This paper presents the design of a new preprocessing and control board that fulfills with the experiment requirements having in mind that it should not be only a new system but also should serve as replacement of the current electronics. The design is intended to process the data coming from 3 crystals (114 channels) in the same board, with a total aggregate bandwidth of 216 Gpbs using 2 Gbps input optical fiber links in SNAP12 format and with a data readout done through Ethernet fiber optics.

For functional purposes, a prototype able to process one crystal has been designed. This prototype consists on a FMC mezzanine card with four SNAP12 optic links receiving 38 2Gbps channels and a multiplexing aggregation 1:4 to compress the inputs to ten 10Gbps output lines. The output then goes through a FMC connector to a FPGA-based master board. The FMC Mezzanine is controlled by a SPI protocol through the FMC connector with an internal low cost and low power FPGA. This slave FPGA is seen as a standalone intelligent device to the master board FPGA, making unnecessary to implement an active slow control on it.

The data readout will be managed by another FMC mezzanine based on an Ethernet 40 Gbps connector and a FPGA to make it independent of the master FPGA. Readout will use a homemade protocol based on UDP to secure data transmission.

It is expected that, with this new system, the level of integration will raise up to 3 times while cost will scale down a 30% with respect to the current electronics.

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