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Design and evaluation of a FPGA online feature extraction data pre-processing stage for the CBM-TRD experiment

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The feature extraction is a data pre-processing stage of the proposed data-acquisition chain (DAQ) for the CBM-TRD experiment at FAIR, aiming to deliver event-filtered and bandwidth-reduced data to the First Level Event Selection (FLES). A data rate of about 1TB/s and a high event rate of approximately 100 kHz is expected for the final experiment. The TRD detector of the CBM experiment will be composed of about 24,000 SPADIC 1.0 chips. The SPADIC 1.0 can deliver full time-bin signals plus useful metadata.

The presented firmware implements multiple algorithms in order to find and extract regions of interest within time-bin signals. Algorithms such as peak-finding, charge integration, center of gravity and time-over threshold were implemented for online analysis. On the other hand, a local clustering algorithm allows to find cluster members and to implement even further data reduction algorithms.

Feature extraction is a common problem in data acquisition of high-energy particle experiments. However, the hardware description language (HDL) based designs tend to be written to solve very specific problems in the data-acquisition chain. Constraints as data format, front-end electronics and data containers make reusing and maintaining HDL designs a difficult task for a firmware designer. According to the problem at hand, a previously developed feature extraction framework has been used to generate an alternative FPGA firmware that implements similar processing algorithms to the originally hand-written VHDL design. The mentioned framework allows the creation of FPGA firmware without the need of writing HDL code, such as VHDL or Verilog for instance. This is achieved by using a domain-specific language (DSL) with which the designer is able to focus on the mathematical operations to be applied over the time-bin signals while leveraging the low-level code generation to the DSL compiler.

The presented results in this work compare and analyze the design architecture of the hand-written FPGA firmware against the firmware generated by the feature extraction framework. Furthermore, performance results of the feature extraction stage used in the TRD data-acquisition chain during a beam-test campaign performed at the CERN-SPS hall in 2015 will be presented and discussed.

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