Development of a SiPM-on-tile ZDC Prototype

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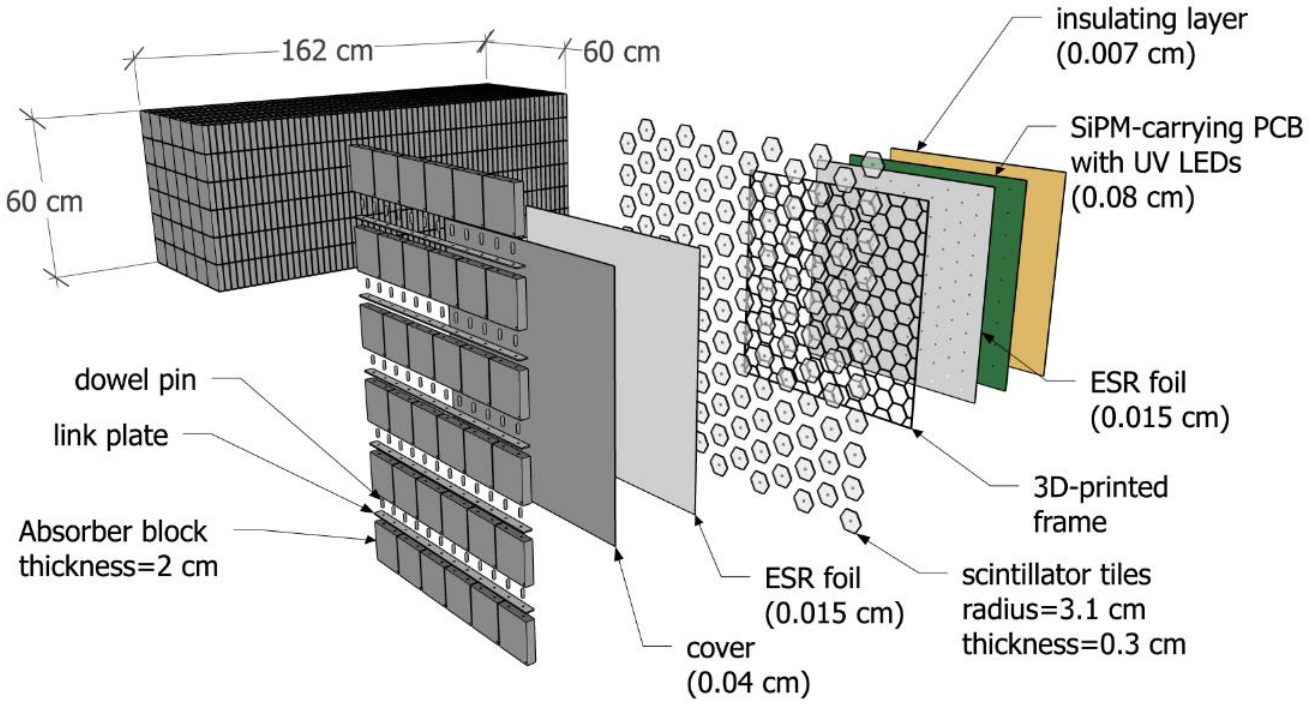
1/9/25

Overview

- The ZDC and previous prototypes
- Design and construction of the ZDC prototype
- Benchtop QA testing
- Related simulations
- Scaling to the full ZDC

Zero Degree Calorimeter

- SiPM-on-tile calorimetry will be employed at ePIC in the forward + backward HCAL, CALI, and the Zero Degree Calorimeter
- An iron-scintillator design is non-compensating on the hardware level, but can be corrected in software
- The position resolution can be enhanced by staggering each layer of tiles



Design of a SiPM-on-Tile ZDC for the future EIC, and its Performance with Graph Neural Networks

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Previous Prototypes

- Gen I prototype consisted of 10 sampling layers, 40 channels
  - Tested with 4 GeV positrons at Jefferson Lab in Jan 2023

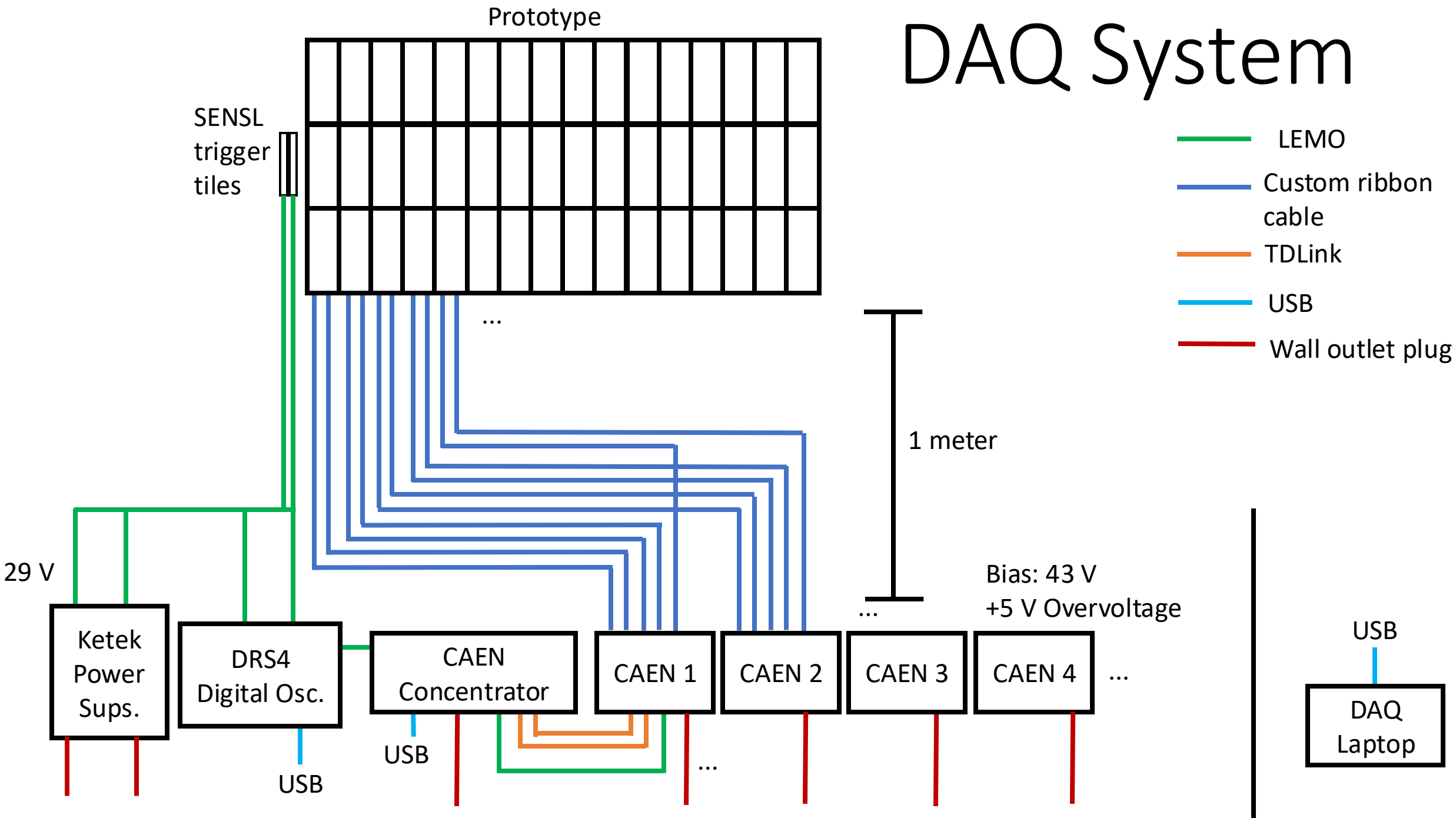
- Gen II prototype consists of 9 sampling layers, 192 channels
  - Tested in the STAR experiment hall at RHIC, run from April – October 2024
  - We plan to expand to 368+ channels for the upcoming RHIC run

Generation III Prototype Design

- Same block-and-pin construction as previous prototypes
- Area of 29.4 cm x 28.8 cm
- Each layer consists of 5 x 5 square scintillating tiles, shifted diagonally every other layer
- To be tested in February with 2 GeV p and 56 GeV Fe-56 at NSRL at BNL, with 30 sampling layers
- To be tested with 4 GeV e+ at JLab with 15 sampling layers

2 cm of iron = 1.1 X_0

DAQ System


Prototype
SENSL
trigger
tiles
...
LEMO
Custom ribbon
cable
TDLink
USB
Wall outlet plug
1 meter
29 V
Ketek
Power
Sups.
DRS4
Digital Osc.
USB
CAEN
Concentrator
USB
CAEN 1
CAEN 2
CAEN 3
CAEN 4
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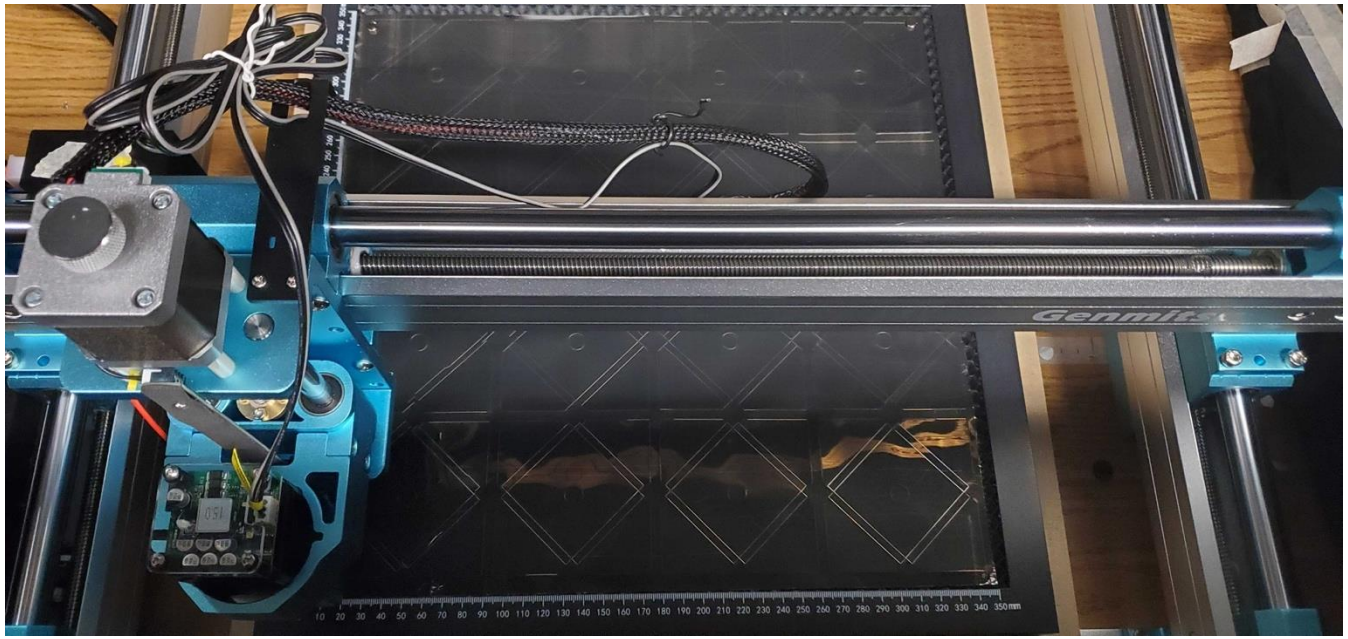
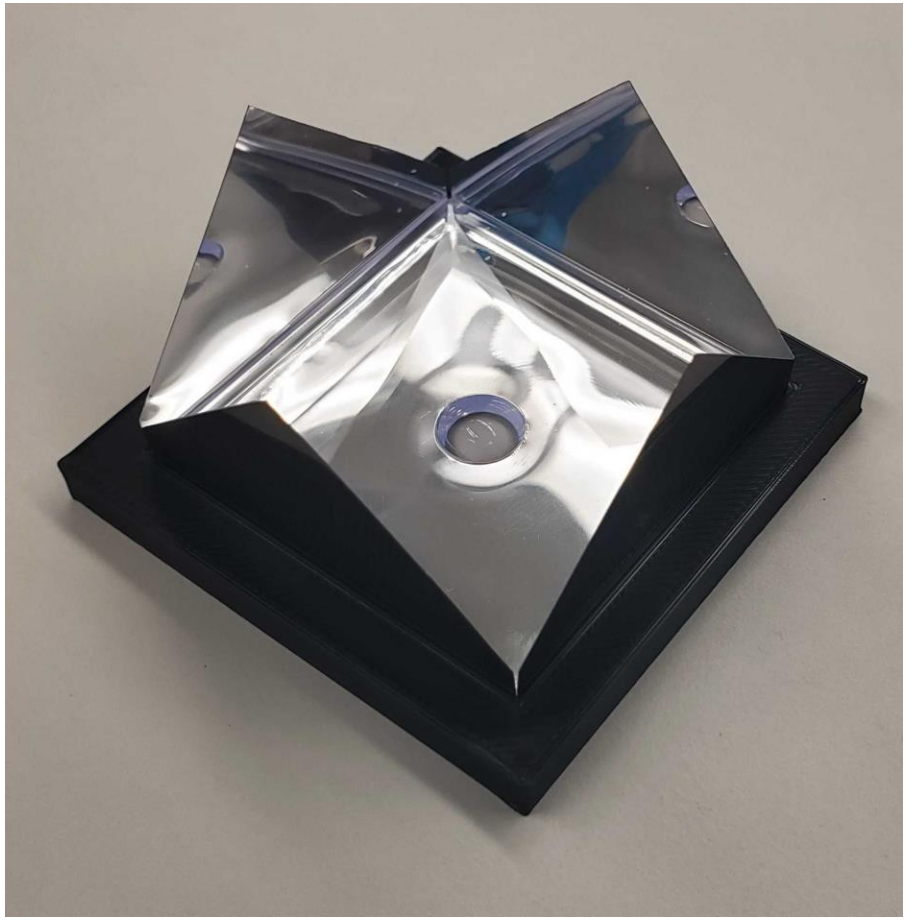
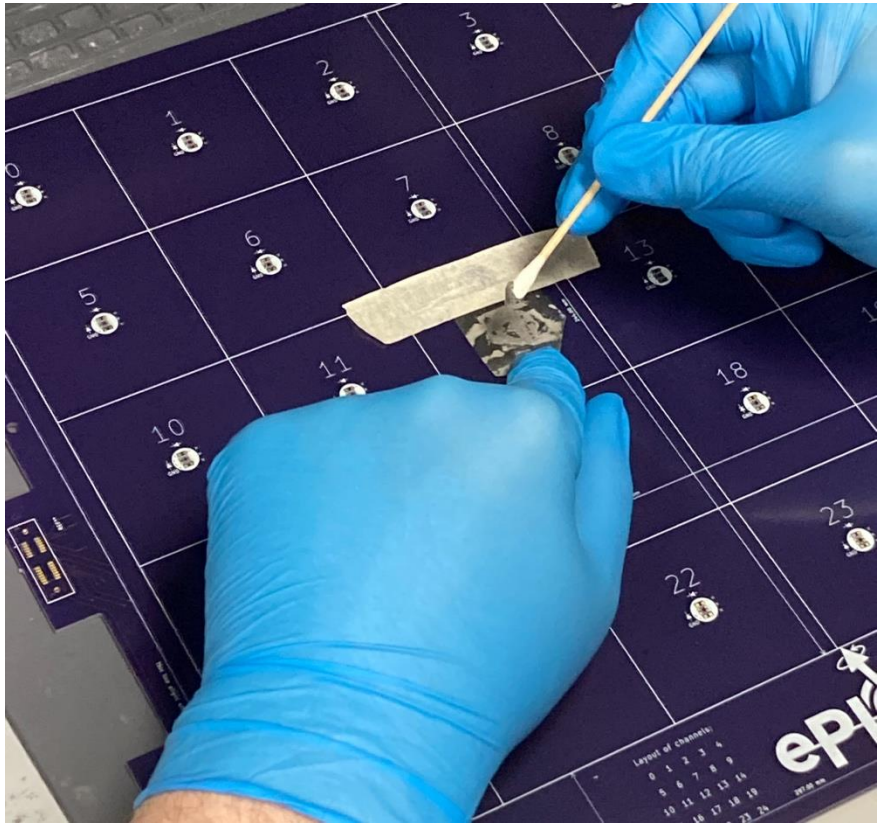
Bias: 43 V
+5 V Overvoltage
USB
DAQ
Laptop

Tile Construction



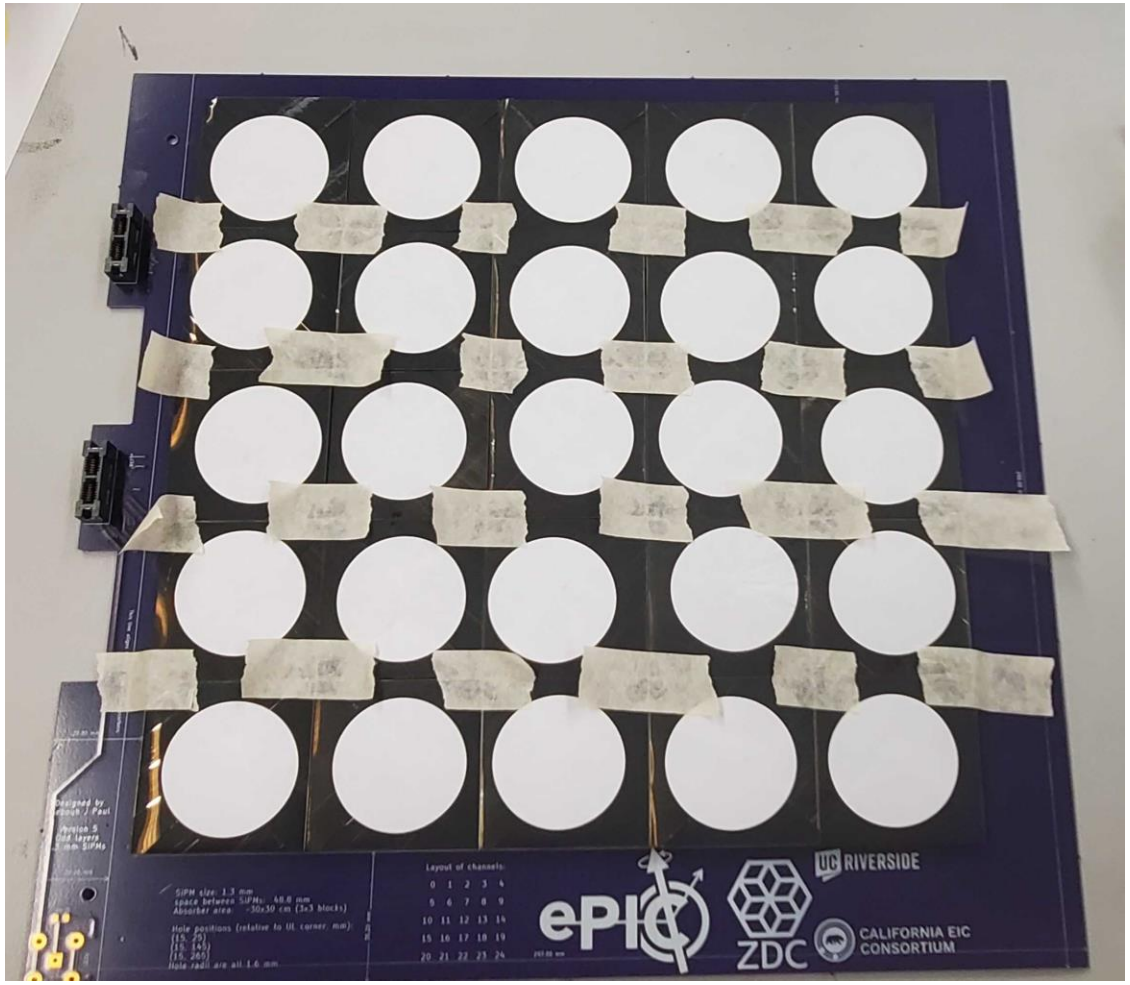


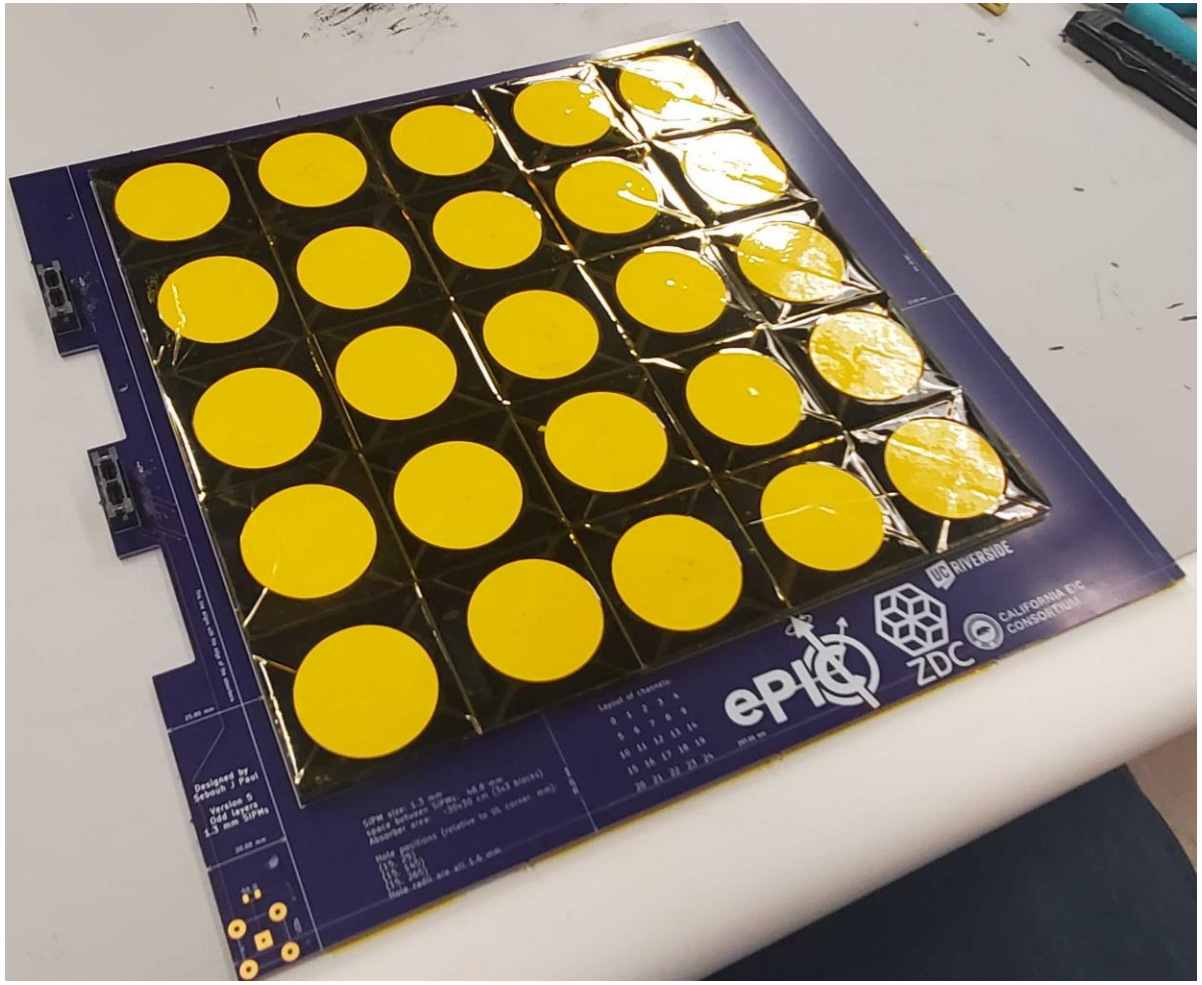
- ESR foil is cut using a CNC laser, and individually folded around each tile
- Tile dimensions 48.8 mm x 48.8 mm x 4 mm
- Completing 16 tiles: 10 minutes preparing, 30 minutes cutting, 40 minutes folding



PCB Construction

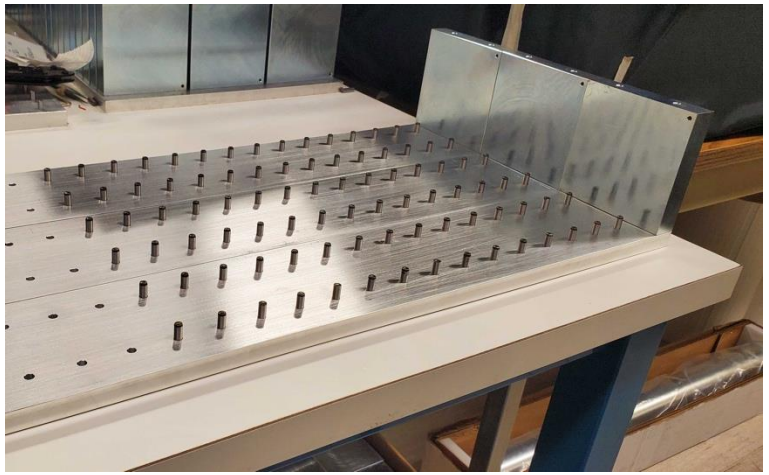
- Connectors are soldered to the PCB
- 1.3 mm SiPMs are soldered to the PCB using an IR oven

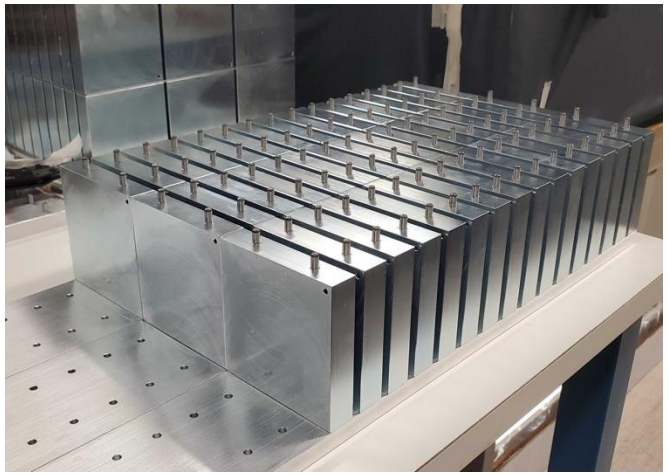


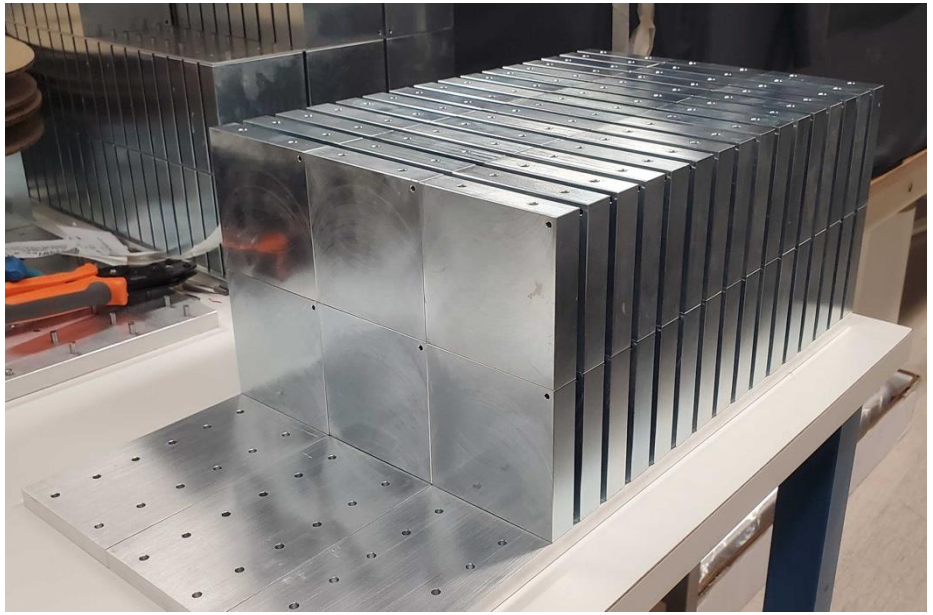


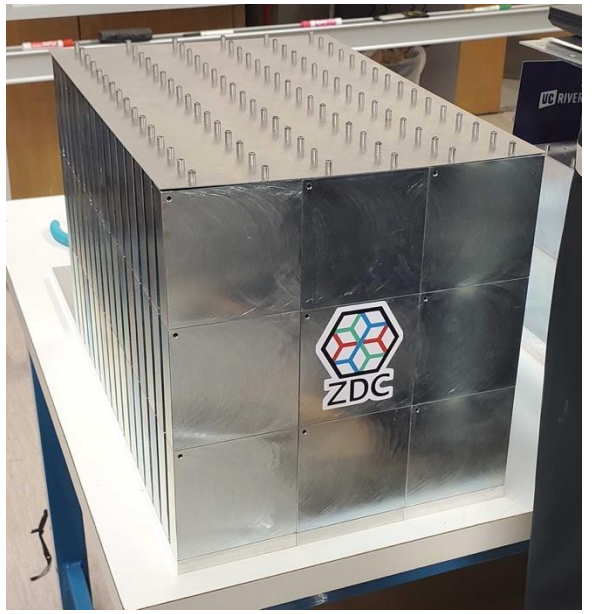
- After QA checks, tiles are affixed to the board via double-sided tape
- Polyimide film is placed on the front and back of the board to protect it from damage

Iron Structure Construction

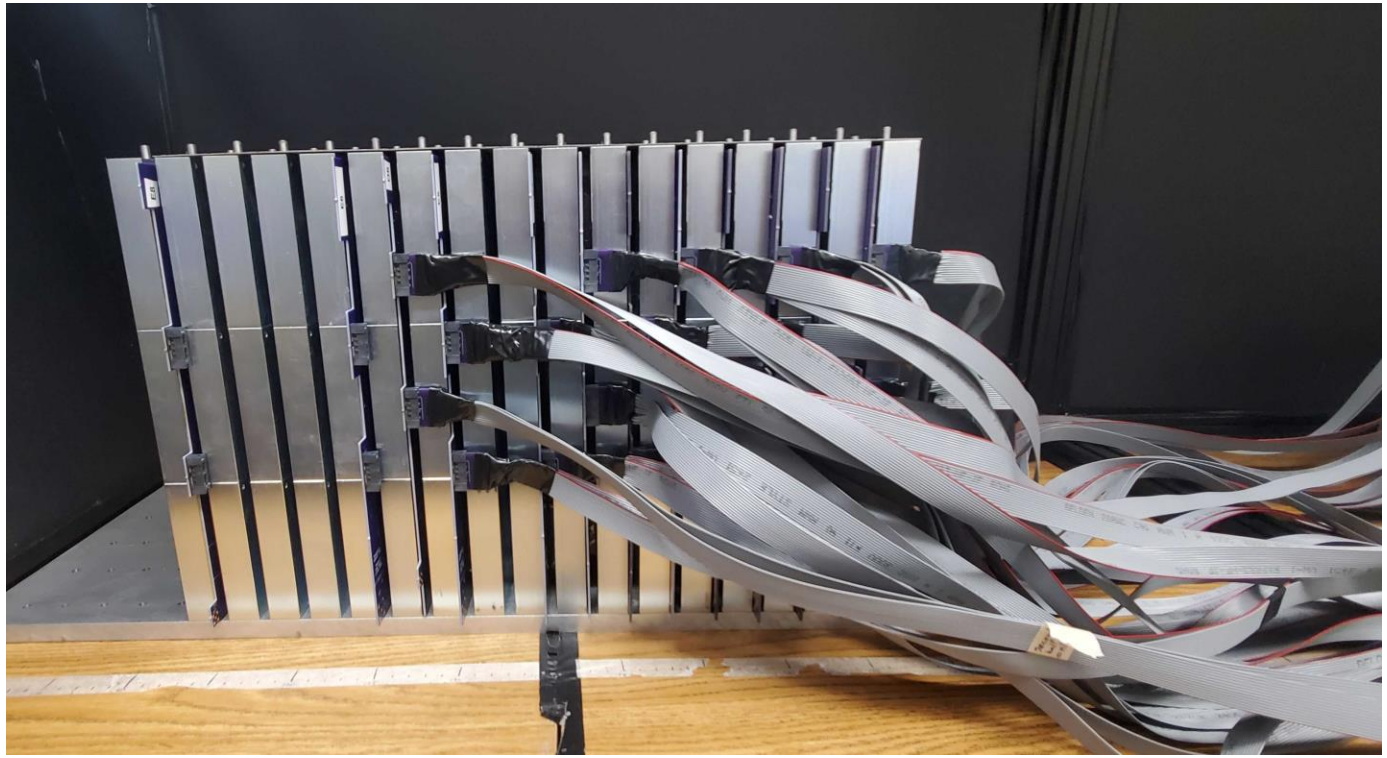








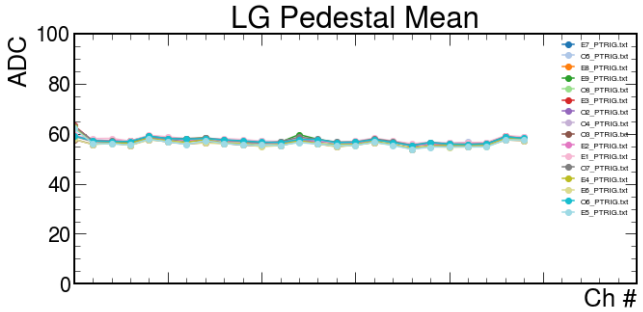
- LEGO-style pin-and-block assembly
- Active components can be placed in their respective slots post-assembly
- 15 layers can be assembled in 20 minutes
- Absorbers are being shipped to each laboratory

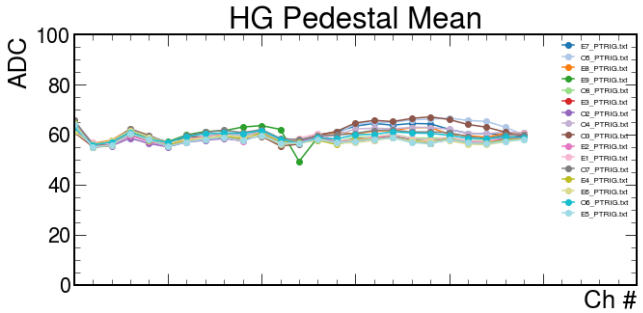


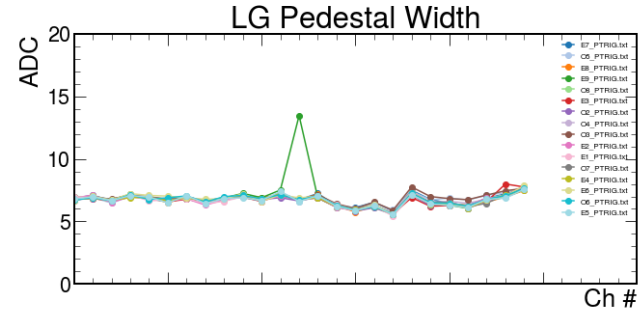
- PCB layers are connected to CAEN-DT5202 units via custom soldered 28 AWG ribbon cables and custom CAEN adapters
- The cables and connectors will remain the same for the final ZDC
- CAEN-DT5202 units, a CAEN-DT5215 concentrator, and DRS4 digital oscilloscope will be mounted on an 80-20 frame one meter away

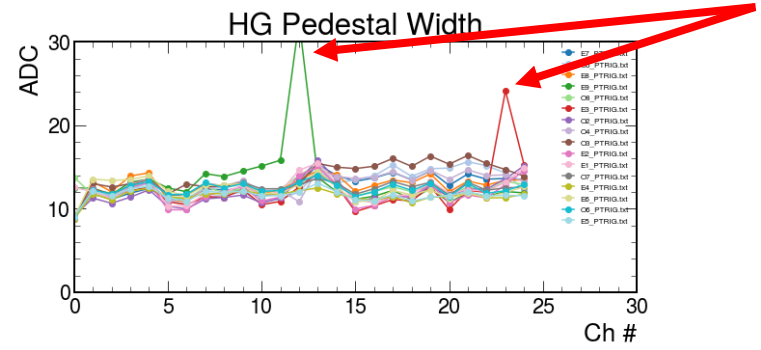
Benchtop QA Tests

- Before tiles are affixed to a board, it is QA tested to ensure all channels are behaving nominally
- Recording pedestal means and widths via the CAEN Janus DAQ software can quickly identify shorts or other obvious faults



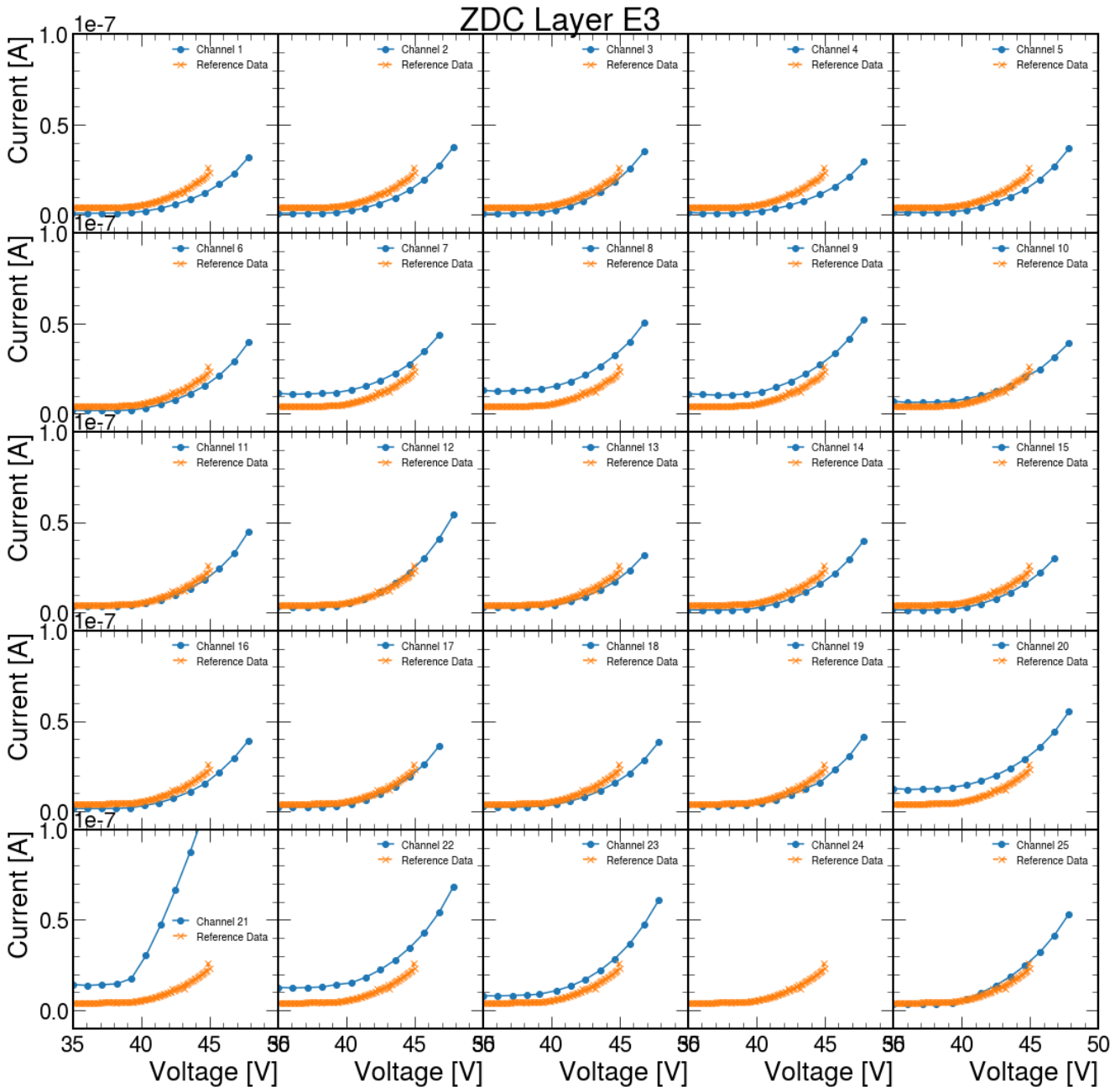




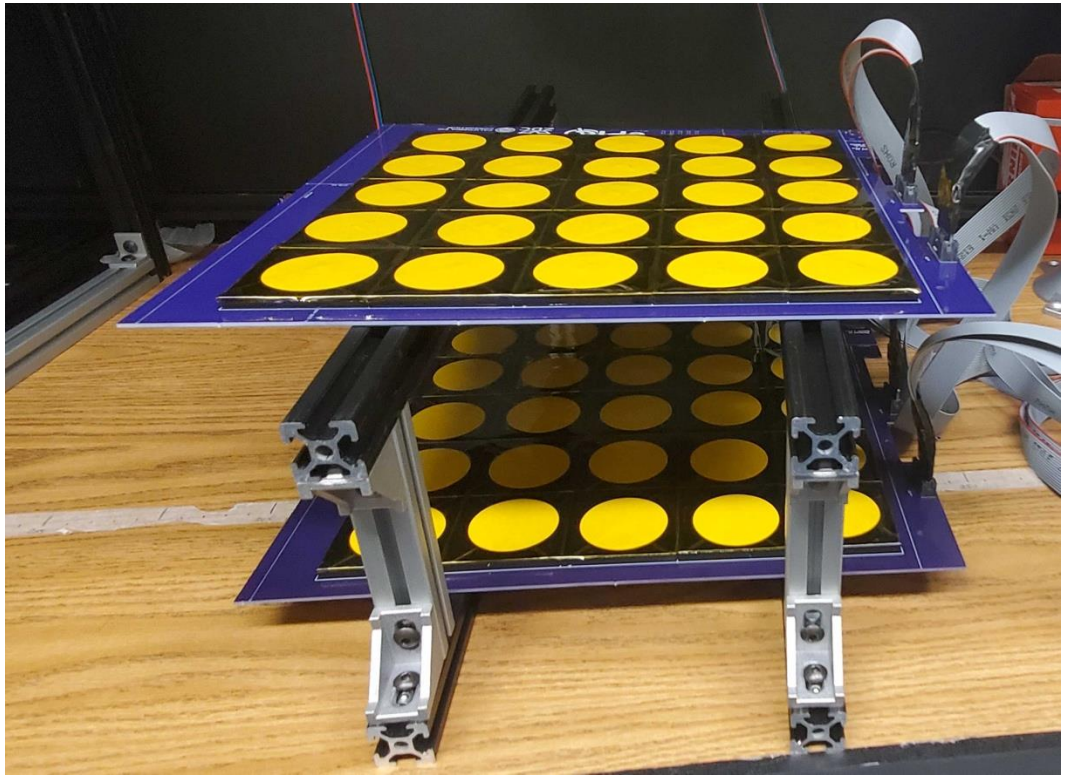


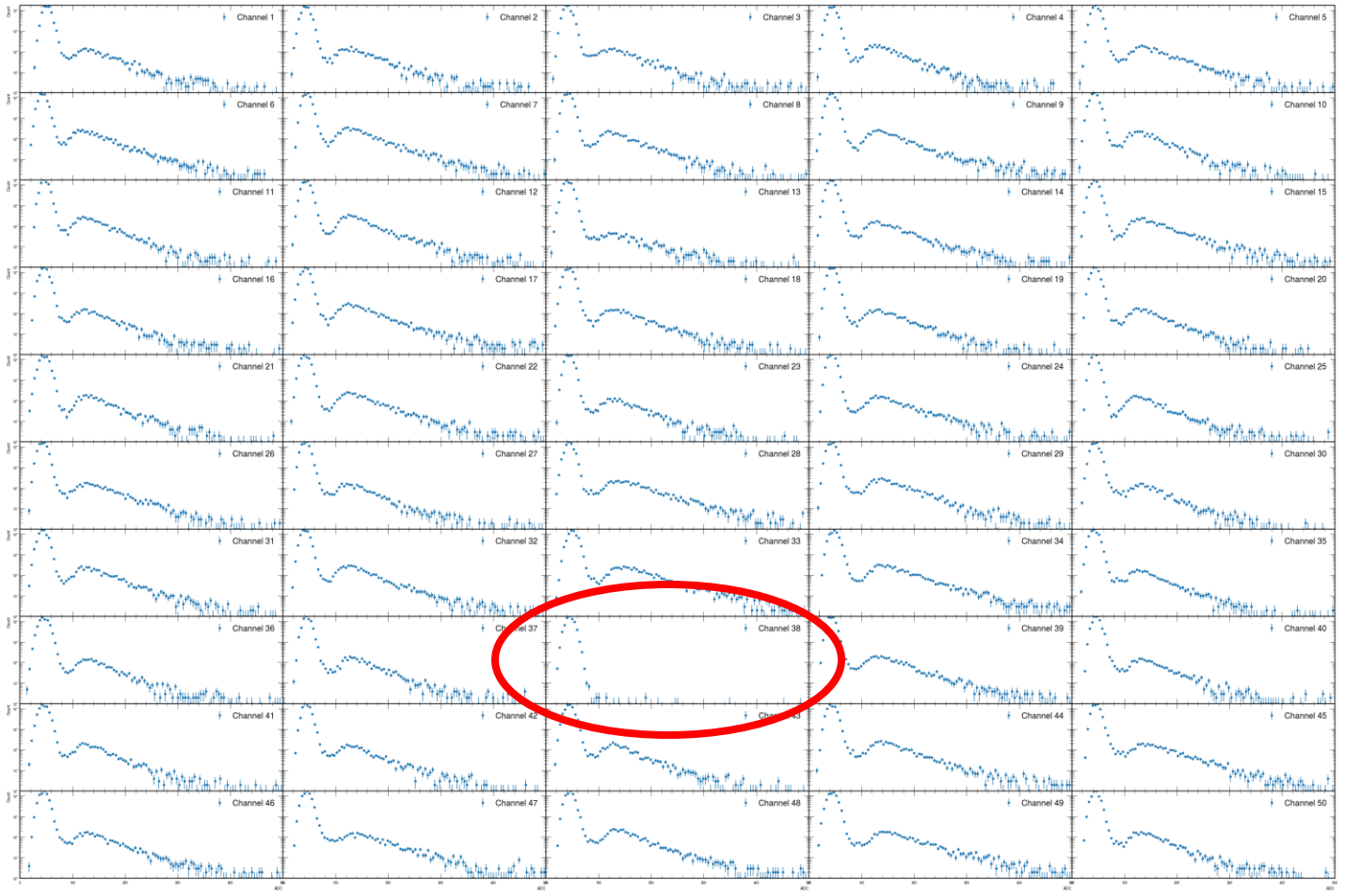
- Passing the pedestal test, each channel in a board is tested with an IV scan

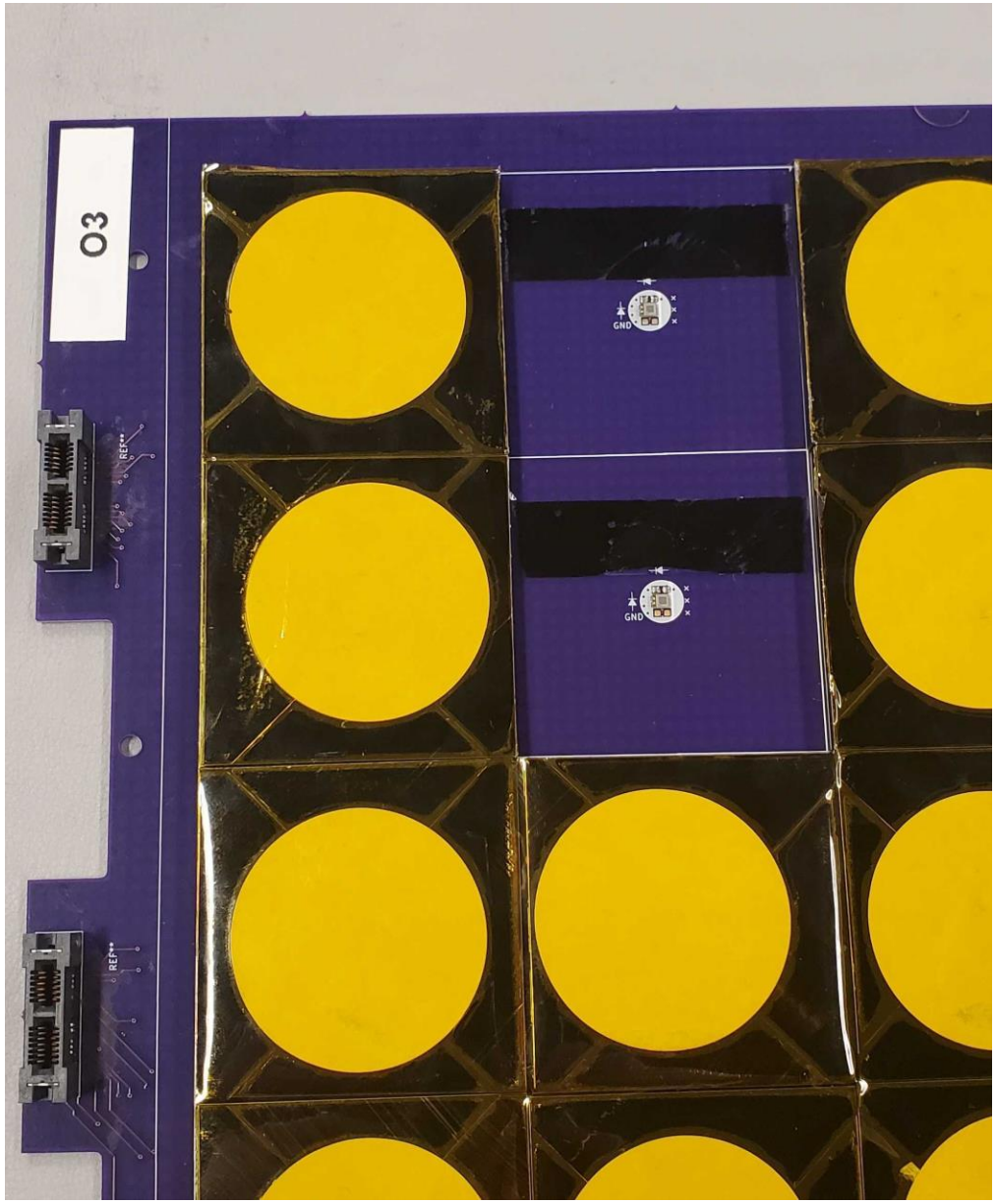
- If a channel behaves significantly different from a reference SiPM, it is closely monitored during a cosmic ray test



- Layers are then tested with cosmic rays two at a time with a MAJ=2 trigger, to confirm that it begins to record a landau curve



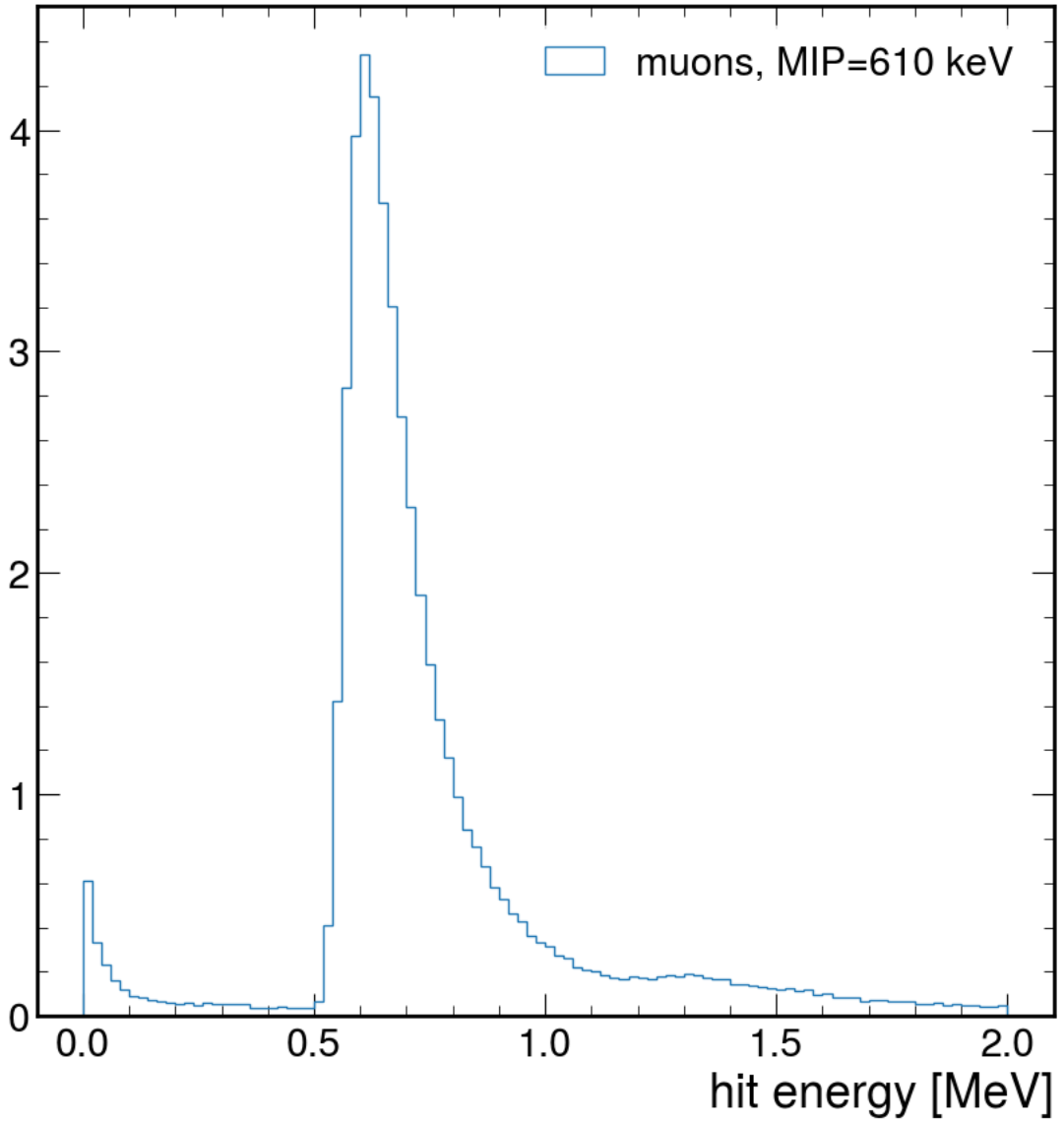




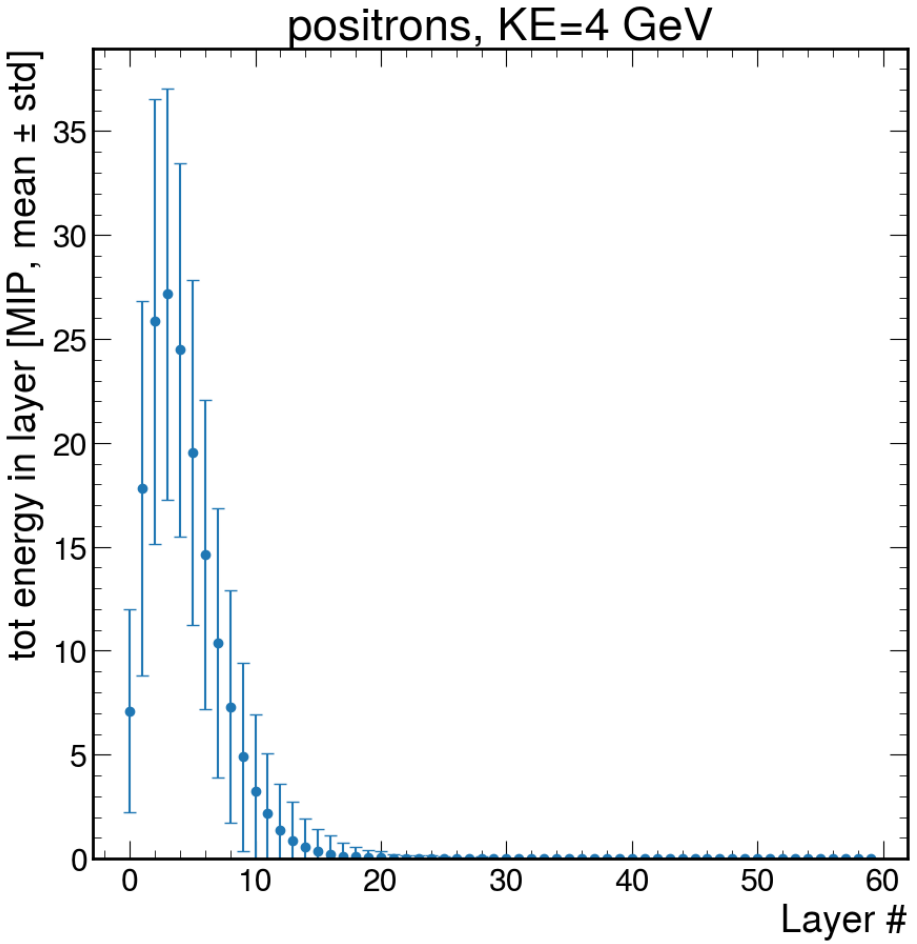
- If a channel is confirmed dead via the QA tests, the SiPM is replaced by heating the channel from below with a hot air gun

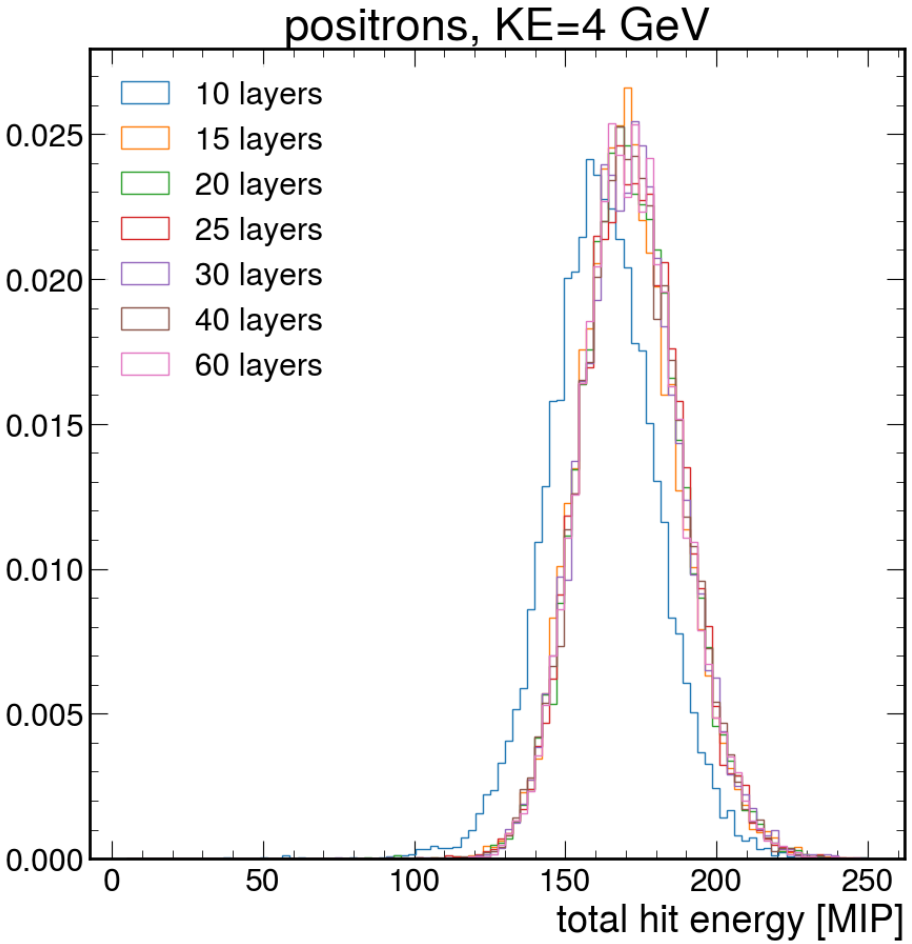
- If the tiles are affixed and wrapped in polyimide before the channel goes dead, the SiPM can still be accessed and replaced

Simulations



- Simulating muons reveals the MIP peak to be found at 610 keV
- Channel-by-channel MIP calibration will be performed via benchtop tests and in-situ

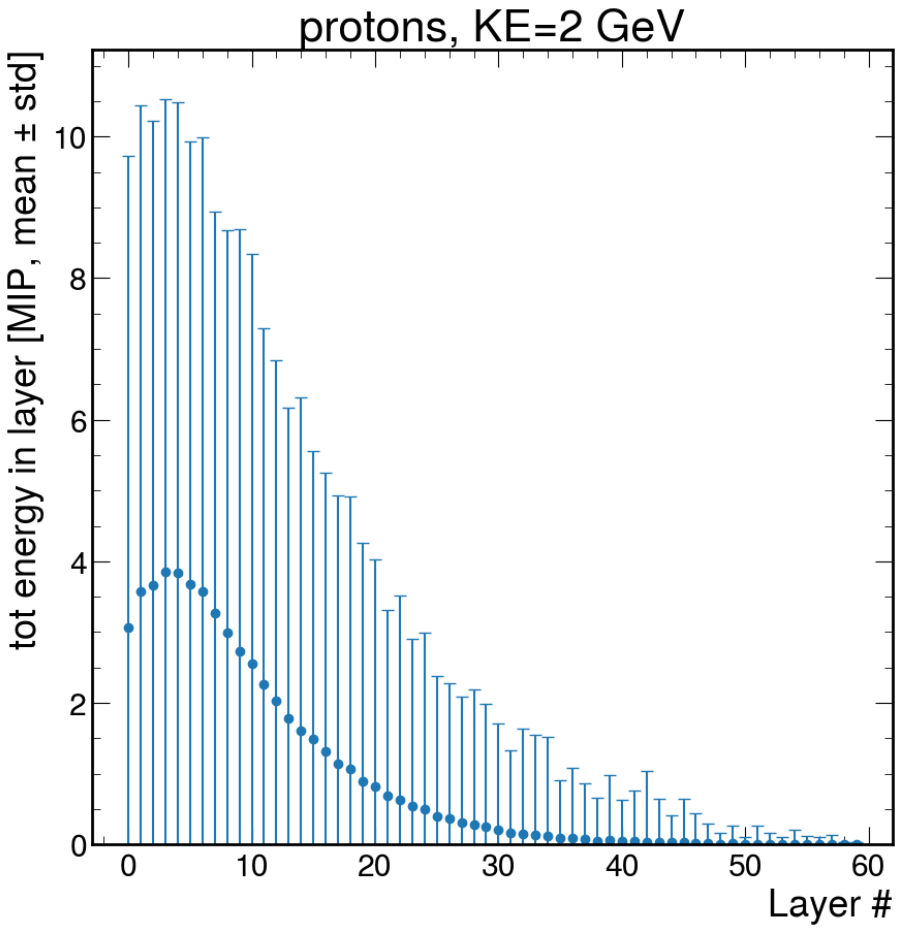


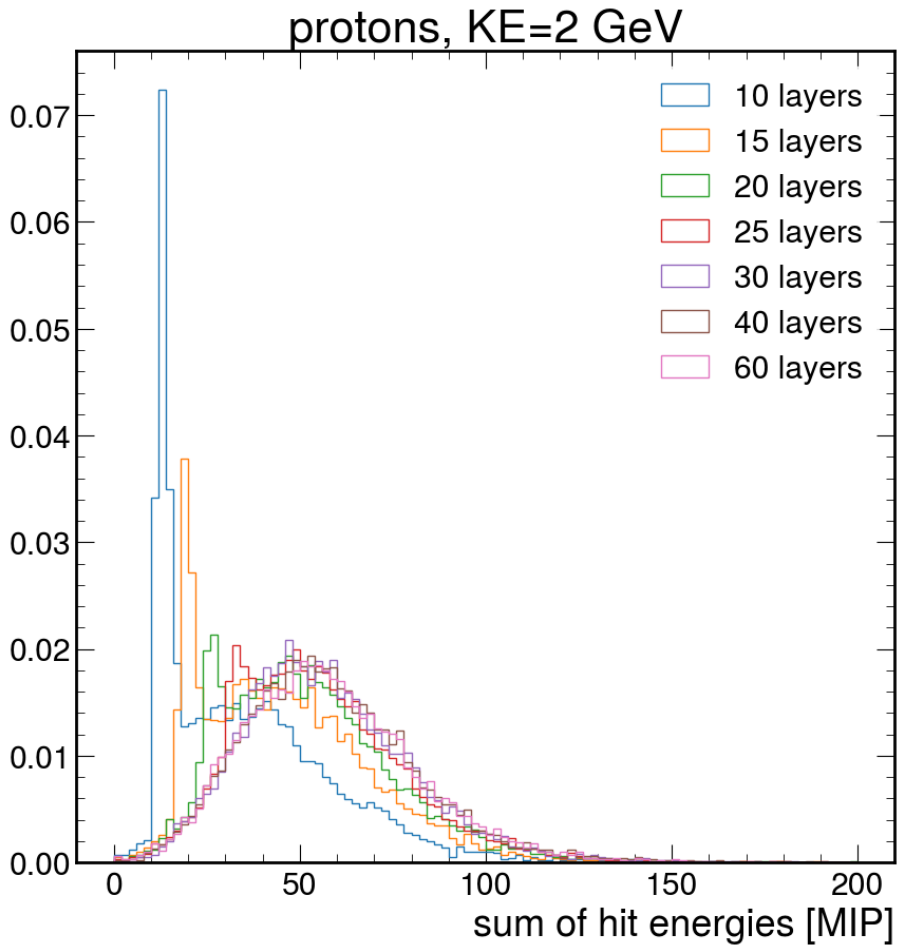


Jefferson Lab Hall-D Pair Spectrometer simulation

- When simulating 4 GeV e+, only 15 layers are needed to capture the entire shower

Brookhaven National Laboratory

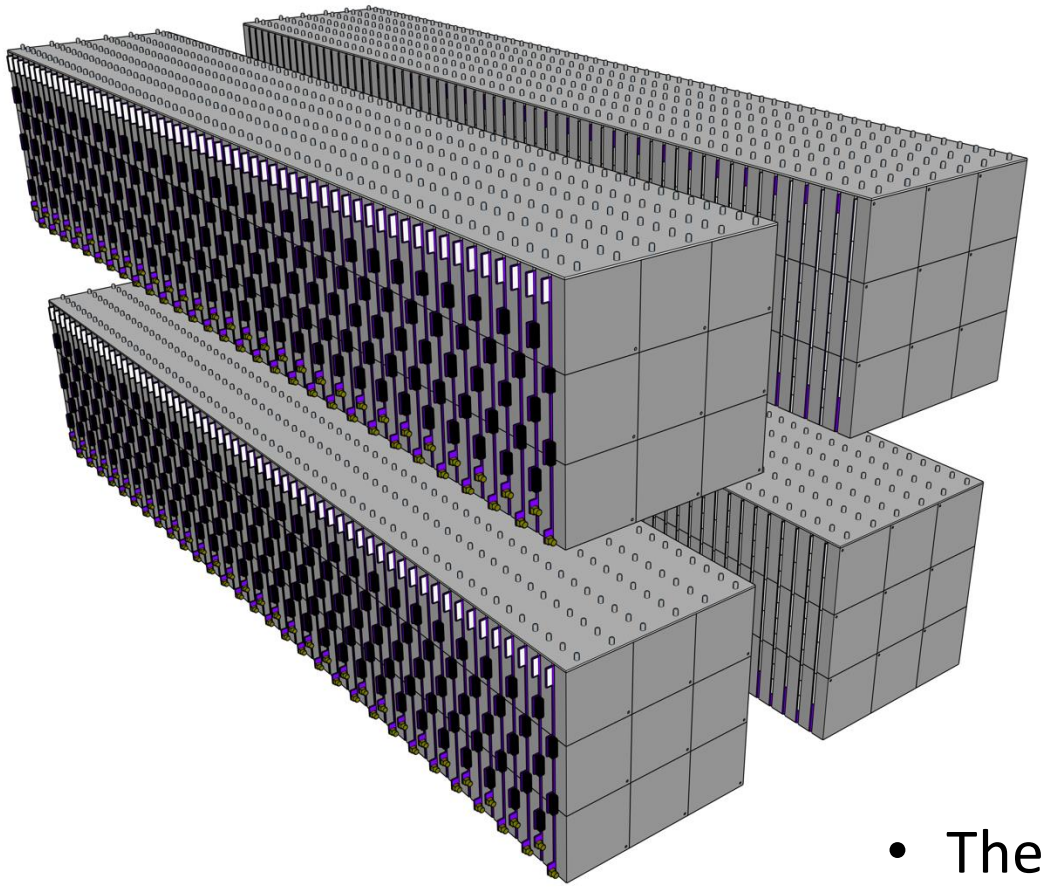


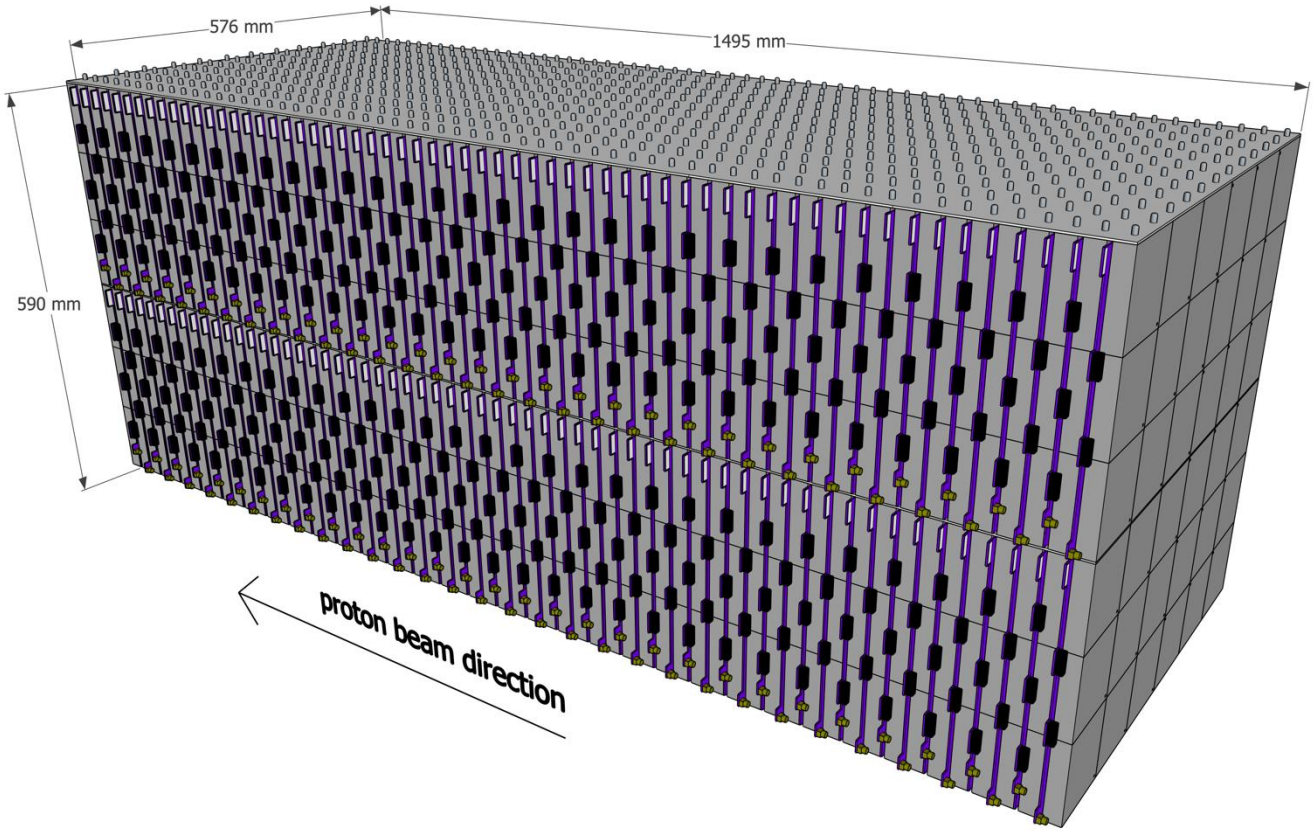


BNL NSRL Simulations

- When simulating 2 GeV p, 30 layers are needed to capture the entire shower

Scaling to the full ZDC

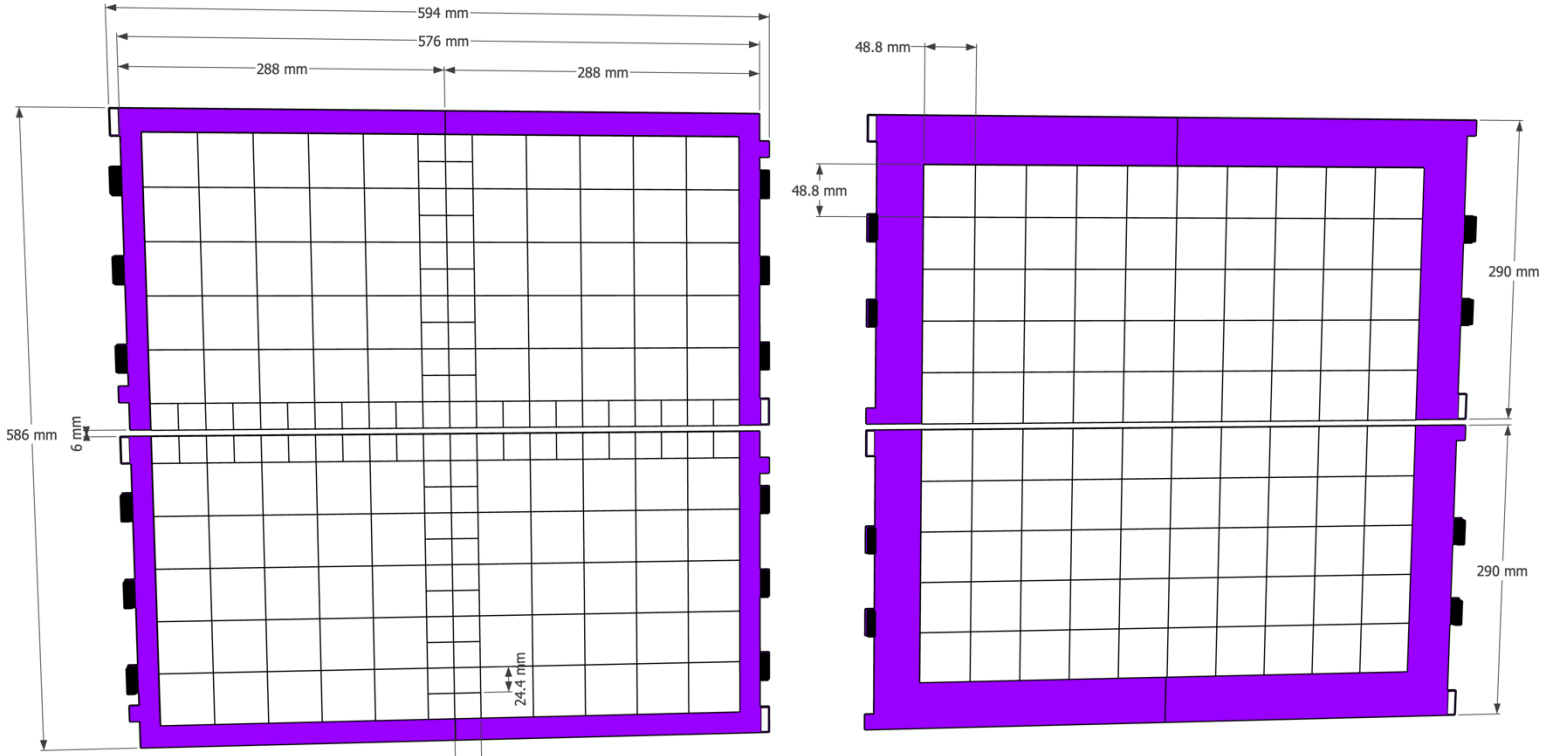


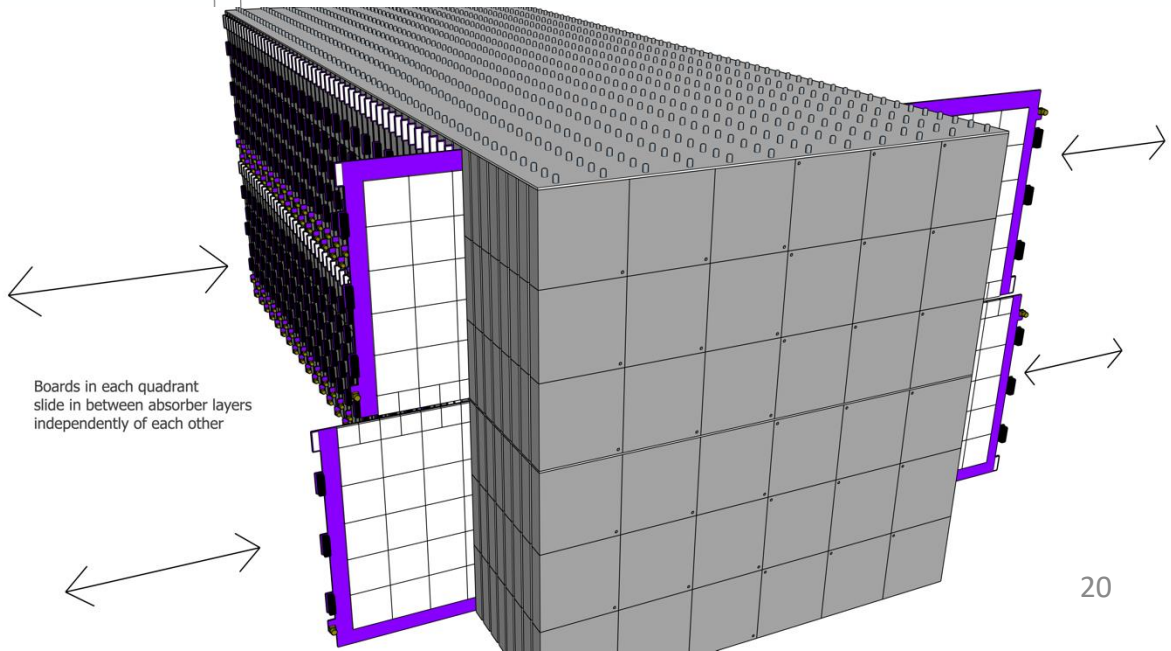


- The ZDC prototype is structured as 30 (out of 60) layers of one quadrant of the entire ZDC

- The final ZDC PCB design is mostly unchanged from that in the prototype, so they may be reused in the ZDC

- Every other layer will add one row and one column of small cells to prevent dead gaps between PCBs





Summary

- Improving from the Gen I and II SiPM-on-tile prototypes, the ZDC prototype will consist of 15 / 30 sampling layers, with 25 channels per layer
- Construction methods and QA testing are being refined to manufacture 100% functional layers in a way that can be scaled to the full ZDC
- This prototype has the same mechanical structure as one quadrant of the ZDC
- The ZDC prototype will be tested with p and Fe-56 beams at the NSRL in BNL, and e+ at the JLab Hall-D Pair Spectrometer

Thank you!