iRPC FEB cooling system

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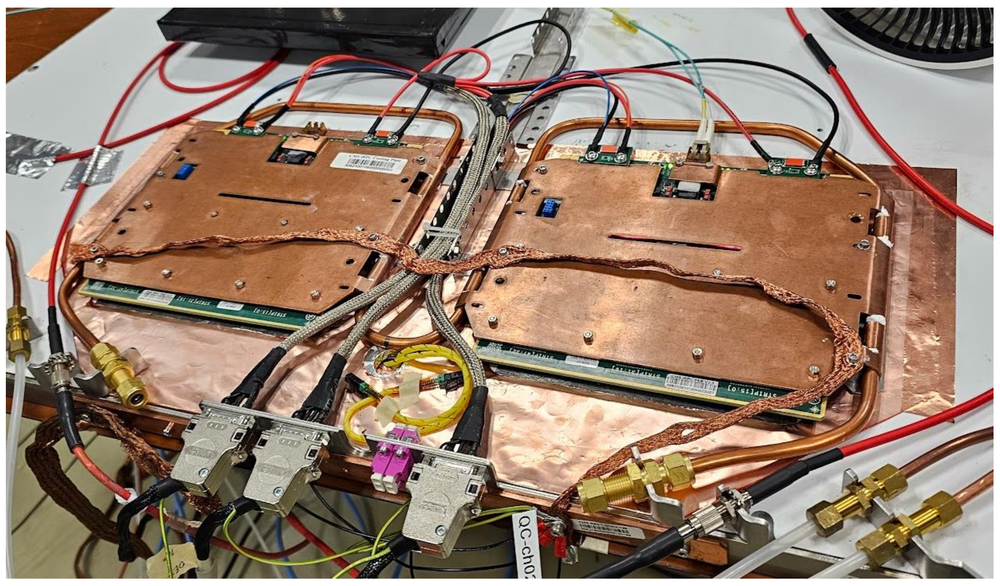
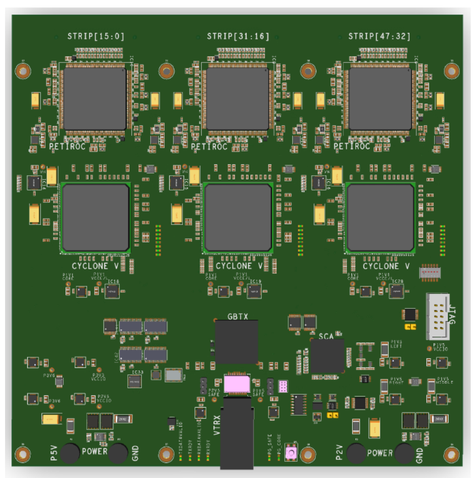
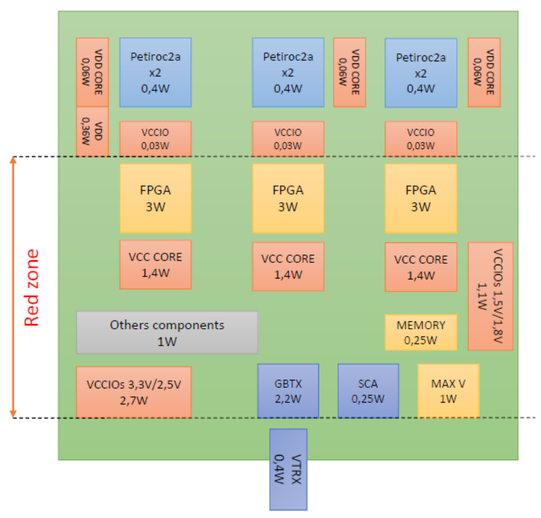
1. iRPC Feb cooling system Setup

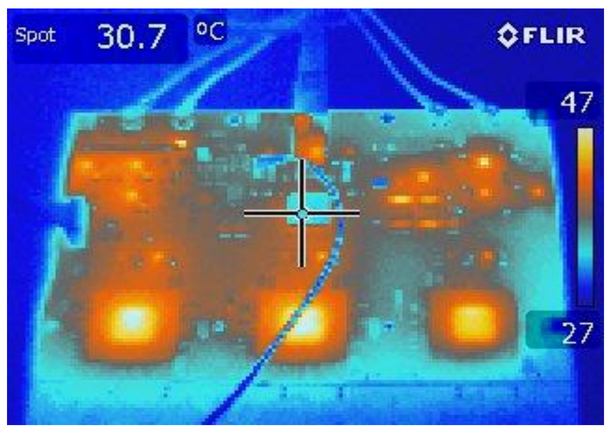


The cooling system consists of two 1.5mm copper plates, four copper bars, which are connected to a copper pipe, where the water flows. iRPC FEB Total power consumed by the FEB is ~19.5 W. According to the FEB description [1], the simulation model was created.



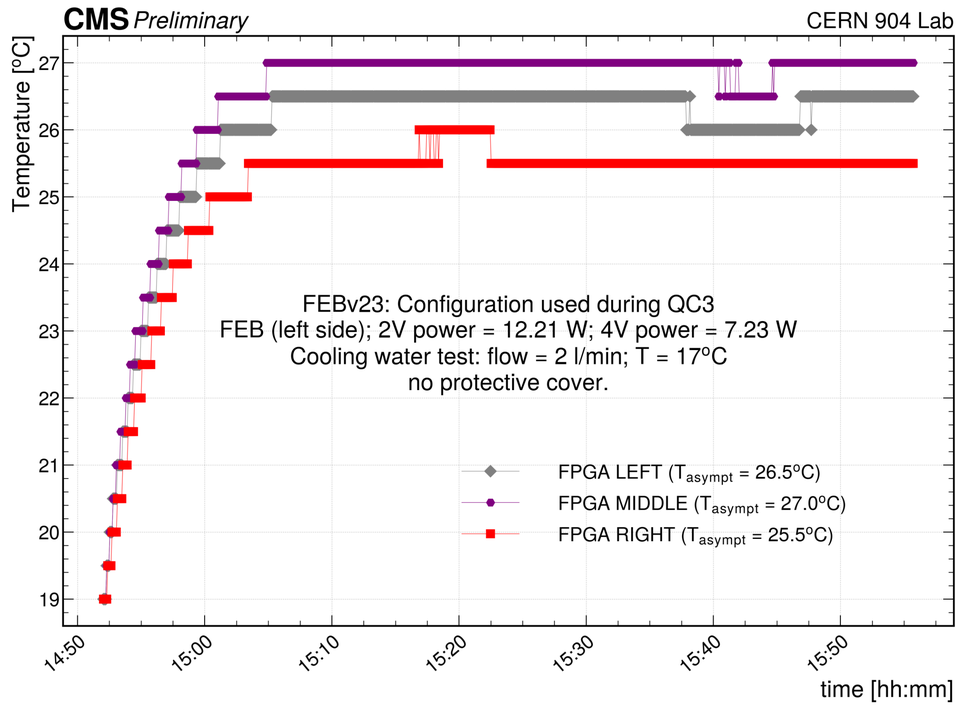


2. Test Results

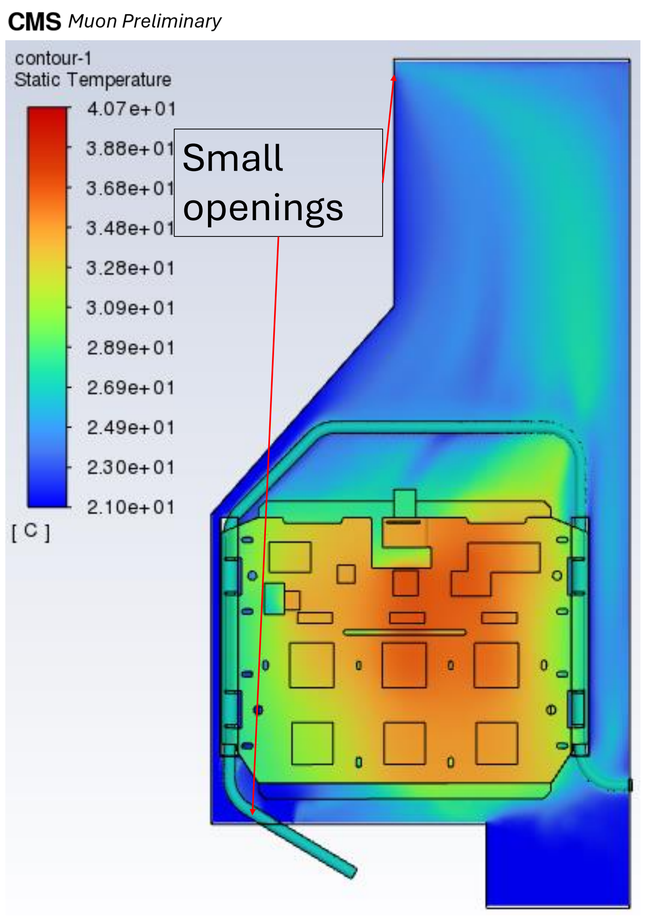


The image shows a thermal image of a working FEB.

The plot below illustrates the temperature behavior over time of an iRPC Front-End Board (FEBv23) equipped on an iRPC production chamber [2], measured by five sensors strategically positioned at the hottest points of the Front-End Board (FEB). A one-hour water cooling test was conducted with a controlled flow rate of 2 liters per minute and an input water temperature of 17°C, and the FEB powered with 12.21 Watt 2V port and 7.23 Watt shared 4V port.



3. Simulation results, thermal contours



The air convection here, is visible. This helps transfer of a heat from the hot areas, to the upper opening of the cover. The simulation was done with Ansys Fluent module, Transient, pressure-based solver. The setup consisted of 4 300 000 mesh hexagonal elements.
The adaptive, error based time stepping method was used.

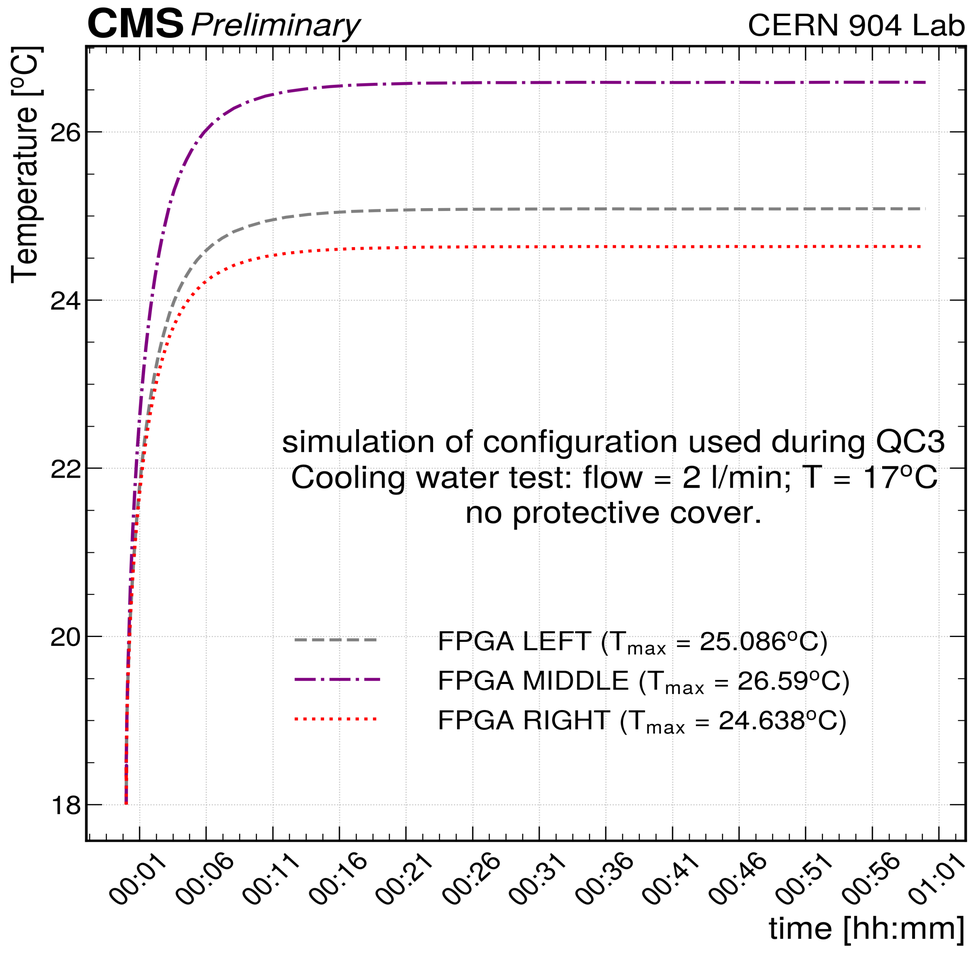
Flow rate of 2 liters per minute and an input water temperature of 17°C was assumed, as well as a water flow from right to left. A total power of 20W was assumed distributed over 21 most consuming components.

The outline of the gas domain, resembles to the cover, which isn't shown in the photo of the setup, above.

As expected, the high temperature area is in the middle of the FEB, around the middle FPGA which is the furthest from the cooling pipes.

4. Simulation results, temperature plots

The plot illustrates the temperature behavior over time simulated as an iRPC Front-End Board (FEBv23) equipped on an iRPC production chamber. Data took at three points of the Front-End Board (FEB) to be validated with the experiment. The temperature peaks at around 27 °C in 20 minutes from powering up the febs.



5. Conclusion

The simulation results closely align with the experimental test outcomes, demonstrating a strong agreement between the two. Both the maximum temperature and the rate of temperature increase are in close proximity, with a maximum temperature difference of 1.5°C observed for the FPGA chips. This minor discrepancy can likely be attributed to the idealized boundary conditions employed in the CFD module.

References

1. CMS Muon Collaboration, M. Gouzevitch, "CMS iRPC FEB development and validation", *Nucl.Instrum.Meth.A* 1064 (2024) 169400
2. CMS Collaboration, A. Samalan, "Upgrade of the CMS resistive plate chambers for the high luminosity LHC", *JINST* 17 (2022) 01, C01011

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