

The T-SDHCAL Hadronic Calorimeter for a Future Higgs factory



-  • IP2I Lyon
-  • OMEGA
-  • CIEMAT
-  • UCO - University of Cordoba
-  • VUB - Vrije Universiteit Brussel
-  • GWNU - Gangneung–Wonju National University
-  • YCC - Yonsei Cancer Center GWNU
-  • SJTU - Shanghai Jiao Tong University
-  • University of Tunis El Manar

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Outline

Semi-Digital HCAL (SDHCAL) technological prototype

- ✓ Description
- ✓ Test Beam results

Timing-SDHCAL (T-SDHCAL)

- ✓ Motivation
- ✓ Progress

Semi-Digital Hadron CALorimeter

The SDHCAL-GRPC is one of the two **highly-granular HCAL** options **based on PFA**; proposed for the **International Linear Detector (ILD)** option for the ILC/CEPC

Modules are made of 48 RPC chambers ($6\lambda_I$) equipped with **semi-digital, power-pulsed electronics** readout and placed in **self-supporting mechanical** structure that serves as absorber as well

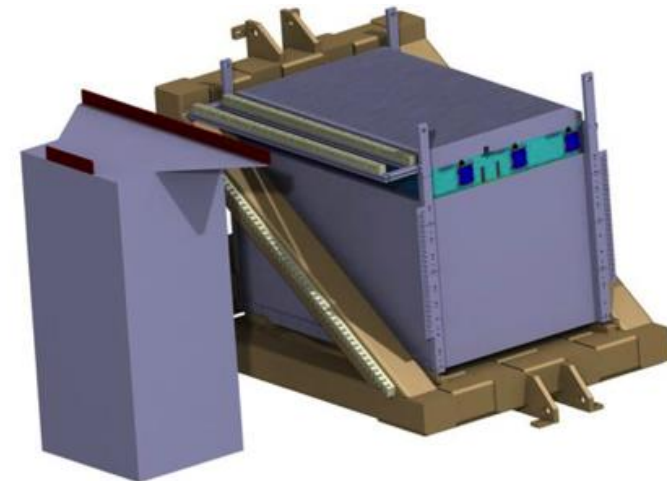
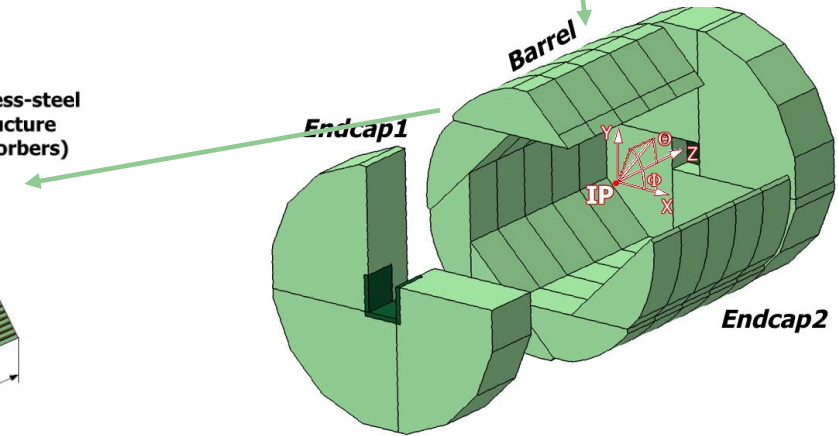
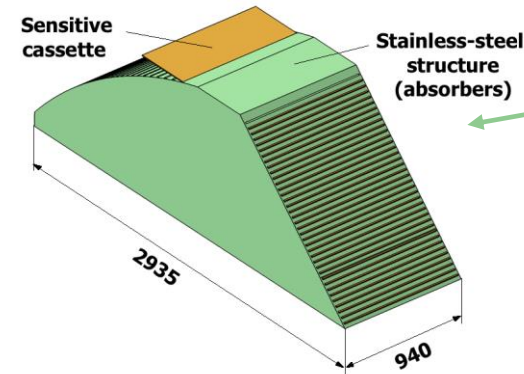
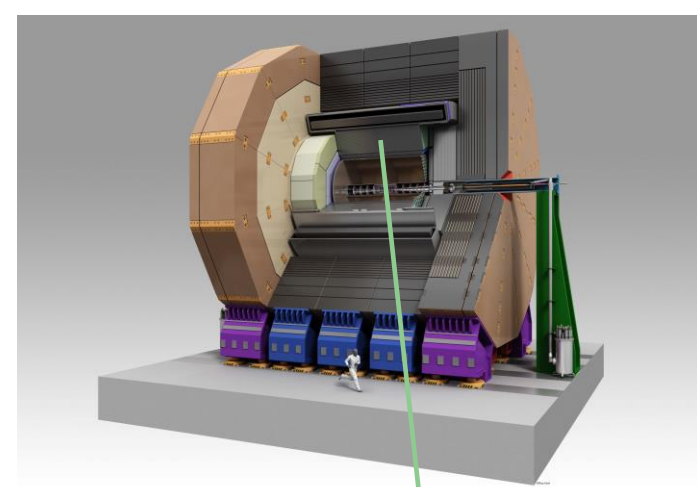
The structure proposed for the SDHCAL :

- very **compact** with negligible dead zones
- eliminates projective cracks
- minimizes barrel / endcap separation (**services leaving from the outer radius**)

SDHCAL Technological Prototype should be as close as possible to the ILD module and able to study **hadronic showers**

Challenges:

- Homogeneity for large surfaces
- Thickness of only few mms
- Lateral segmentation of 1 cm x 1 cm
- Services from one side
- Embedded power-cycled electronics
- Self-supporting mechanical structure

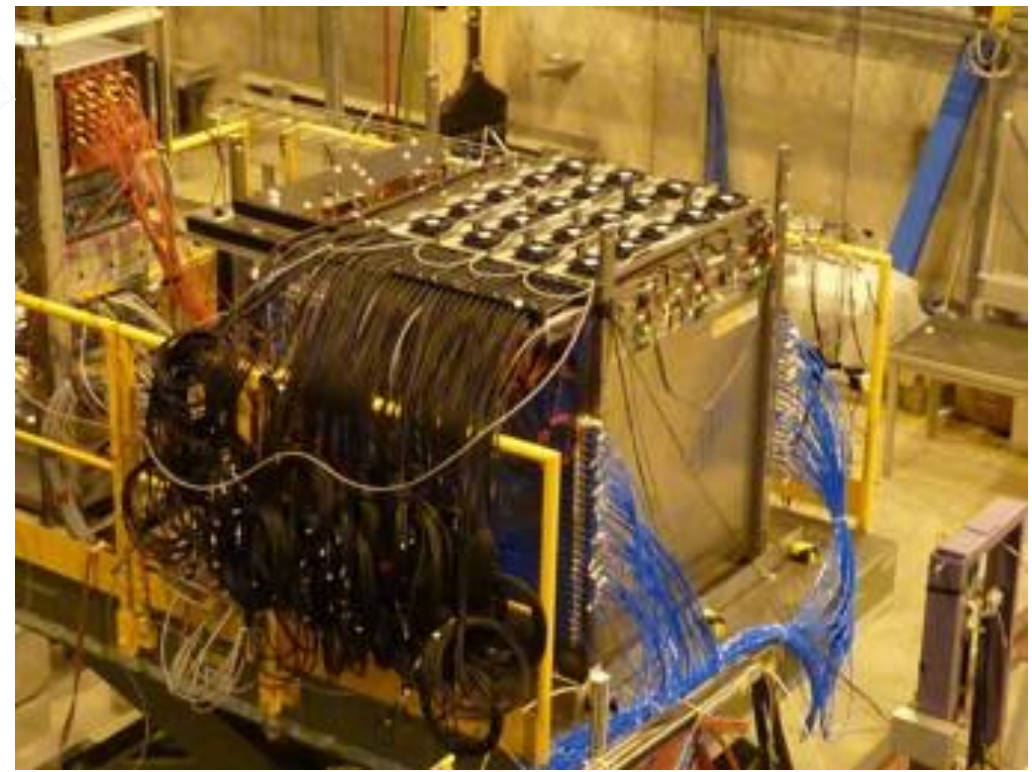
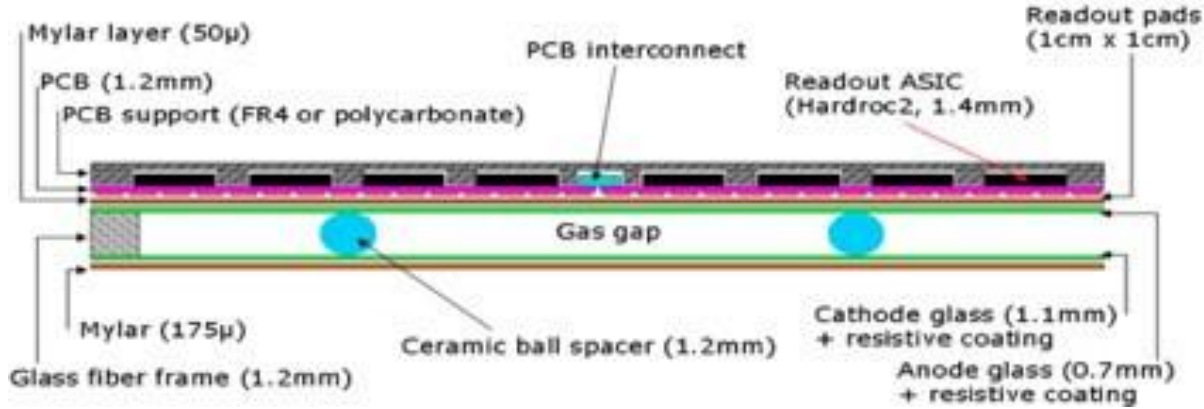


SDHCAL

SDHCAL was developed inside CALICE Collaboration
Sampling calorimeter:

Absorber: Stainless Steel

Active medium: single-gas Resistive plate Chambers



gRPC (3mm) + readout electronics (3mm), inserted in cassettes made of two 2.5mm stainless steel plates, i.e. **11mm thick layers**



JINST 10 (2015) P10039

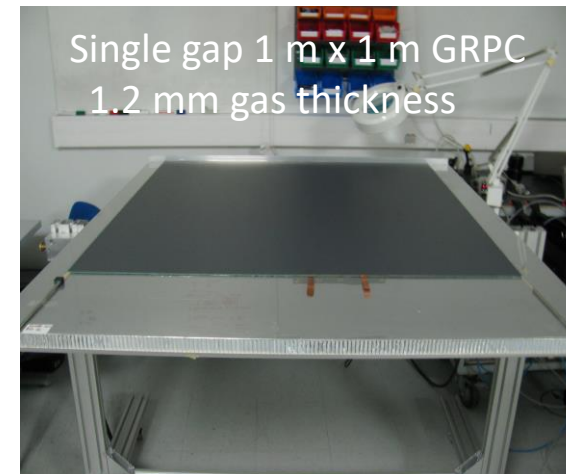
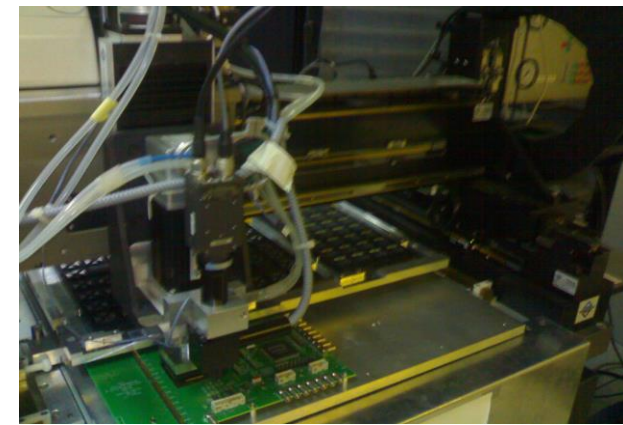
1 pad = 1cm²,
interpad 0.5 mm

144 ASICs = 9216 channels/1m²

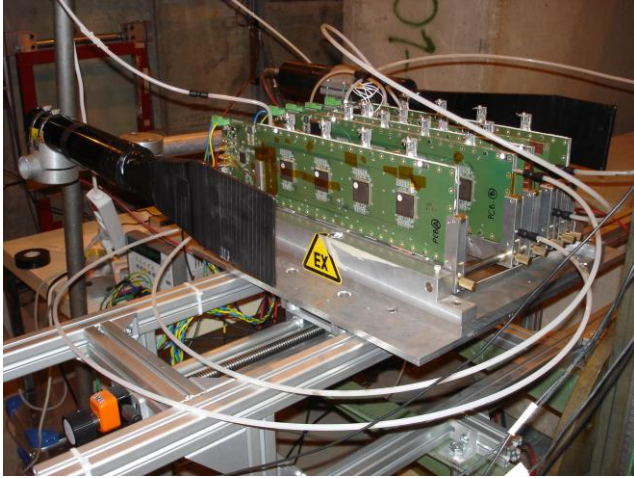
- ▶ 48-50 layers ($-6\lambda_1$); $\sim 1.3\text{m}^3$ prototype
- ▶ 1 cm x 1 cm granularity; $\sim 450\text{k}$ channels (more than full CMS calorimeter system)
- ▶ 3-threshold readout with 64-ch HARDROC ASICs
- ▶ Power-Pulsed system
- ▶ Triggerless DAQ system
- ▶ Self-supporting mechanical structure made with 15mm stainless steel plates
- ▶ gRPC operated with TetraFluoroEthane (TFE, 93%), CO₂ (5%) and SF₆ (2%)

SDHCAL Prototype Construction

- ✓ 10500 64-ch HARDROC ASIC were tested and calibrated using a dedicated ASICs layout
- ✓ 310 PCBs were produced, cabled and tested; they were assembled by sets of six to make 1m² Active Sensor Units (ASU)
- ✓ 170 Detector InterFace (DIF) boards, 20 Data Concentrated Cards (DCC) were built and tested
- ✓ 50 detectors were built and assembled with their electronics into cassettes
- ✓ Self-supporting mechanical structure
- ✓ DAQ system using both USB and HTML protocol was developed and used
- ✓ Full assembly took place at CERN

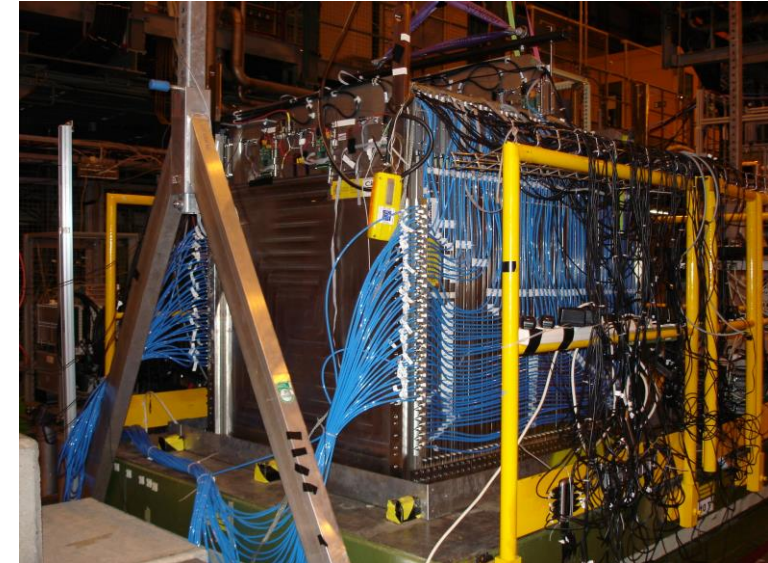
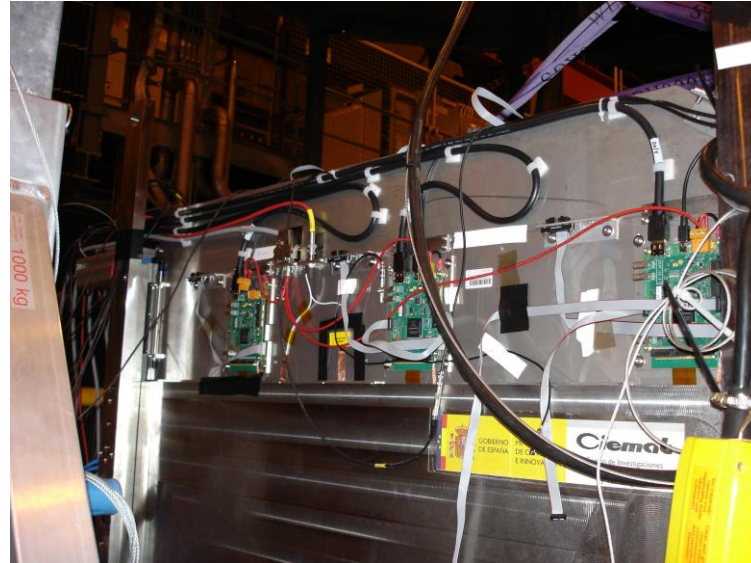


SDHCAL @ CERN Test Beams

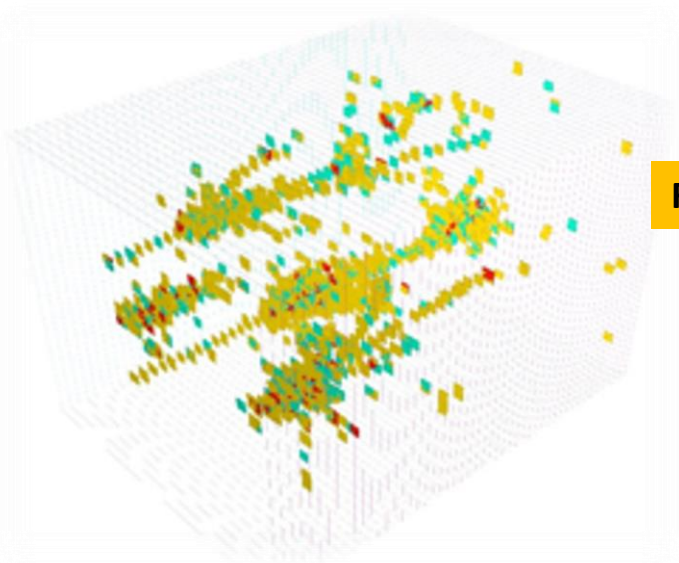


2009 –
initial
beam tests
with small
gRPCs

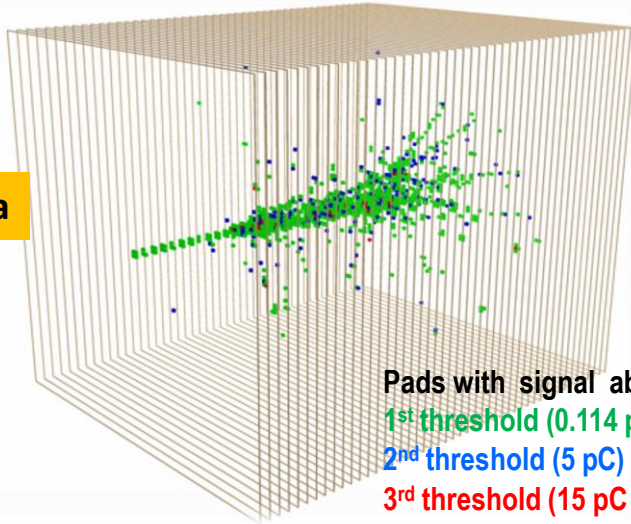
SDHCAL prototype
was exposed to
beam particles at
CERN PS, SPS in
2012, 2015,
2017, 2018 and
2022



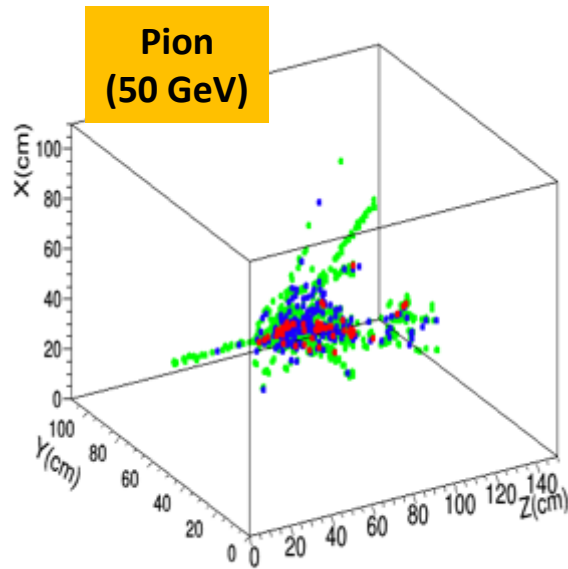
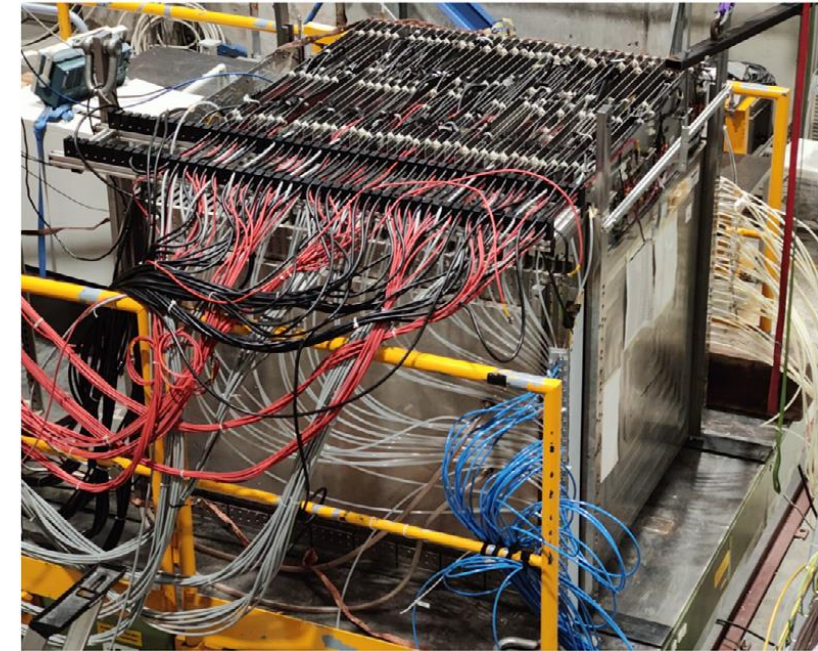
SDHCAL @ CERN Test Beams



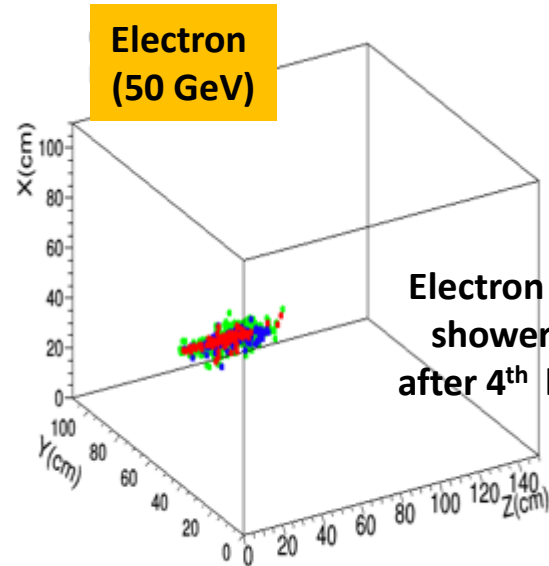
Raw data



Pads with signal above
1st threshold (0.114 pC)
2nd threshold (5 pC)
3rd threshold (15 pC)

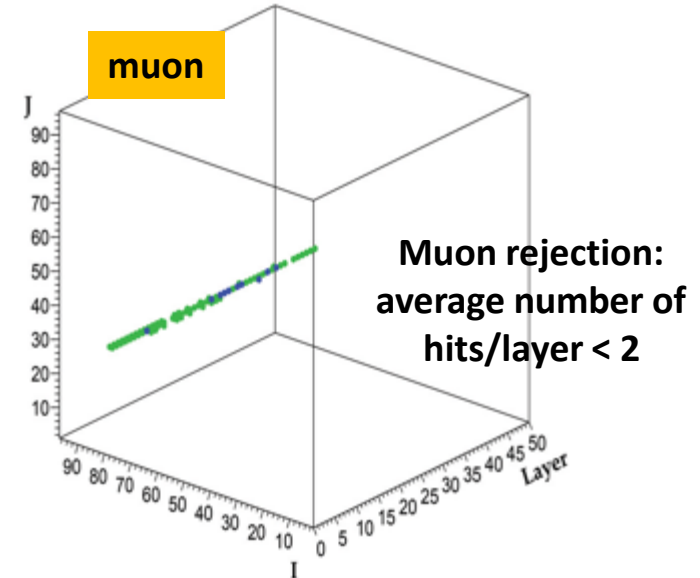


Pion
(50 GeV)



Electron
(50 GeV)

Electron rejection:
shower starting
after 4th layer ($6 X_0$)



muon

Muon rejection:
average number of
hits/layer < 2

Energy Reconstruction

$$E_{\text{rec}} = \alpha (N_{\text{tot}}) N_1 + \beta (N_{\text{tot}}) N_2 + \gamma (N_{\text{tot}}) N_3$$

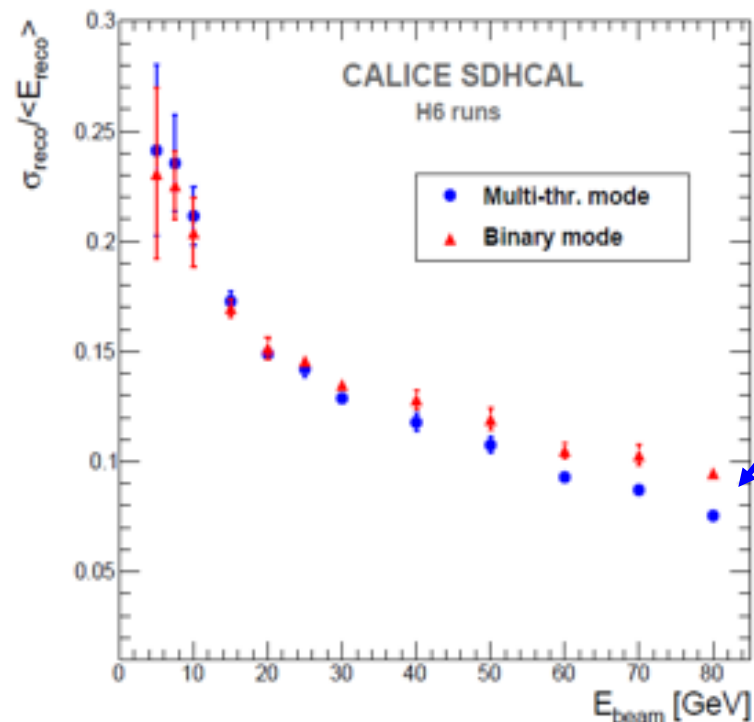
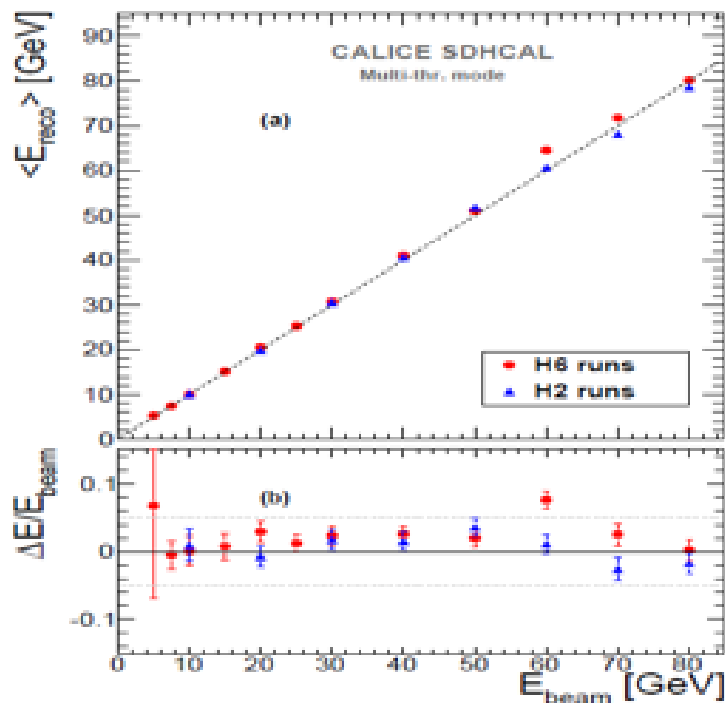
$$N_{\text{tot}} = N_1 + N_2 + N_3$$

N_1 = #pads with 1st threshold < signal < 2nd threshold

N_2 = #pads with 2nd threshold < signal < 3rd threshold

N_3 = #pads with signal > 3rd threshold

α , β , γ are quadratic functions of N_{tot} computed by minimizing $\chi^2 = (E_{\text{beam}} - E_{\text{rec}})^2 / E_{\text{beam}}$



multi-threshold mode (semi-digital) helps at high energy

JINST 11 (2016) P04001

Tracking within Hadronic Showers

Reconstruction of track segments associated to charged particles inside shower using 3D- Hough Transform technique

Avoid the dense shower core, by keeping only hits that have a small number of neighbours in the same detector layer.

Track segments allow in-situ layer efficiency and multiplicity studies, can help the PFA algorithm and can improve the energy reconstruction

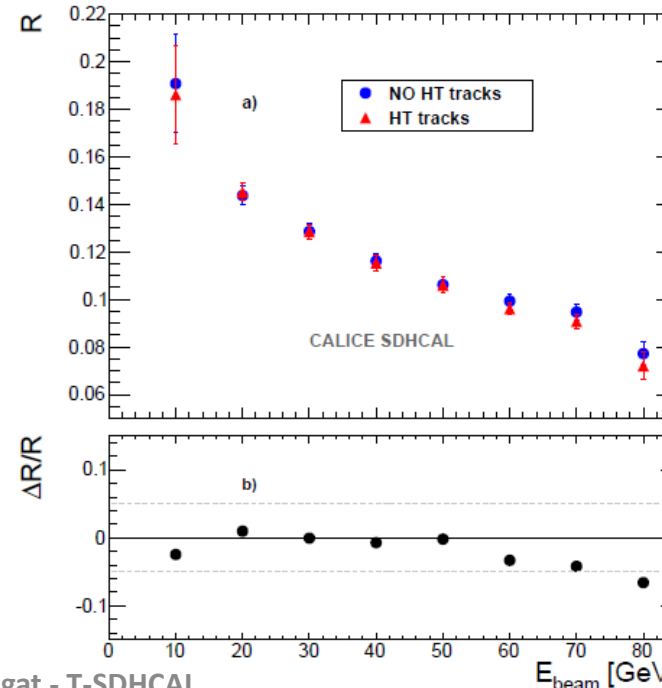
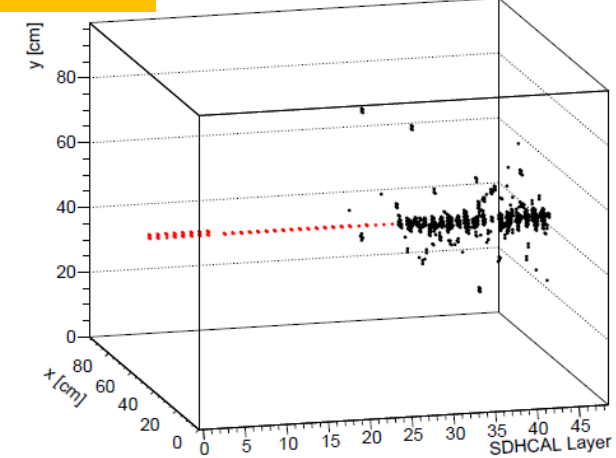
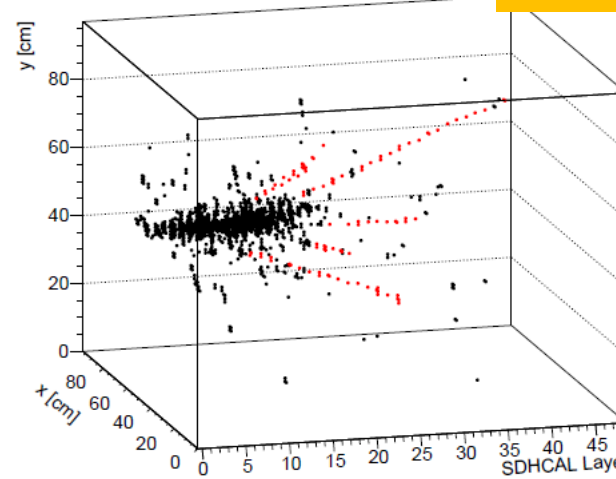
Low energy tracks may stop in calorimeter and create hits above 2nd or 3rd threshold, biasing the energy reconstruction

$$E_{rec} = \alpha (N_{tot}) N'_1 + \beta (N_{tot}) N'_2 + \gamma (N_{tot}) N'_3 + c N_{HT}$$

$$N_{tot} = N'_1 + N'_2 + N'_3 + N_{HT}$$

JINST 12 (2017) P05009

80 GeV pions



Slight improvement seen at high energy where 2nd and 3rd threshold play a role

Particle Identification

The high granularity of SDHCAL enable particle identification and allows one to discriminate pions, electrons and muons

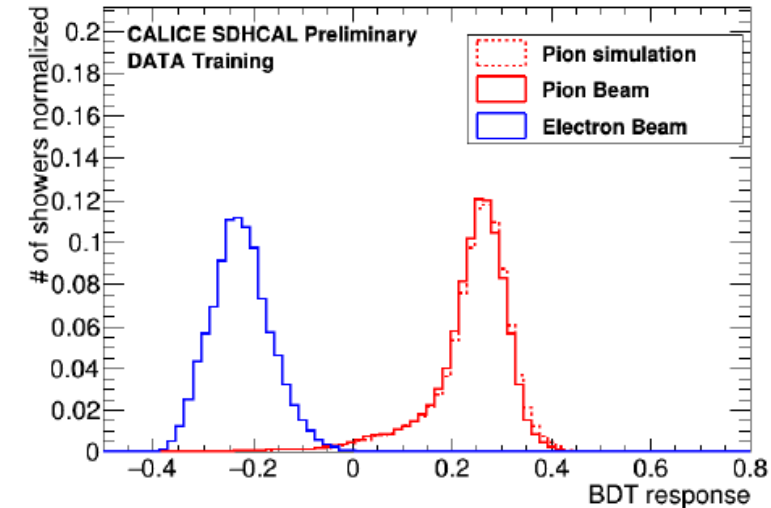
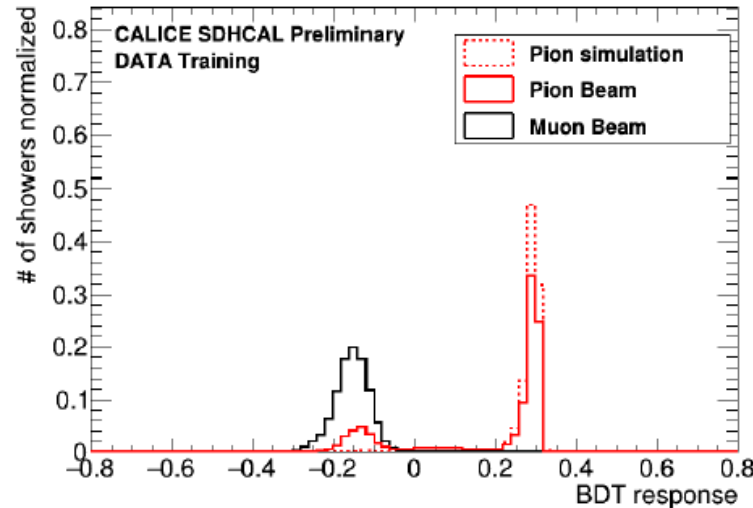
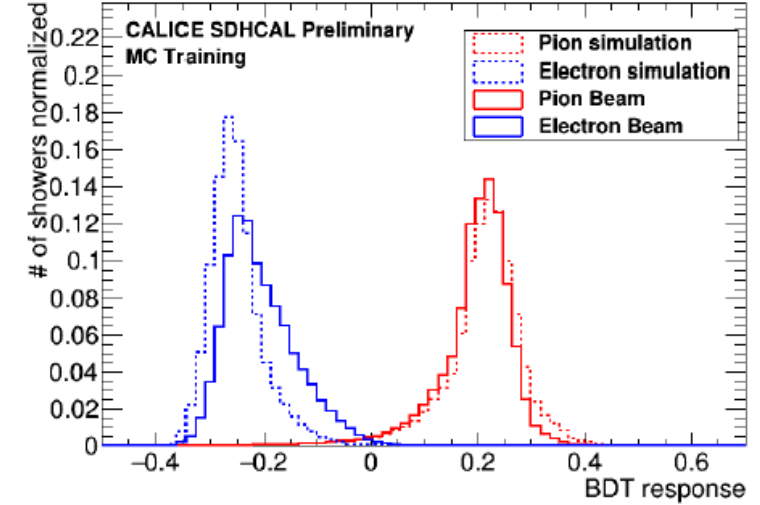
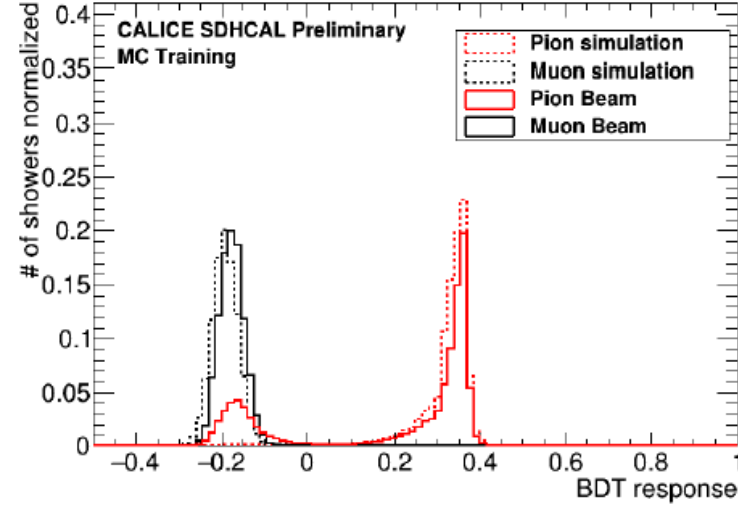
Discrimination power is well exploited using multi-variate analysis techniques: Boosted Decision Trees in our case

Two methods were used, using either

- simulation events
- pure electron and muon beam events for the training

BDT input variables: first layer of the shower, number of track segments in shower, shower density, shower maximum

...



JINST 15 (2020) P10009

Electron and muon rejection > 99%

B. Liu PhD thesis

From SDHCAL to T-SDHCAL

Overall performance of PFA algorithms depends on capability to associate calorimeter showers to tracked particles, and on the energy resolution of the calorimeters

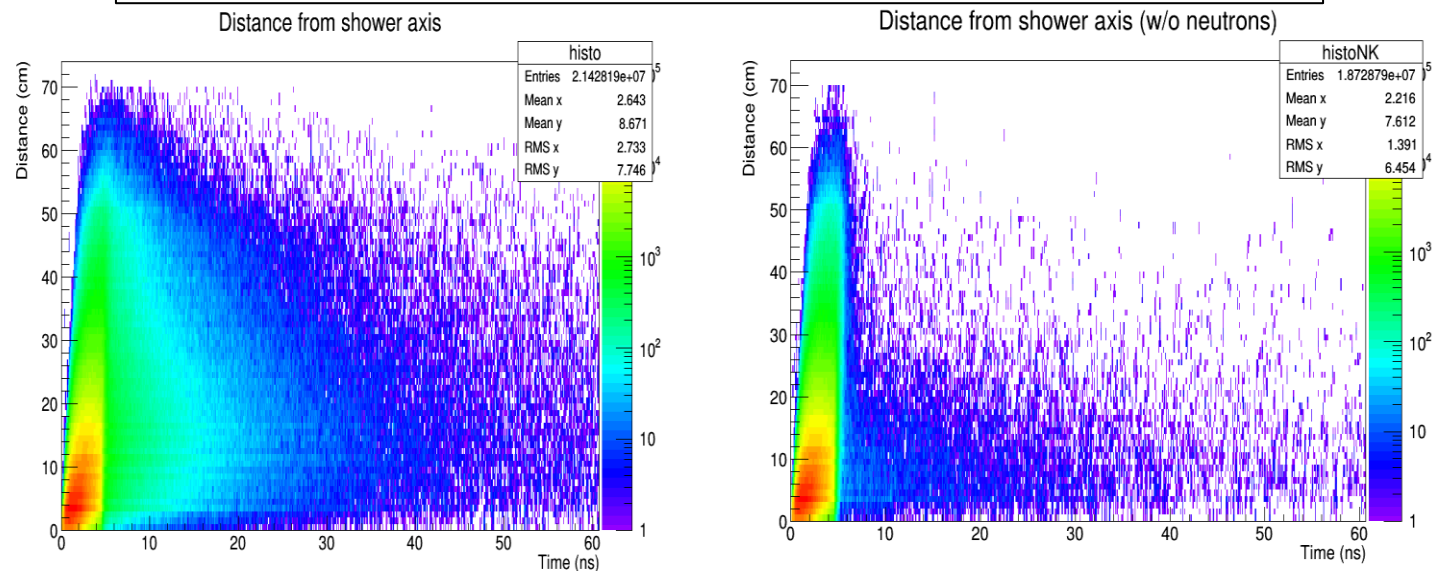
Timing capabilities of the calorimeter systems in collider detectors open up new possibilities in event and object reconstruction (TOF, LLP, shower reconstruction ...)

Hadronic showers show a complex time structure, with late components connected to neutron-induced processes

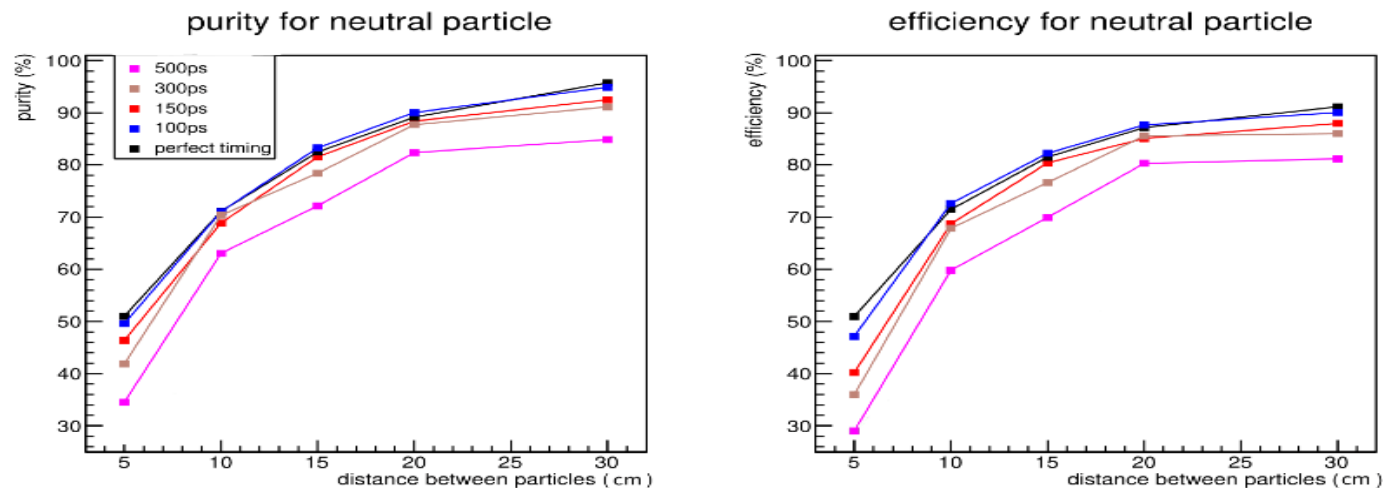
A time resolution on the order of a few 100 ps to 1 ns results in a sharper definition of the shower core

In addition, we found that time information could improve significantly hadronic showers separation at lower distances

Separate delayed neutrons for better energy reconstruction



Separation of close-by showers (e.g. 10 GeV neutral and 30 GeV charged particle)



Timing SDHCAL Project

- **Replacing the single-gap RPCs in SDHCAL with MRPCs**
 - Need to study how many gaps are needed to reach 100 ps, taking into account the cost on the cassette thickness.
- **Replacing the HARDROC ASIC with a new ASIC (continuous readout + Internal TDC)**
 - Started with PETIROC but we need to go further (Liroc+TDC)

SDHCAL was first developed for **ILC**, i.e. low rate and power pulsing, and needs to be adapted to cope with future **circular collider** requirements, i.e.

- Continuous readout
 - High particle rates
-
- **Developing a cooling system**
 - The cooling system should not add too much dead zone; could we use it with the present SDHCAL mechanics with limited efforts? Initial studies on this topic done
 - **Increase rate capability with low resistive materials**
 - low resistivity glass, PEEK doped with Carbon Nanoparticles

Developing Multi-gap RPC Prototypes

Glass resistivity $\sim 10^{12} - 10^{13} \Omega\text{cm}$

two times 4-gap
PCB inserted
between the two

1cm strip width



1x1m² chamber

Two times 3-gap
X-Y Strip

30x30cm²

Mylar spacers



Glass resistivity $\sim 5 \times 10^{12} \Omega\text{cm}$

Single stack of 5 gaps
X-Y Strip
4mm Strip width



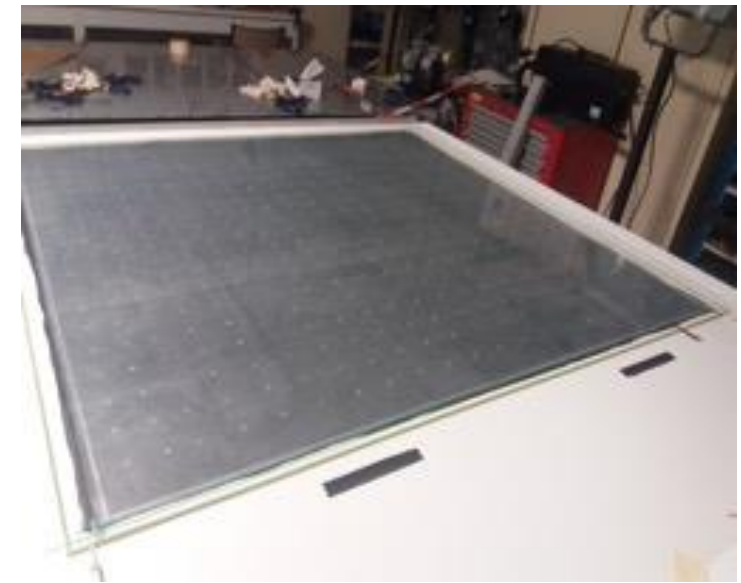
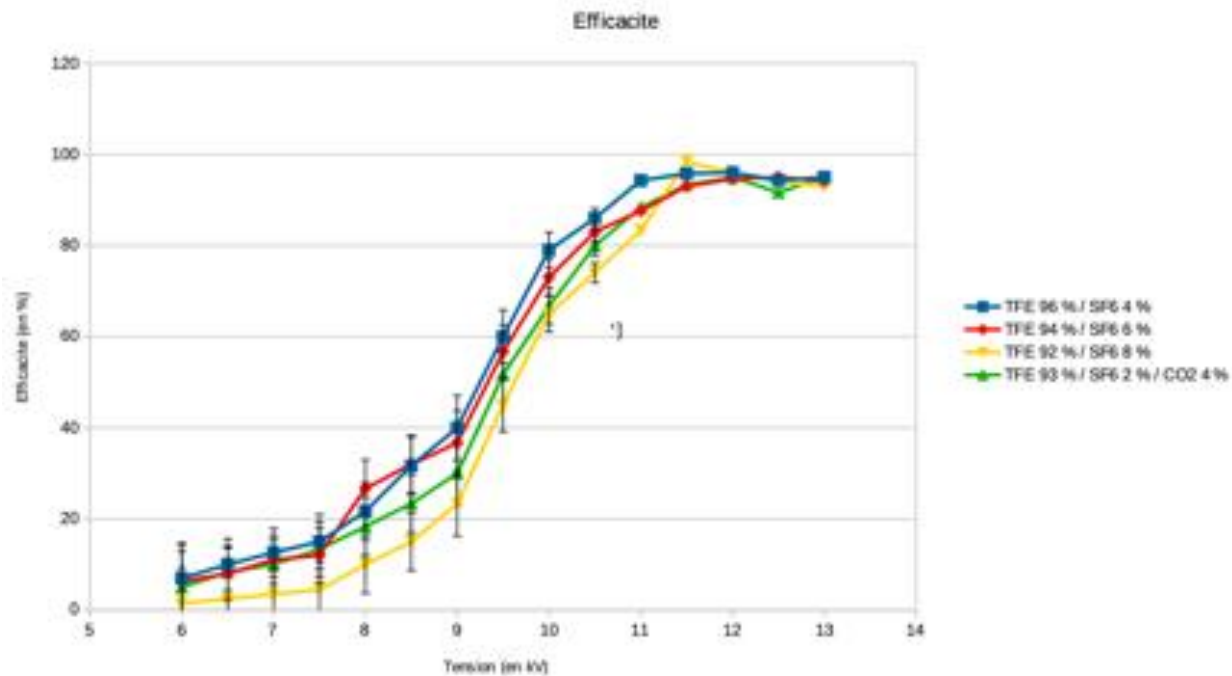
20cm x 20cm

$\varnothing 230 \mu\text{m}$ ceramic fishing line

Expecting less charge going to the fishing line

Multi-gap RPCs

- We built small and large 4-gap RPCs of 1 m² using **fishing lines**; efficiency > 92%
- We built small and large 4-gap RPCs of 1 m² using a new technique using **Mylar spacers** that renders the fabrication process very easy; first results show good efficiency (> 95%)



Electronics for T-SDHCAL

Present baseline solution



- 32 channels
- on-chip TDC
- Time resolution below 50ps

Pros: embeds preamp, TDC, QDC

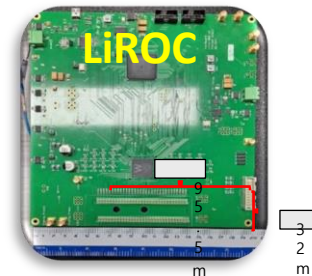
Cons: limited digital logic, difficult to chain, deadtime

Developed at CNRS-OMEGA partially thanks to AIDA2020 for CMS-muon upgrade

Medium/long term possible option



Board is under development by the WEEROC company



- 64 channels
- FWHM < 20 ps

Developed for SiPMs readout on LIDAR (*) No internal TDC



- 64 channels
- Time resolution < 12 ps

(*) LIDAR = Light Detection And Ranging

Electronics for T-SDHCAL

PETIROC was proposed for iRPC@CMS (see e.g. talk “iRPC front-end board readout electronics”, Maxime Gouzevitch”)

- Excellent performances are obtained with double-gap RPCs using pickup strips

→ A good candidate to start with for T-SDHCAL

Small PCBs with 1 cm x 1 cm pickup pads were conceived by SJTU in collaboration with IP2I and OMEGA to read out MRPC

FEB v1:

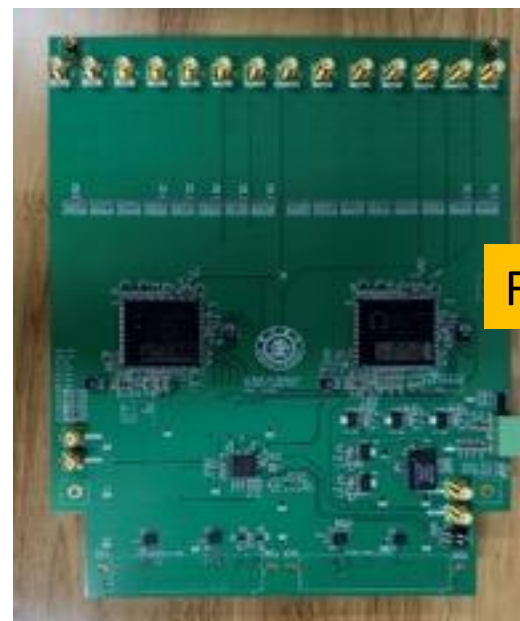
- 12 layer structure
- Laser-drilled via-in-pad
- Buried vias

FEB v2 has been designed and fabricated

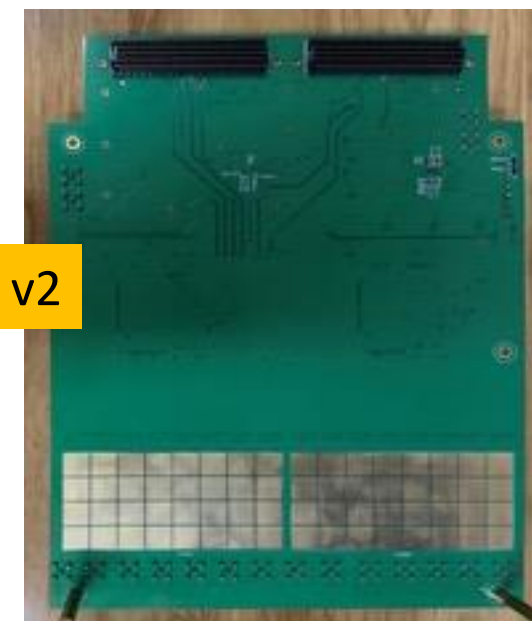
- 2 PETIROCs on-board
- Power rails designed on board
- 64-channel input pads
- SMA connectors to inject signals
- Crosstalk issue in injection tests has been fixed



FEB v1



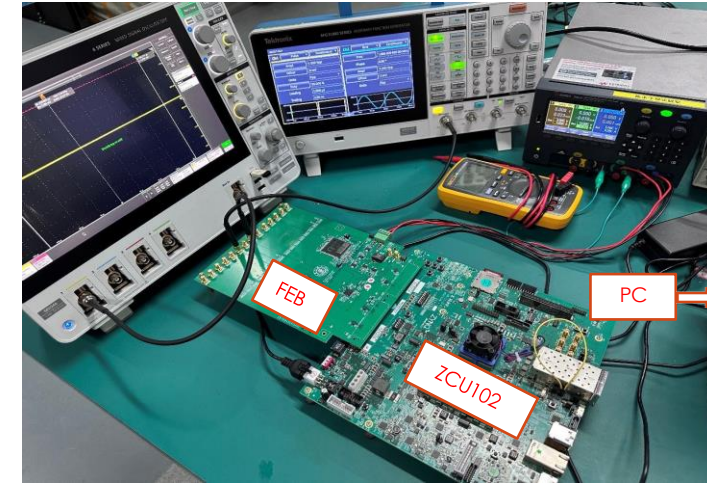
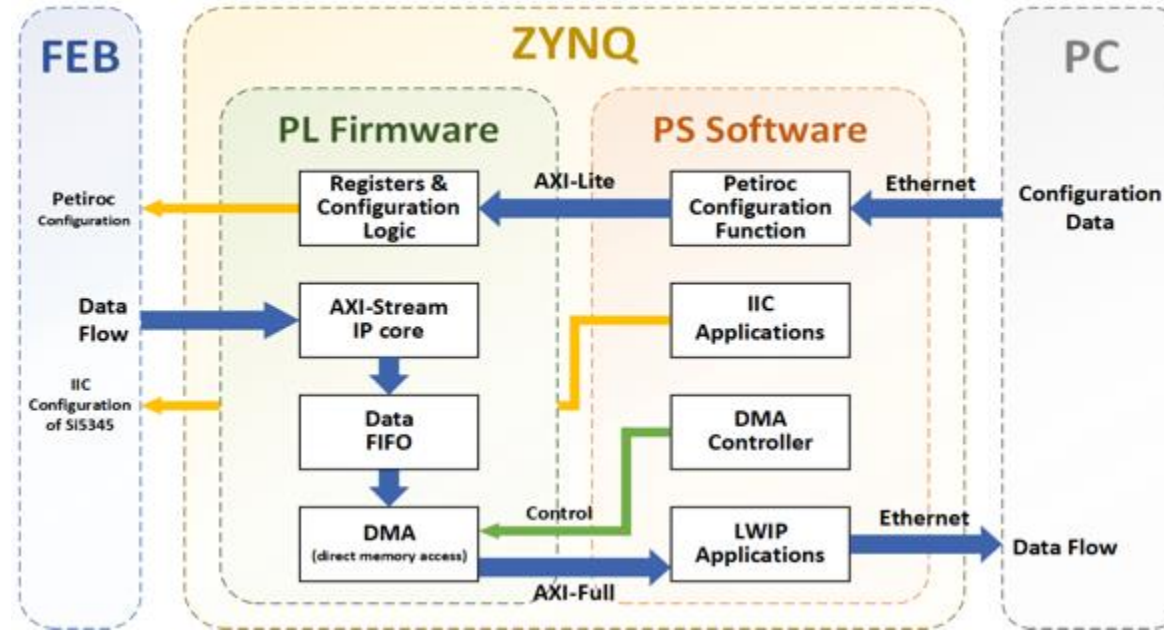
FEB v2



Data-acquisition

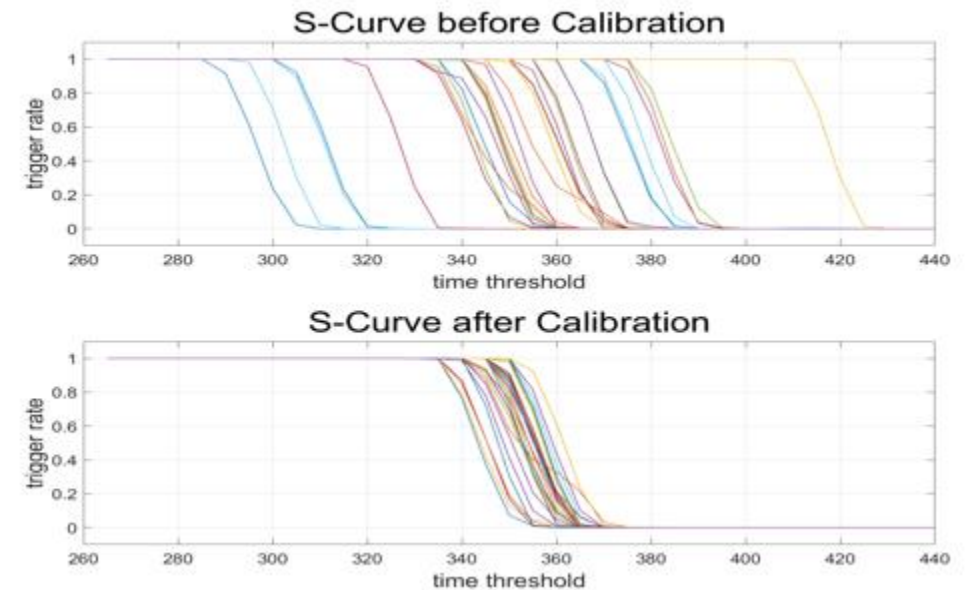
DAQ system based on commercial ZCU102 FPGA evaluation board with Zynq UltraScale+ System-on-Chip (SoC):

- Light-weight IP (LwIP) data transmission on processing system (PS)
- Other logic cores in programmable logic (PL) for configuration and data transmission



Software developed with Python and Qt5:

- 648-bit configuration data flow is sent through Ethernet
- Receive and decode data from FEB
- Tune the threshold of each PETIROC channel (through 6-bit DAC) to enhance the uniformity
- After calibration RMS of 50% trigger rate threshold reduces from 25.3 DAC to 4.56 DAC



Injection Tests for Timing Evaluation

Two tests were performed with function generator, i.e. single channel injection and coincident signal injection

(i) single channel injection

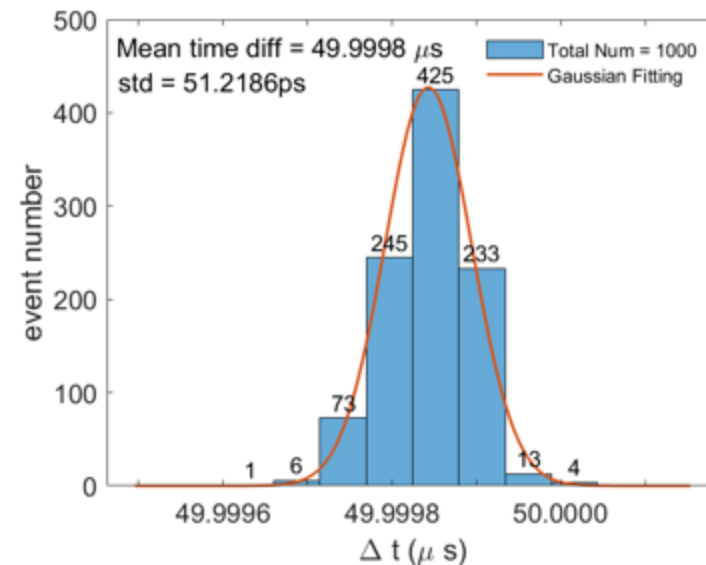
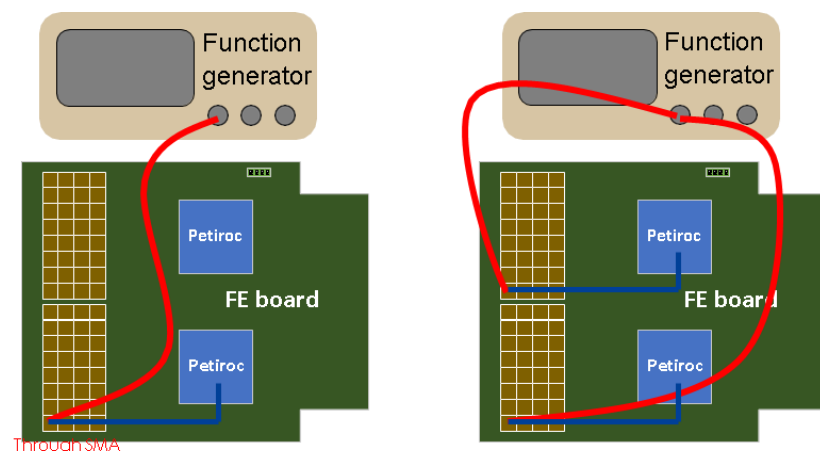
Inject periodic signal into one channel and measure the time differences of two consecutive hits to get the intrinsic time resolution

$$s_t = 36 \text{ ps}$$

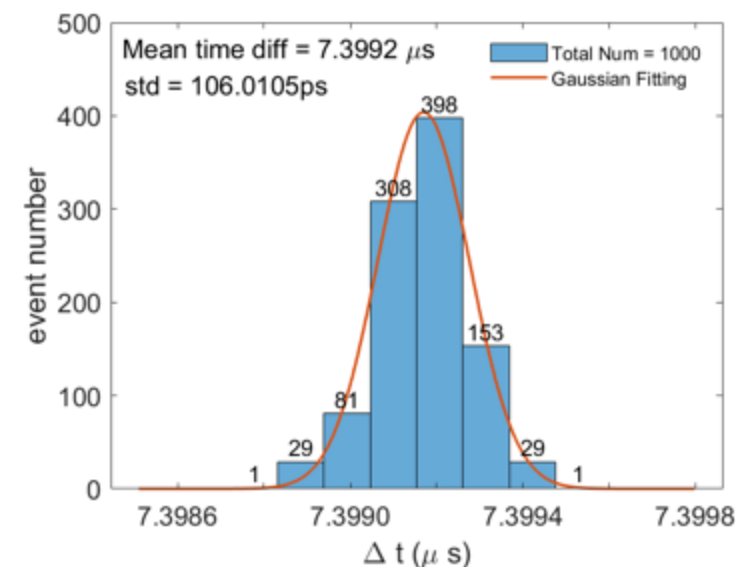
(ii) coincident signal injection

Inject identical signal into two ASICs, measure the time differences of the identical hits between two ASICs and get the time resolution between ASICs

$$s_t = 75 \text{ ps}$$



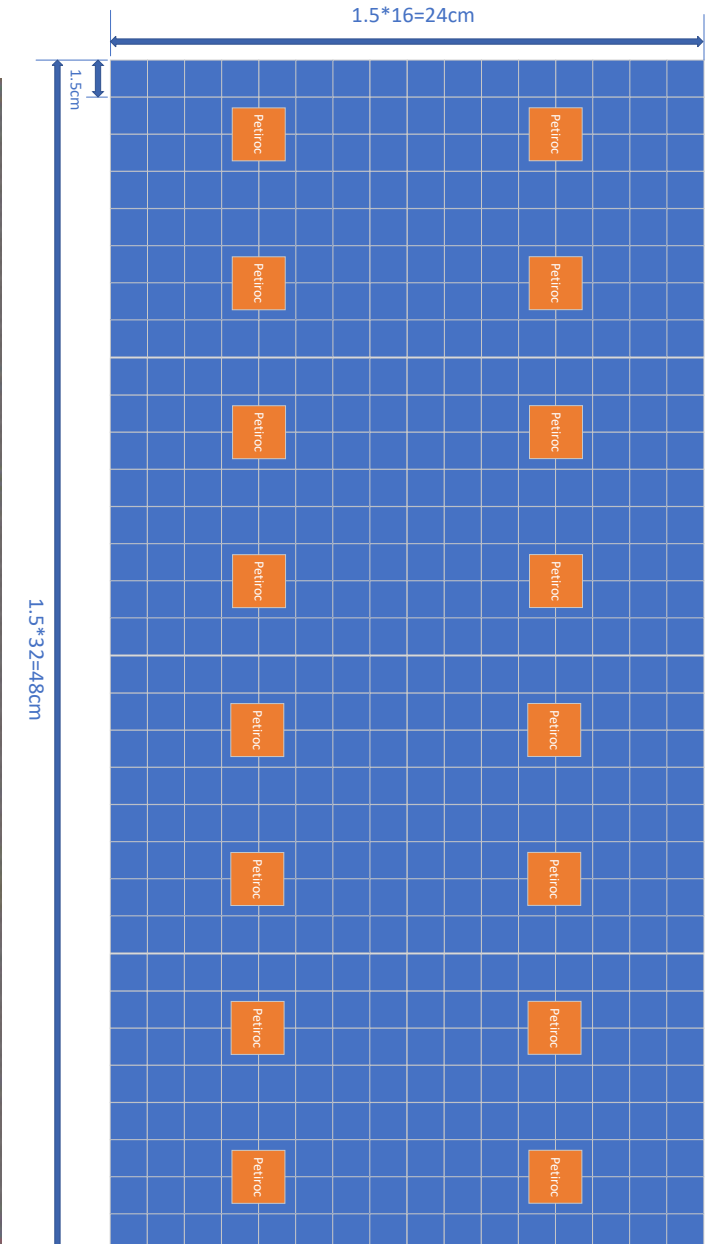
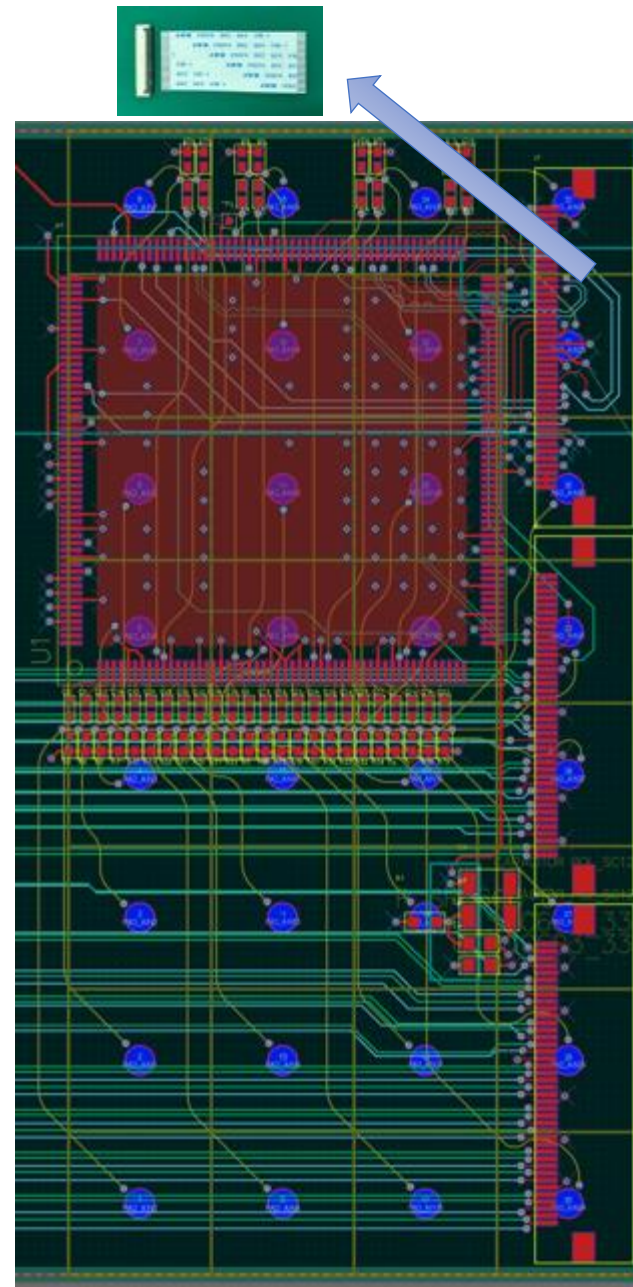
Single channel injection



Coincident signal injection

Ongoing Activities

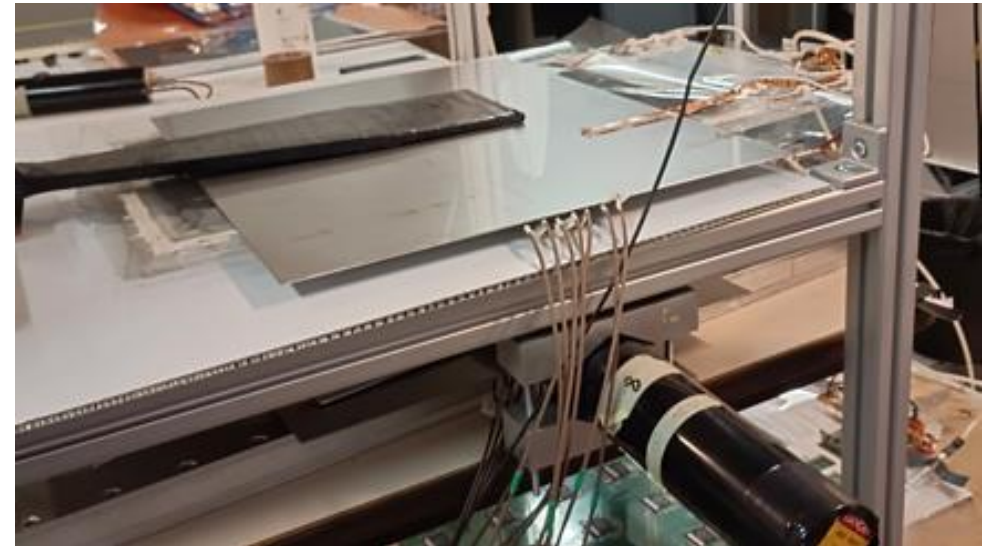
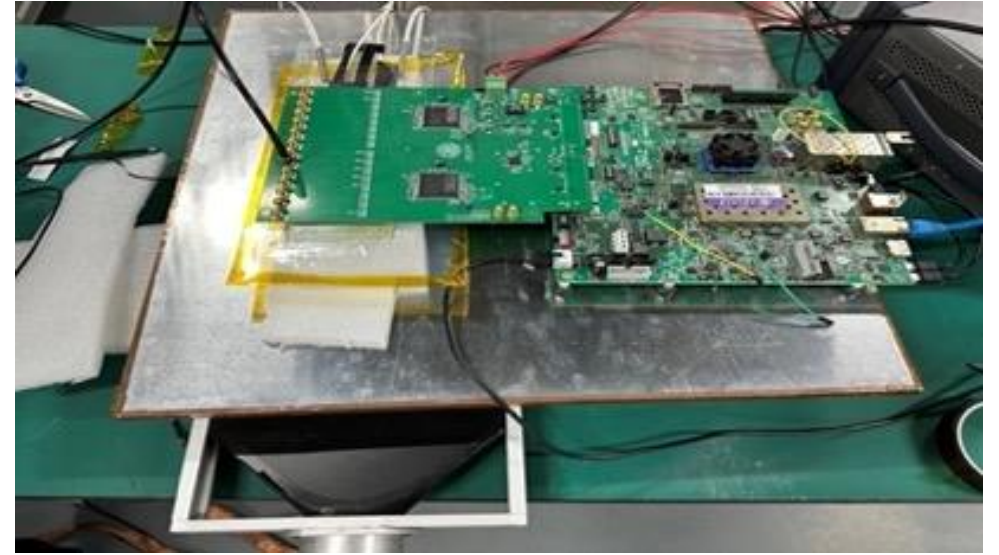
- The idea is to design two boards that can be linked together with tiny connectors
- Each board houses 16 PETIROCs (512 channels)
- Board size is about 24 cm x 48 cm, i.e. 4 pairs of these boards can cover 1m² area
- The readout pads are designed to be 1.5 cm x 1.5 cm, so that it is possible to layout within 10 layers
- Current evaluation boards will be replaced with Alinx core boards



Ongoing Activities

- 2 small MRPC were built in Lyon and sent to Shanghai to be tested with the new FEB v2 and others, with different gas gaps configurations to be built and sent soon

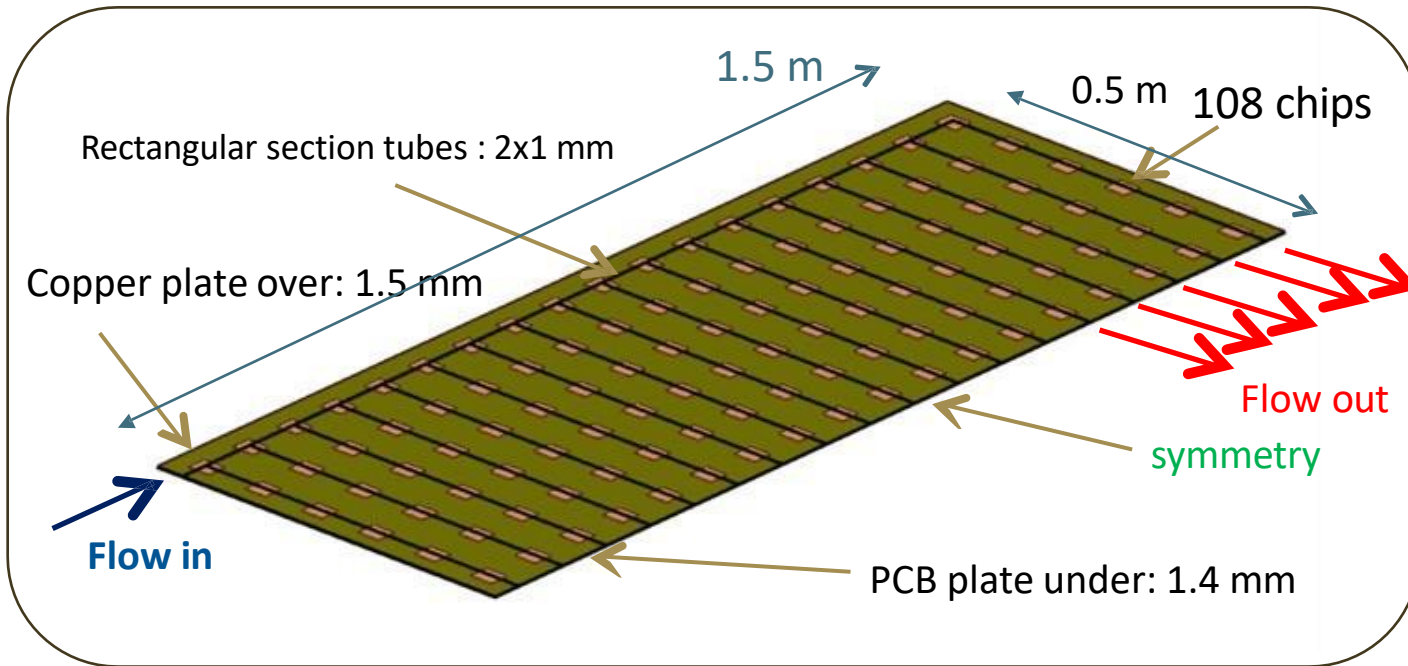
- Tests with PETIROC on medium-size chambers (50 cm x 35 cm) with 3, 4 and 5 gas gaps, using pickup strips are ongoing; PETIROC test board of OMEGA will be used



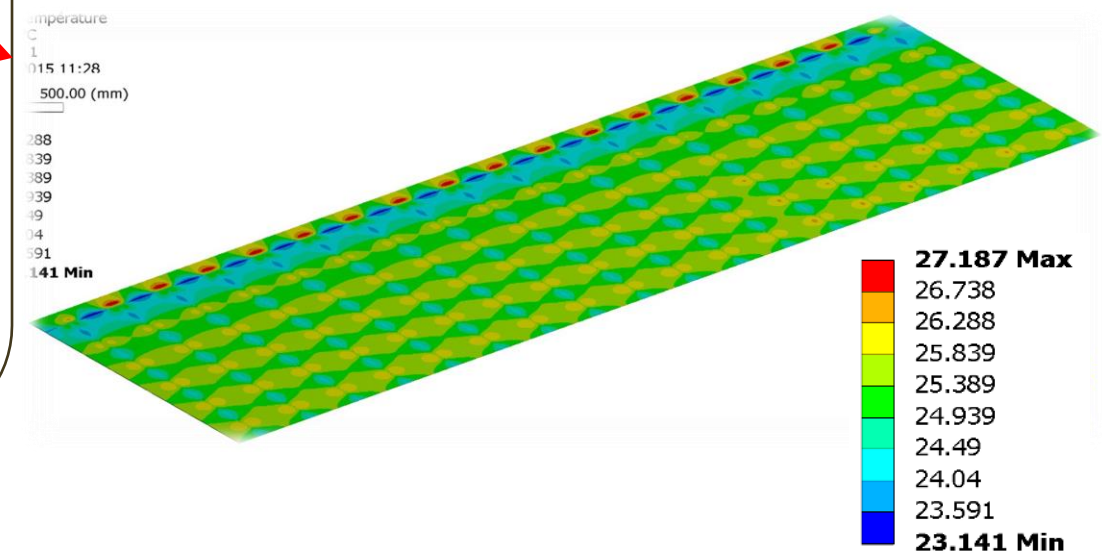
Cooling System

In contrast to ILC, **CEPC/FCC-ee will not allow power pulsing for SDHCAL**, i.e. power consumption increases by factor 100-200 and active cooling will be needed:

- Previous studies were performed on HARDROC (full regime) showed efficient heat absorption using water circulating in Copper tubes in contact with the ASICs
- redo the studies with the new ASICs and the mechanical structure in mind



Simulation with HARDROC electronics
To be redone with the new ASICs



A simple cooling system based on water circulating into Copper pipes designed

High Rate Capability

Low resistivity materials will be used for the future MRPCs

Doped low-resistivity glass developed by Tsinghua U.

→ problem with the glass thickness

Low-resistive PEEK ($10^{8-9} \Omega \cdot \text{cm}$) developed by IP2I-Lyon with help of Krefine company; doped with Black Carbon

→ Some efforts to reach better homogeneity is needed but no thickness issue here



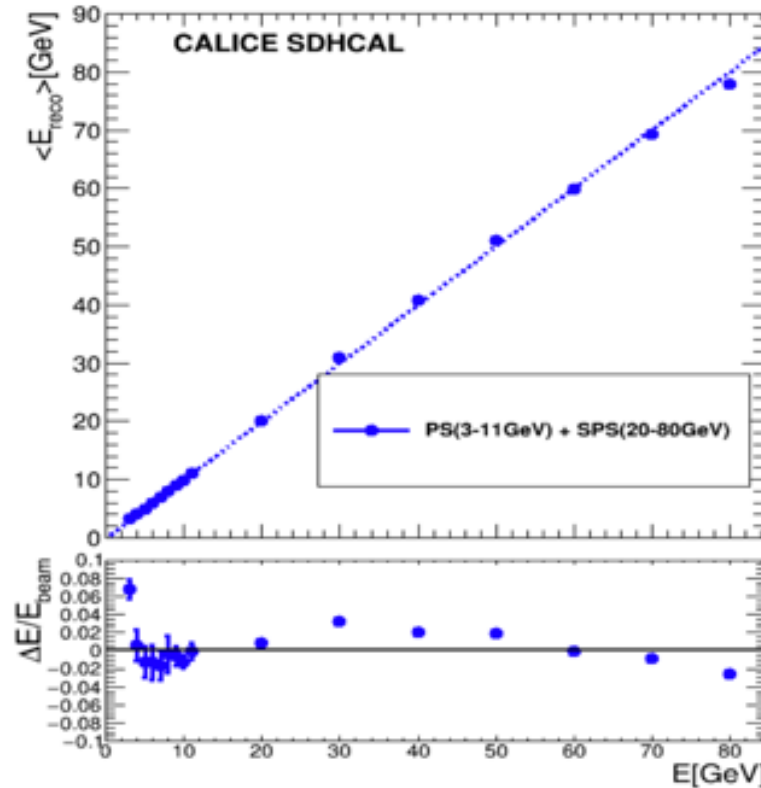
Summary

- T-SDHCAL is an excellent calorimeter candidate for a future Higgs factory detector
- T-SDHCAL is recognized as an important project and is part of the DRDs activities
 - ❑ DRD1
 - WP5 on Calorimetry
 - WP7 on Gaseous Timing Detectors: high-rate, large, precise timing (M)RPC, but also MPGD (PICOSEC, FTM), $\mathcal{O}(100/\text{ps})$
 - ❑ DRD6
 - WP1 on Sandwich calorimeters with fully embedded electronics
- Many efforts are still needed to show that T-SDHCAL can achieve its goals
- Construction of a few cassettes with MRPC equipped with timing electronics will be the first step
- The MRPC cassettes will replace some of those of the SDHCAL prototype to show the impact of time resolution on the hadronic shower reconstruction

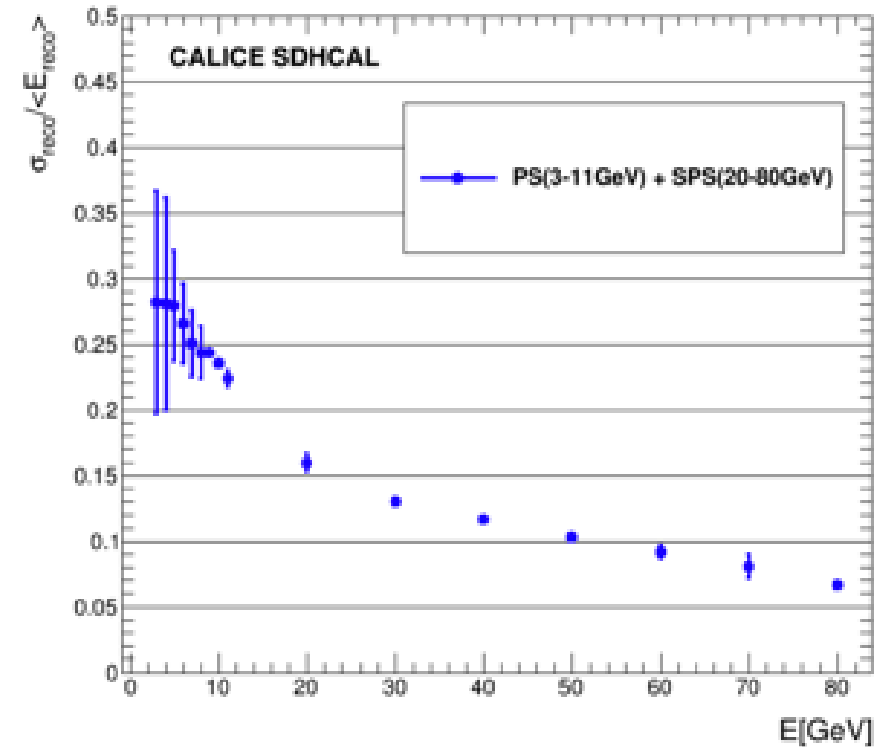
BACKUP

Energy Reconstruction

The energy reconstruction technique was successfully applied to both low energy (PS) and high energy (SPS) hadrons



Linearity



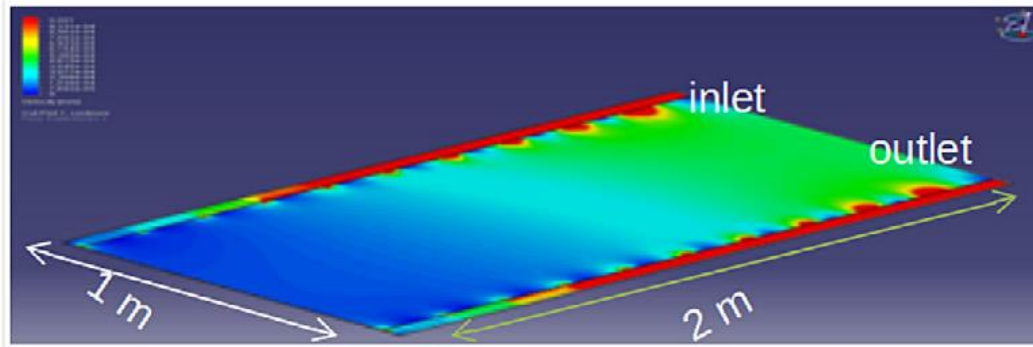
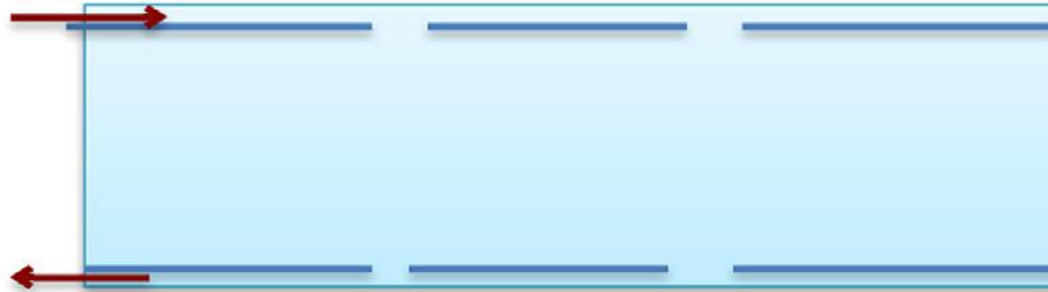
Energy resolution

JINST 17 (2022) P07017

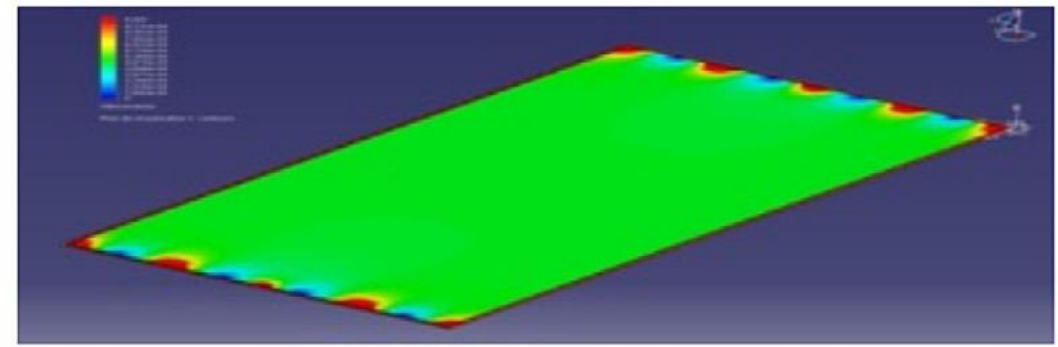
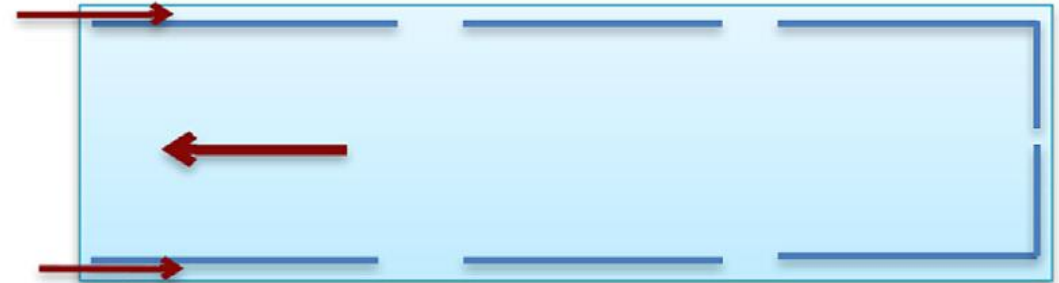
B. Liu PhD thesis

Gas Circulation in Large-Size Chambers

Current system



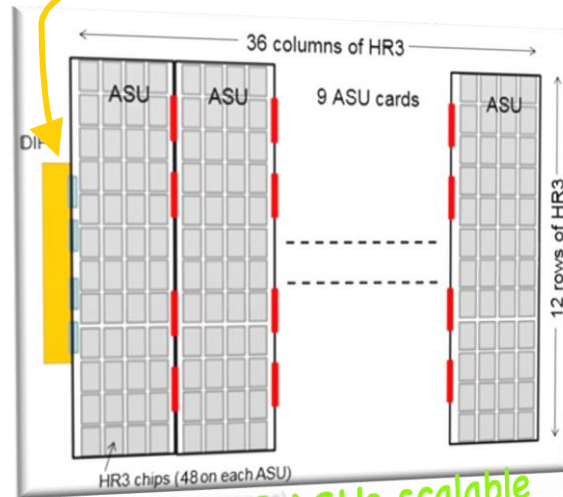
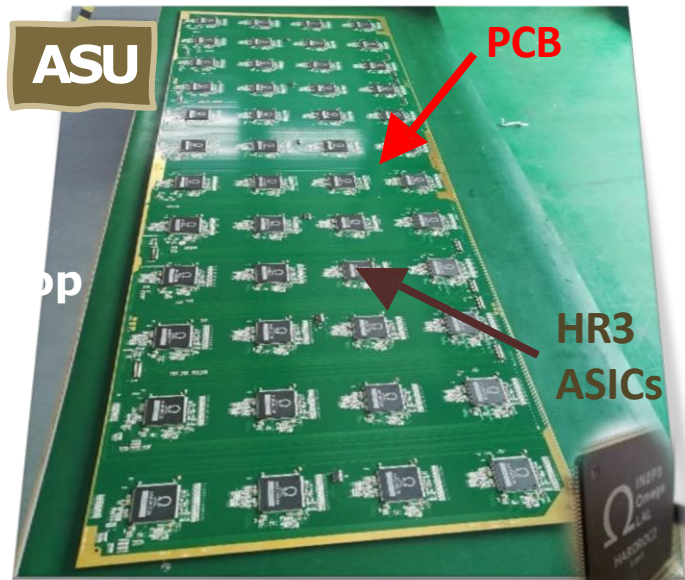
New system



Challenges: Electronics

- ⌚ Electronics must be compact despite the huge number of channels → Embedded in the calorimeter
- ⌚ Homogeneous response → Stringent planarity requirements for PCBs to insure homogeneous contact of pads with RPCs
- ⌚ Lower power consumption → Power pulsing for linear colliders, more developments needed for circular

Best 13 layer PCB option found up to 1x0.33 m²

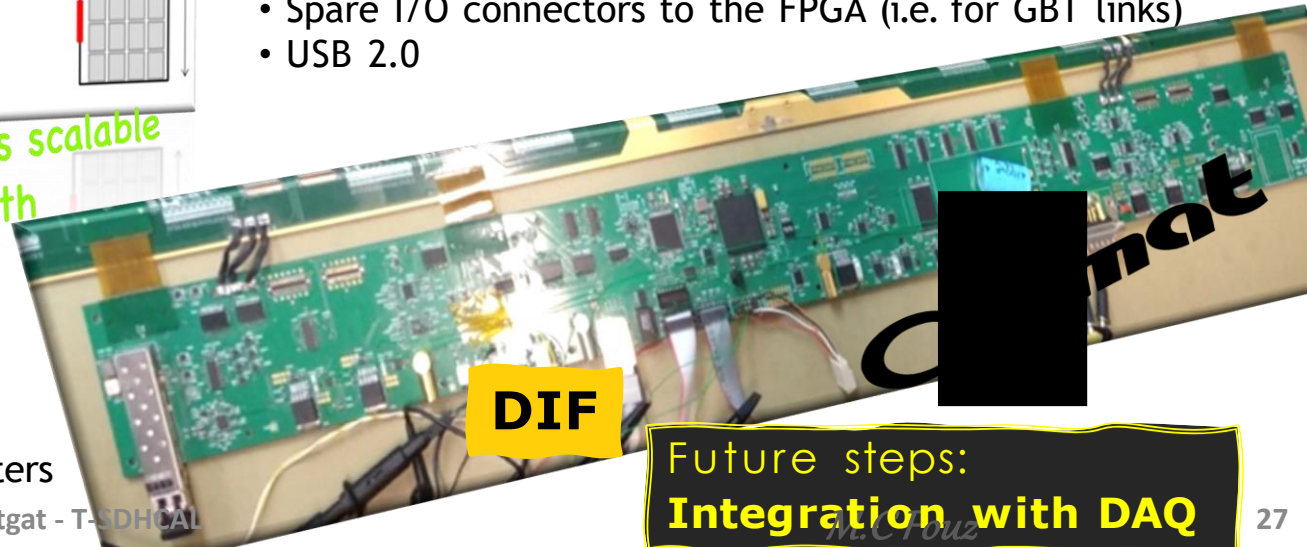


DIF (Detector InterFace)

Sends DAQ commands (config, clock, trigger) to front-end and transfer their signal data to DAQ.

- 1 DIF per RPC plane handle up to 432 HR3 chips
- HR3 SC through I2C bus (12 IC2 buses).
- Data DAQ transmission by Ethernet
- Clock and synchronization by TTC (also used in LHC)
- Spare I/O connectors to the FPGA (i.e. for GBT links)
- USB 2.0

Number of ASUs scalable with GRPC length



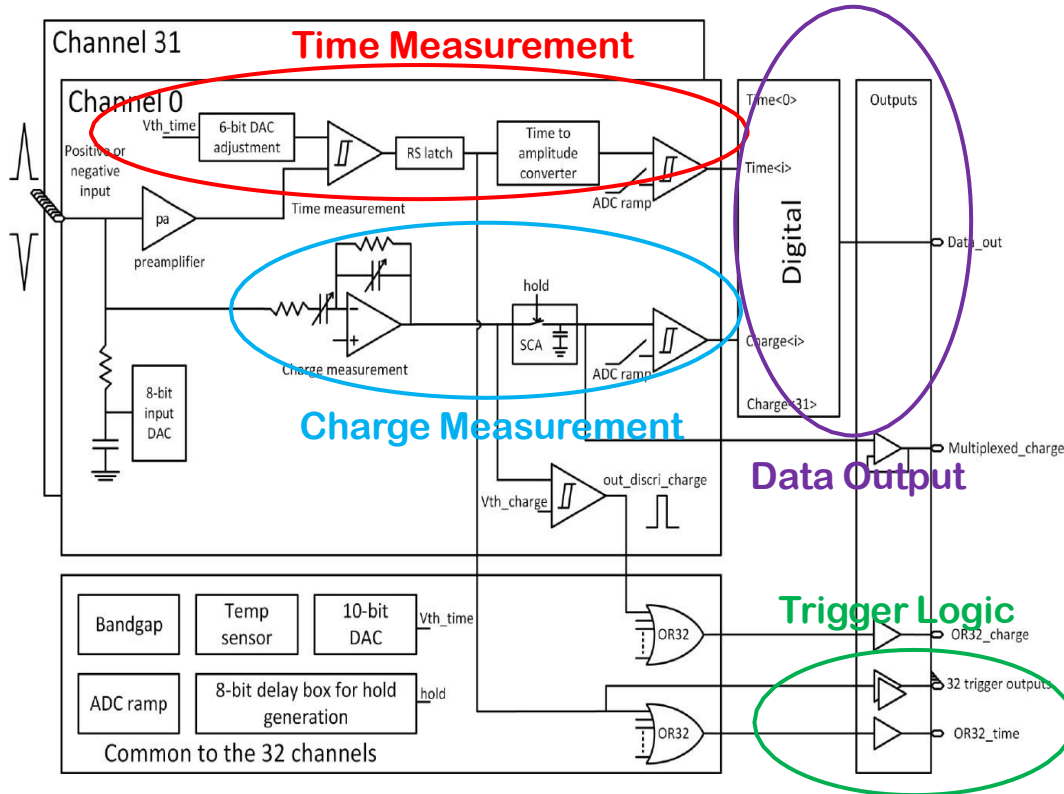
DIF

Future steps:
Integration with DAQ

Bottom
1 pad = 1cm²,
Inter-pad 0.5 mm

HADROC3
Independent channels
Zero suppress
Extended dynamic range (15fC to 50 pC)
I2C link with triple voting for SC parameters
packaging in QFP208, die size ~ 30 mm²

PETIROC ASIC



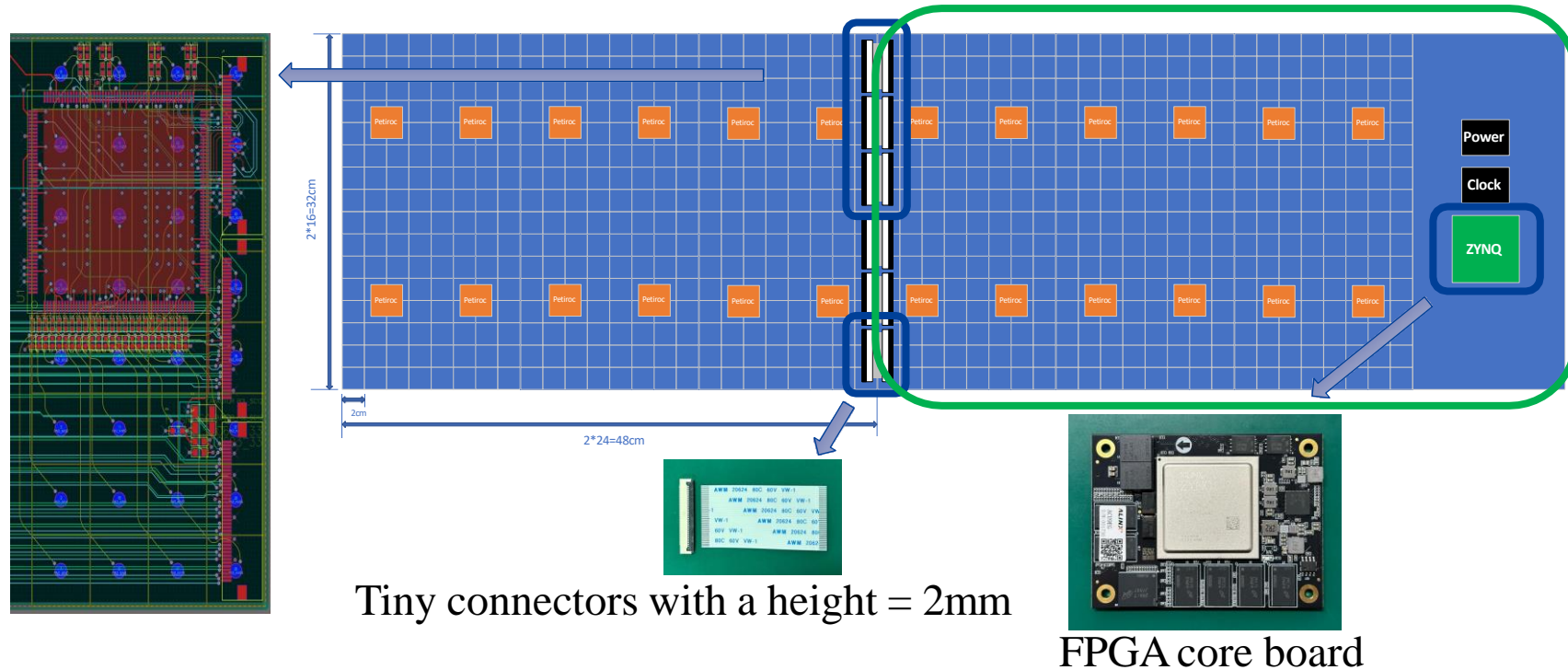
- A 32-channel front-end ASIC designed for SiPMs readout
- Charge and timing measurement
- 40 ps bin size of on-chip TDC
- Readout time: 12us
- Fast trigger line output
- Dynamic Range 0-480 pC i.e. 3000 photoelectrons @ 10^6 SiPM gain
- Power consumption 6mW/channel

Ongoing Activities

Large-size prototype

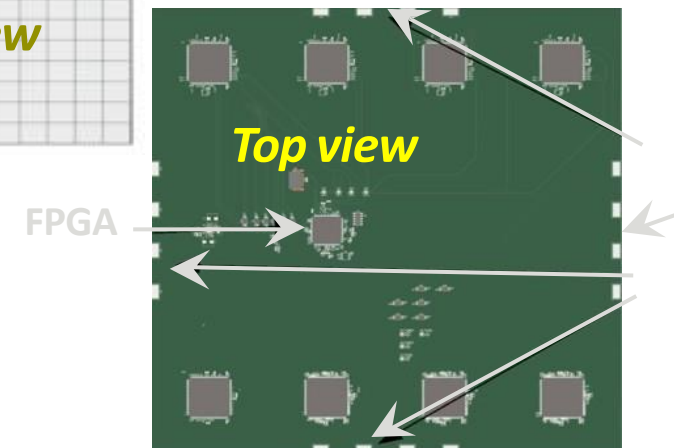
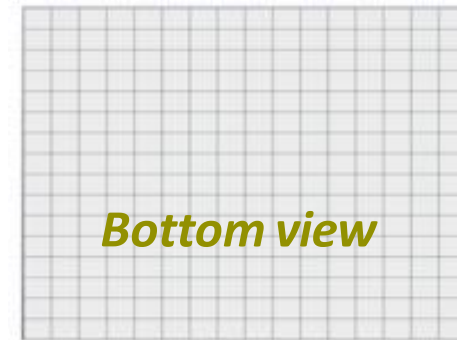
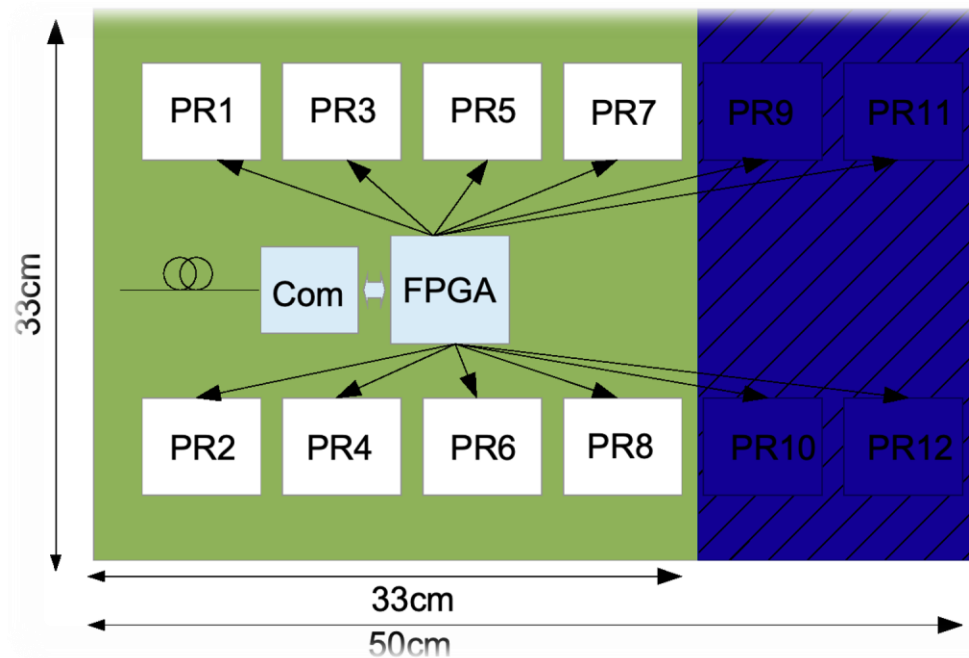
Design two boards, which are connected together by tiny connectors:

- Length of each PCB board should be $<75\text{cm}$, limited by the PCB technology
- $2\text{cm} \times 2\text{cm}$ readout pads
- Each PCB board hosts 12 PETIROCs (384 channels)
- Size is about $32\text{ cm} \times 48\text{ cm}$, i.e. 3 pairs of these boards to cover 1m^2



Electronics for timing calorimeter

- Board with 8 (could be extended to 12) Petircoc2B ASICs
- Pads 2cm x 2cm, 256 channels (to decrease the cost for prototyping)
- Local FPGA (Xilinx Spartan-6 TQFP) embedded on board



High Precision Mechanics

Procedures developed with **roller leveling** for improving planarity of absorber plates (1x3m²) from several mm to ~500 microns

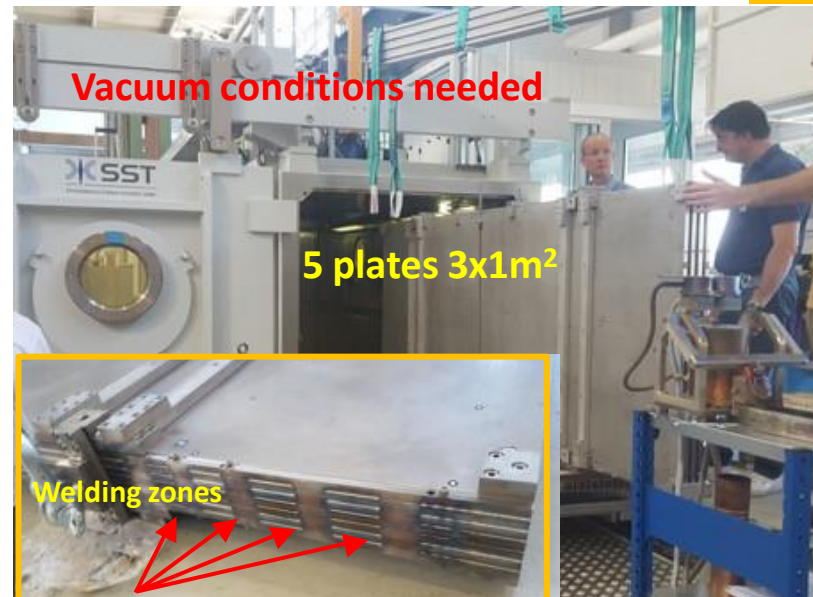
Development of **Electron Beam Welding** assembly protocols to reduce deformations introduced by welding procedures to below mm level (600 microns in this test with 5 plates 3x1 m²)

Larger modules (more plates), i.e. bigger machine needed & complicated handling (heavy structure to be moved and rotated several times)

Possible option is to **build sub-modules and afterwards weld them using laser welding**; the procedure should introduce reasonable deformations (the rigidity of the modules is much higher than for individual plates)



CIEMAT



New RPC Ecog-friendly Gases

The CERN gas group has identified friendly gases to replace TFE and SF6 for (M)RPC

TFE → HFO1234ze

SF6 → Novec 4710 (not good for Bakelite but ok for GRPC and MRPC)

Techniques of recycling the gas mixture is being constantly improved (>90%)

Techniques to recover the different exhaust gases (distillation...etc) are being developed and promising results have been obtained

T-SDHCAL in DRDx

SDHCAL was developed over the years within **CALICE**

T-SDHCAL work started within **DRD1 on Gaseous Detectors** and **DRD6 on Calorimeters**

DRD1: WP5 on Calorimetry

<https://drd1.web.cern.ch/wp/wp5>

conception, construction and characterization of large sampling elements for calorimeters ; timing performance of gaseous detectors for calorimeters; readout electronics for calorimeter gaseous detectors; high-rate capability gaseous detectors for circular collider calorimeters

WP7 on Gaseous Timing Detectors: high-rate, large, precise timing (M)RPC, but also MPGD (PICOSEC, FTM), $\vartheta(100/\text{ps})$

<https://drd1.web.cern.ch/wp/wp7>

optimize the amplification technology towards large-area detectors; enhance timing performance (number of gaps and sizes); enhance rate capability (low resistive layers); spatial resolution and readout granularity; stability, robustness and longevity; material studies (resistive layers); gas studies for precise timing applications (eco-gases); modelling and simulation of timing detectors; readout electronics for precise timing; precision mechanics and construction techniques; common framework and test facilities for precise timing R&D

DRD6: WP1 on Sandwich calorimeters with fully embedded electronics

<https://cds.cern.ch/record/2886494/files/DRD6-cdscern.pdf>

Hadronic section with gaseous readout: **(T-)SDHCAL**, MPGD-HCAL, ADRIANO3

