Contribution ID: **16** Type: **not specified**

iRPC front-end board readout electronics

Monday 9 September 2024 13:10 (20 minutes)

Advanced front-end electronics are designed for the new improved RPCs of CMS experiment to cope with the HL-LHC era challenges. The front-end electronics (FEB) are equipped with a new ASIC, iRPCROC, which reads the strips and digitises incoming signals, triggering the Cyclone V FPGA to stamp the time of each signal accurately. This electronics was developed to read out the RPC detectors from both ends of a signal strip, using timing information to identify the position along it. The challenges and successful performance of the FEB in nominal conditions, as well as the mass production details will be presented.

Author: GOUZEVITCH, Maxime (Centre National de la Recherche Scientifique (FR))

Presenter: GOUZEVITCH, Maxime (Centre National de la Recherche Scientifique (FR))

Session Classification: HEP performance (part II)