DAQ Control Signal Codec for Time of Flight AFP Detector

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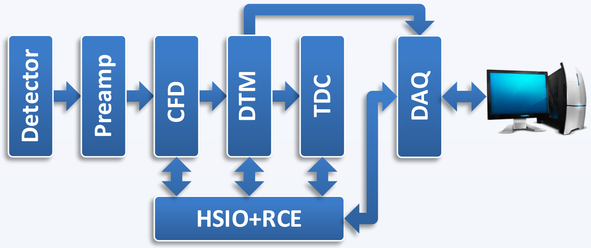
INTRODUCTION

The AFP Time-of-Flight (ToF) detector is located at LHC in CERN. Its main purpose is to measure the time delay of the detected high-energy protons during the multiple proton-proton collisions. Data acquisition (DAQ) system is the key component dedicated to data collecting and storing at different stages of the particle detecting system.



The depicted ToF detector consists of following blocks:

- Cherenkov particle detector - 4×4 quartz & photomultiplier
- 2 stages of preamplifiers
- Constant Fraction Discriminator (CFD)
- Digital Trigger Module (DTM)
- Time-to-Digital Converter (TDC)
- Data Acquisition System (DAQ)
- High-Speed I/Os & Reconfigurable Cluster Element (HSIO, RCE)

OBJECTIVES

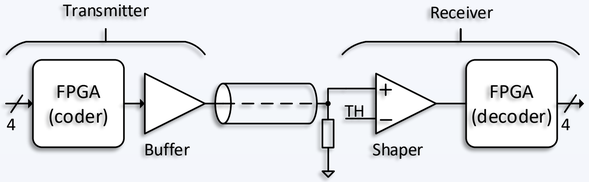
The aim is to develop the reliable system that is able to code, transmit and decode the commands sent from DTM to DAQ. In principle the device can be considered as a pair of fast parallel/serial and then serial/parallel converters. The device requirements are following:

- Coding of the 4 input signals (according to the activities of the DTM trains 1, 2, 3, 4) to the 5-bit data frame (start bit is added).
- Sending the data frames via 265 m low-loss coaxial cable (i.e. fast buffer is needed).
- Processing of the input signals up to 40 MHz rate.
- Recovering and decoding of the received signal.
- Rad hard and compact design.

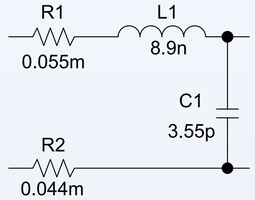
DEVICE ARCHITECTURE

The overall Codec architecture depicted below is composed of three main parts:

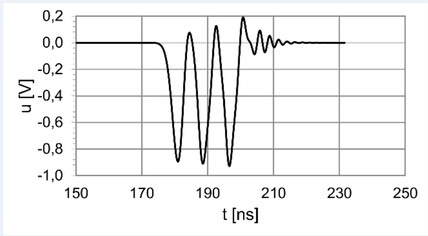
- Transmitter – FPGA coder and fast cable buffer
- Transmission line – 265 m of low loss coaxial cable
- Receiver – termination, shaper, FPGA decoder



The clock signal used for the coder FPGA is set to 400 MHz. The coax capacity is significant due to its 265 m of length and therefore the cable buffer design becomes critical.

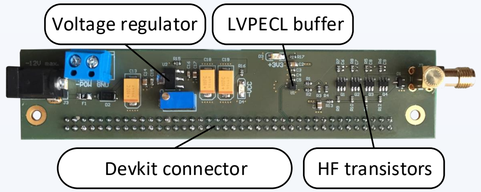


The PSPICE simulation of the data frame transmission was performed as a first step. Twenty transmission line elements (depicted above) were used per 1 m of cable. The figure below shows the waveform for 50 m of length. This simulation used the ideal NIM signal source (i.e. 0 mA/-16 mA) and 50 Ω cable termination. The propagation delay is approx. 180 ns as expected. No significant reduction in amplitude. The theoretical bit length is 2.5 ns (i.e. 400 MHz).



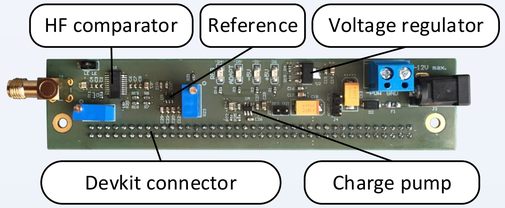
The high-speed output buffer depicted below consists of:

- LVPECL buffer sourcing the output HF transistor stage
- HF transistor-based output buffer including pre-emphasis
- Negative LDO regulator necessary to get the NIM levels
- Connector to the FPGA devkit used as a coder

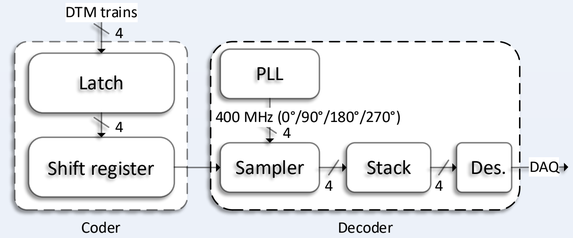


The following picture shows the receiver board. Its main components are:

- 50 Ω res. & HF comparator recovering the received signal
- Voltage reference as a threshold for the HF comparator
- Negative LDO regulator for powering of the comparator or optionally negative charge pump circuit
- Connector to the FPGA devkit used as a decoder

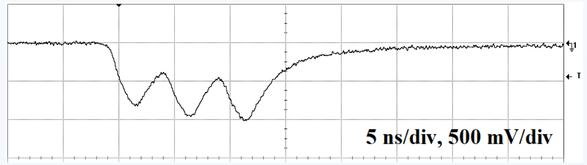


The picture below shows the FW architecture. The coder catches the train activity signals and sends them via shift register to the decoder. The recovered signal is then sampled by 1.6 GHz (equivalently) and decoded to four DAQ outputs.



MEASUREMENT & RESULTS

The codec was tested in the real environment at LHC in CERN. The test vectors covered all of the data combinations (i.e. start bit and numbers from 0 to 15). The received signal for 0101 data frame is captured below.



The whole data frame takes approx. 13.5 ns and the comparator threshold level settings is obviously critical. With the correct threshold level adjustment there is no problem with the data recovering and decoding.

The recovered data frame has to be shorter then 25 ns because of the 40 MHz LHC bunch clock. However, the results show the space for lowering the speed of the data transmission. This step would spread the tolerance for the threshold setting and therefore reduce the effort during tuning of the receiver.

CONCLUSIONS

The performed tests proved the proper function of the DAQ codec in its real environment. The device will be implemented in the next generation of the DTM in the AFP ToF chain. The main benefit of this codec is the possibility to differentiate the activity of the individual DTM trains.

REFERENCES

[1] Zich J., Georgiev V., Holík M., Pavlíček V., Vavroch O. Multichannel Coincidence Circuit with Settable Threshold Level for ToF AFP Detector. I*n: TELFOR. 2019.*

ACKNOWLEDGEMENT

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