

# HEPS-BPIX4: A Prototype Pixel Readout Chip Working in Single Photon Counting Mode with a Novel Charge Sharing Suppression Scheme



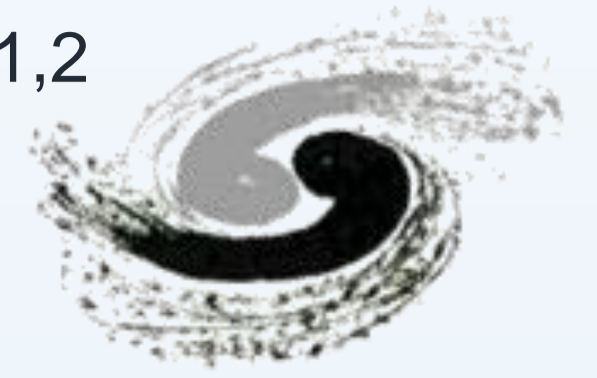
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## 1. Introduction

HEPS-BPIX4 is a hybrid pixel detector readout chip for X-ray applications for the High Energy Photon Source (HEPS) in China. It is upgraded from the HEPS-BPIX3 [1] whose performance is mainly limited by the charge sharing effect between the small size adjacent pixel. A novel architecture is proposed aiming at eliminating the spectral distortion caused by the charge sharing effect due to the fine pixel pitch. The prototype readout chip contains an array of  $20 \times 32$  pixels with a pixel size of  $55 \mu\text{m} \times 55 \mu\text{m}$ , working in single photon counting mode. Each pixel has a counting depth of 11 bits and the chip could work at a 160 Mbps output data rate with zero dead time.

## 2. Implementation

The novel architecture is based on charge summing and centroid arbitration among adjacent pixels. In every cluster grouped by  $3 \times 3$  pixels in the chip, charge deposited in four pixels by a single photon is concentrated into the center pixel and added together. The sum of the charge is compared with the energy threshold for discrimination. In the meantime, the center pixel is also judged by a secondary comparator with a minimum threshold. The arbitrator decides if the charge of the center pixel is the maximum in the cluster. Only those two matched conditions give a photon counting pulse to the digital part.

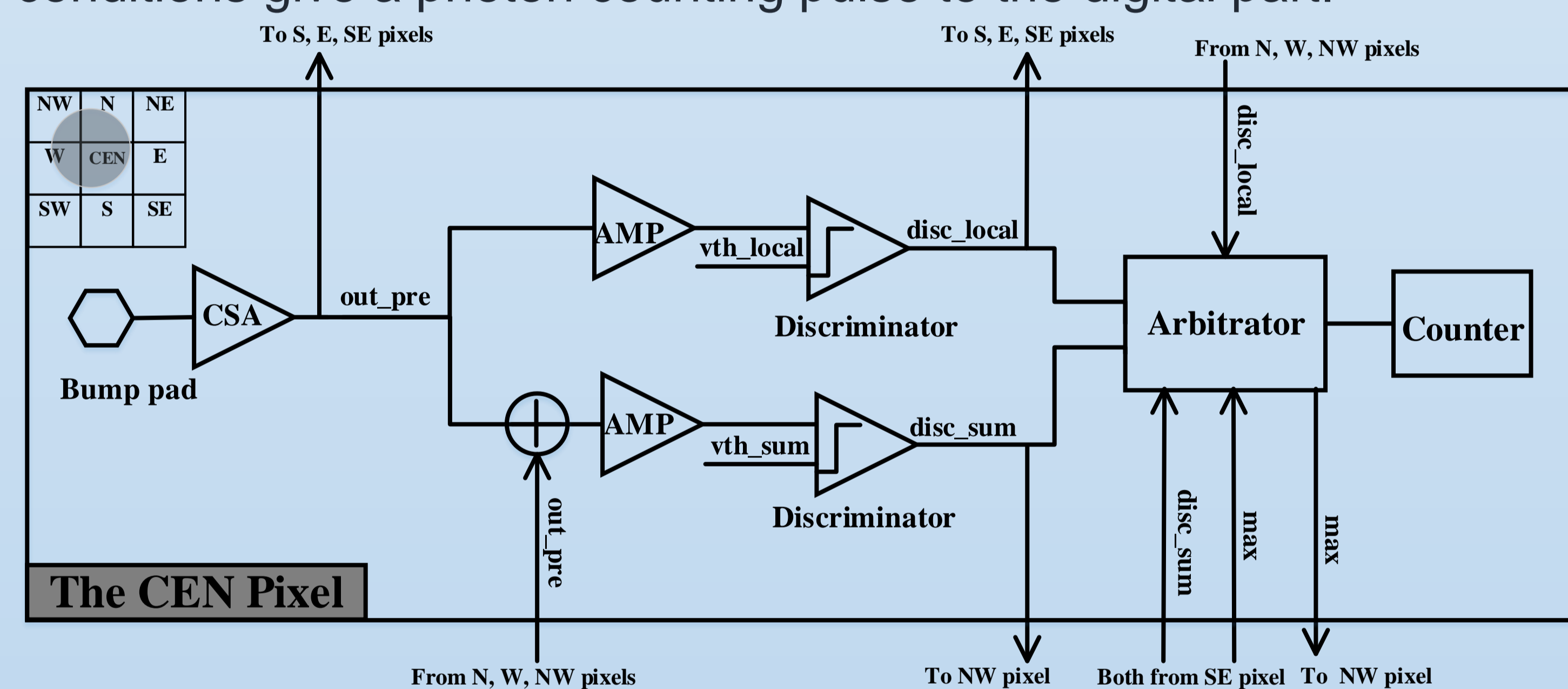


Figure 1. Block diagram of the HEPS-BPIX4 pixel cell

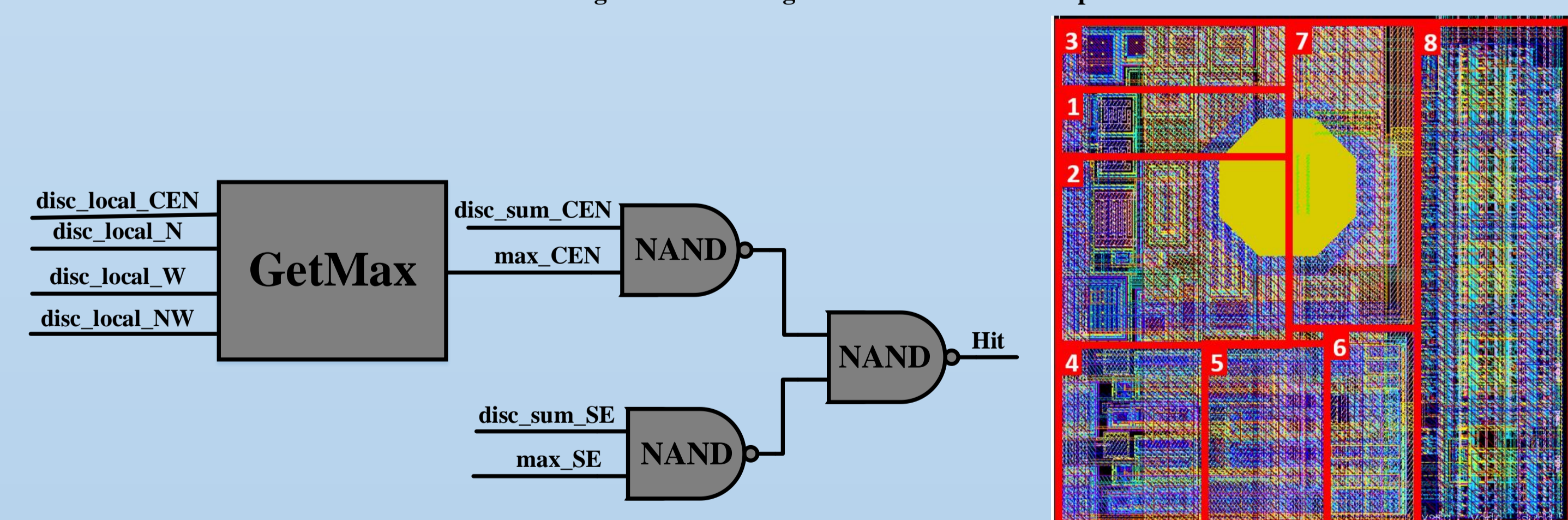


Figure 2. Block diagram of the Arbitrator block in the pixel cell

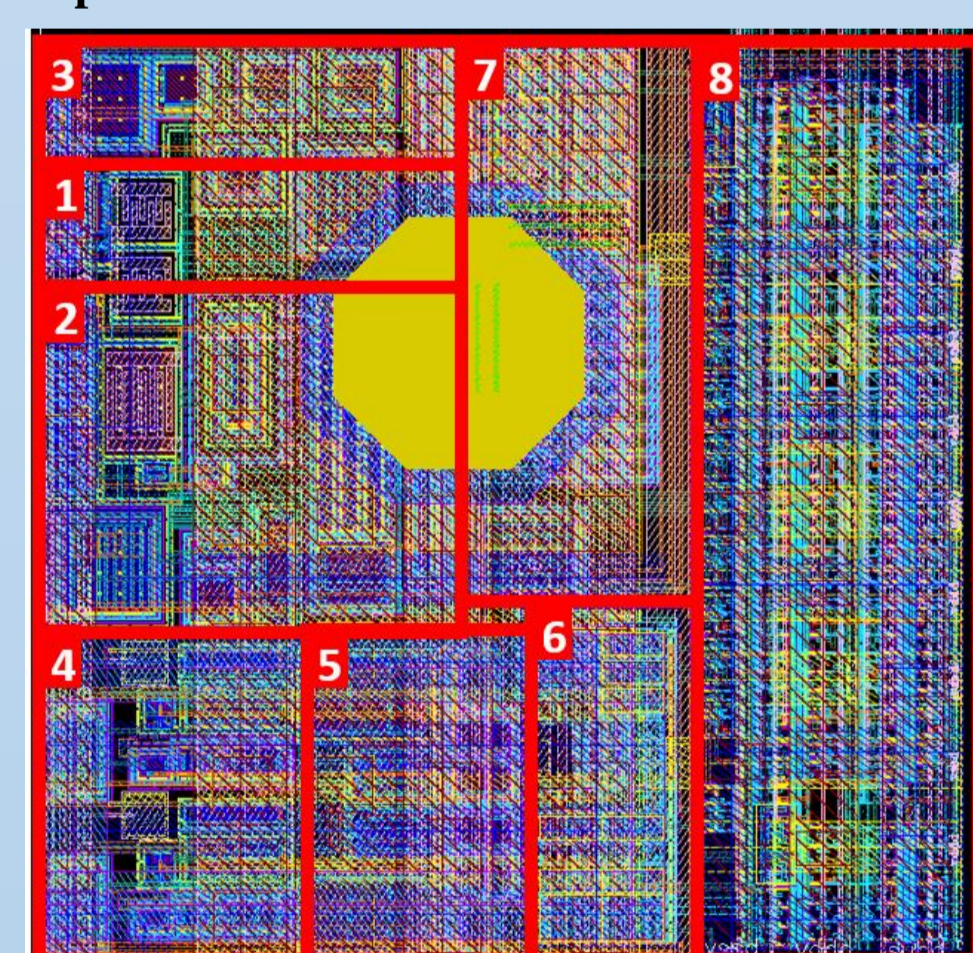


Figure 3. Layout of the HEPS-BPIX4 pixel cell

Compared with reported schemes that transmitted more than ten signals, the proposed scheme reduced the complexity of communicated pixels interconnection in the layout. There are only seven signals including three analog signals and four digital signals received by the center pixel from the adjacent four pixels.

## 5. Summary

The HEPS-BPIX4 chip dedicated for the HEPS in China has been designed and fabricated using a 130 nm CMOS technology. It implements a novel architecture to eliminate the spectral distortion due to the charge sharing effect in a pixel cell of  $55 \mu\text{m} \times 55 \mu\text{m}$ . The chip has been characterized using an electrical test pulse. Measurements show an equivalent input noise of 150 e- rms and effective suppression of charge sharing effect. Further experiments and calibration studies will be performed on synchrotron radiation beamlines.

## Acknowledgment

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[1] S. Cui, W. Wei, et al. HEPS-BPIX3: A Fine Pitch Pixel Readout Chip Working in Single Photon Counting Mode for Synchrotron Radiation Applications 2021 JINST 16 P08004

## 3. Algorithm Simulation

The proposed scheme was proven by algorithm simulation which was interpreted from the circuit logic. Every point in the circle of the graph was generated randomly which simulated a photon hit a  $2 \times 2$  pixel cluster simultaneously. Its coordinate divided the circle into four quadrants whose area represented the received charge of these four pixels. Finally, the algorithm would give the result of which pixel in the cluster should be assigned all the charges. One thousand single photon events had been simulated. Comparison results of the algorithm and the real case proved that the proposed scheme could correctly deal with the cases of charge sharing with 99% precision.

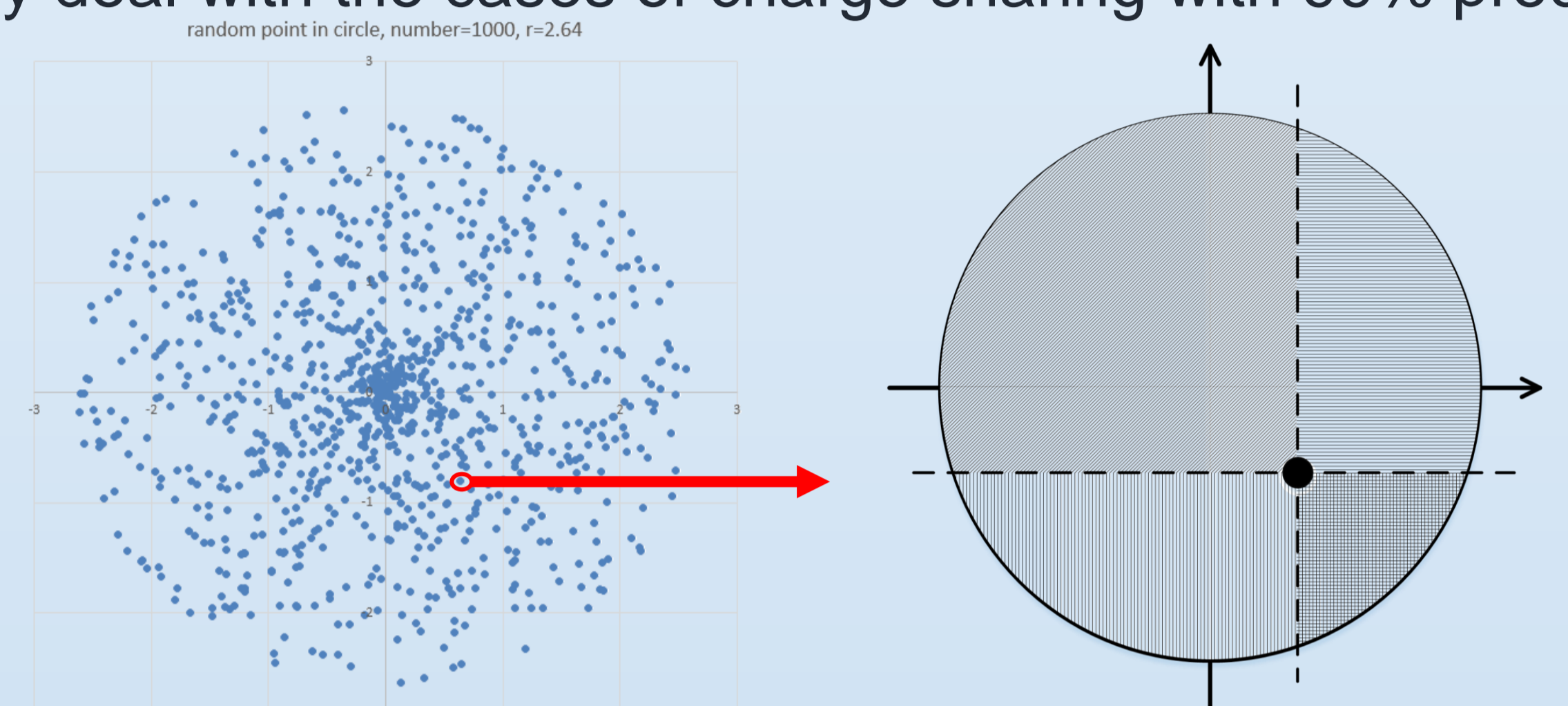


Figure 4. a. The position map of 1000 randomized points in a circle. b. One example in the 1000 randomized points.

## 4. Measurement

The test platform is based on a KC705 FPGA evaluation board. It employs a TCP/IP core (SiTCP) for data transmission. The test PCB is connected to the FPGA board via an FMC socket. All the configuration, control, readout, and calibration commands are carried out via the Python environment.

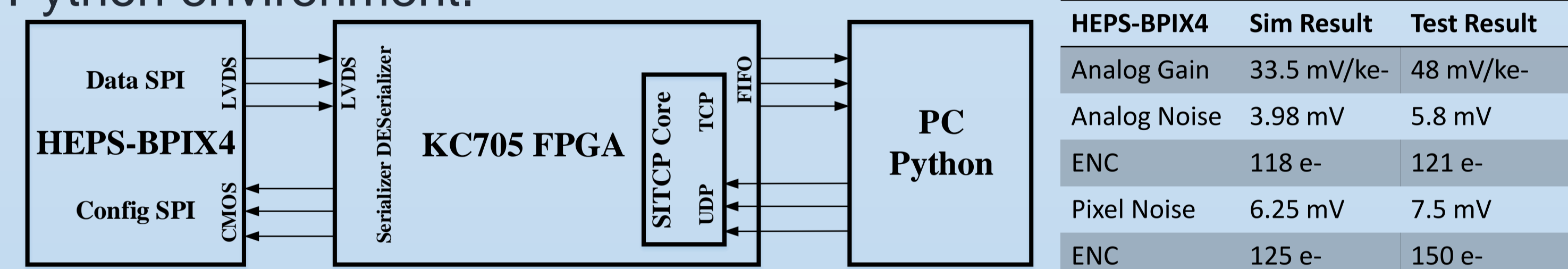


Figure 5. Block diagram of the test system

Measurements have been performed for a  $2 \times 2$  pixel array using a standard electronic test platform. The four pixels which contain both analog and digital buffers permit simultaneously external monitoring of the output of the preamplifier, the shaper, and the discriminator.

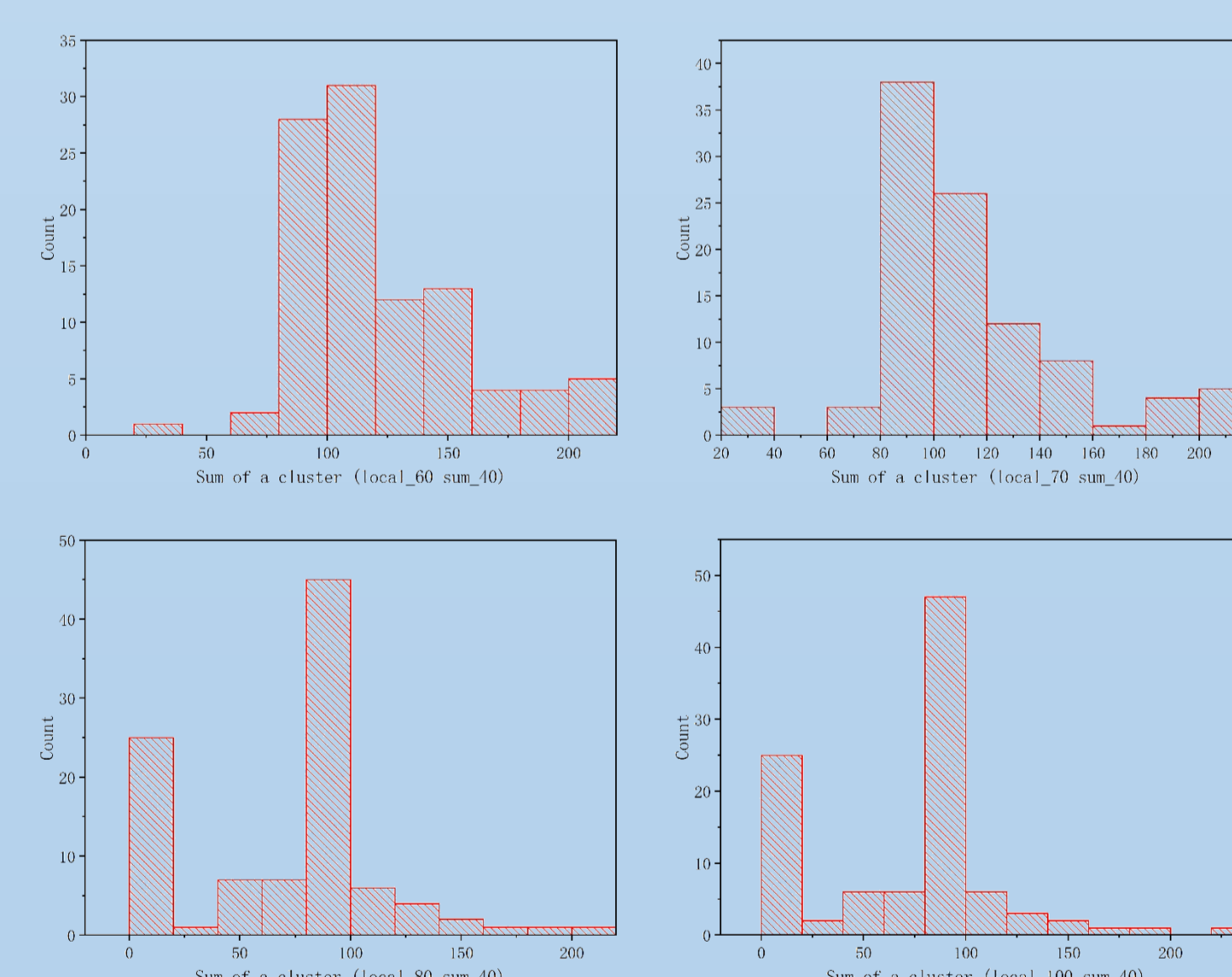


Figure 6. Histogram of the sum counts of the  $2 \times 2$  pixel array in a preliminary test. There are one hundred charge sharing cases that follow Gauss distribution. The four group tests have the same configuration of the sum threshold and the different configuration of the local threshold.

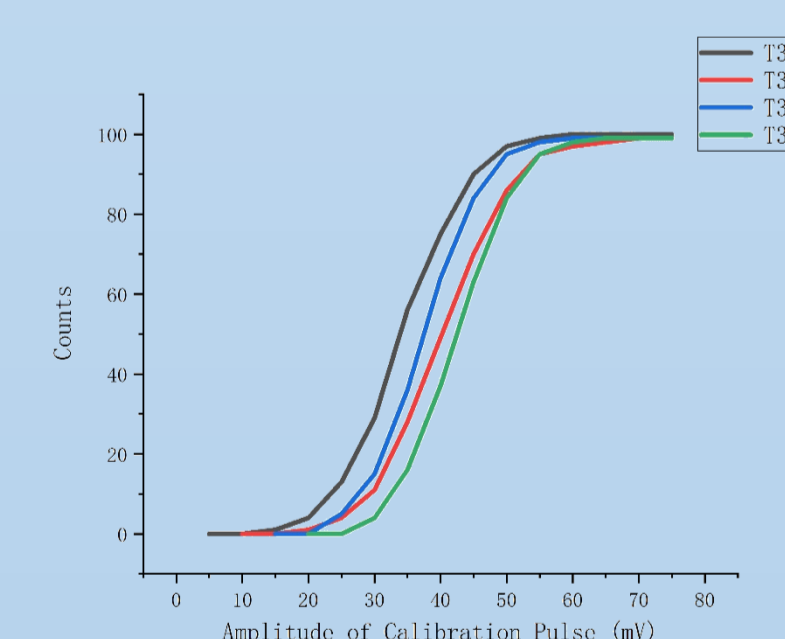


Figure 7. S-curve responses of the  $2 \times 2$  pixel array (GDAC = 70, LDAC = 12)

18	4	0	0
194	84	155	98

Figure 8. A typical case that is selected from the one hundred cases according to the s-curve response. a. The energy distributions of the  $2 \times 2$  pixel array b. The count results of the  $2 \times 2$  pixel array.