# A congestion awareness and Fault-tolerance Readout Network ASIC for High-Density Electrode Array Targeting Neutrinoless Double-Beta Decay Search in TPC



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# Introduction

- Among the current and planed experiments of  $0\nu\beta\beta$ , the high-pressure gaseous Time Projection Chamber(TPC) stand out for excellent energy resolution, very low radioactive background level and good scalability.
- To achieve excellent energy resolution and charge tracking imaging, A pixelated charge readout plane without gas-electron avalanche is desirable because of avalanche gas gain that severely deteriorates the energy resolution. Based on a 0.35um CMOS process, a low noise sensor, Topmetal-S, is being developed which, even without gas gain, the 1% FWHM energy resolution requirement could be met.
- Since  $0\nu\beta\beta$  tracks are extended to tens of cm in high-pressure gas, and taking advantage of the charge focusing electric field, the first prototype of Topmetal-S is designed to have mm-sized charge collection electrode, followed by a charge sensitive amplifier and an ADC in the first prototype.
- To realize a ton-scale high-pressure gaseous TPC, approximately 10<sup>5</sup> Topmetal-S sensors need to be laid on a meter-sized plane with the pith no more than 10mm. The greatest challenge is a reliable high-density sensor readout and sensor control.
- This paper present a readout network Application Specific Integrated Circuit(ASIC) for the high-density electrode array.

# The readout plane

- The hexagonal pattern placed sensor array is organized into two separated 2D-meshes.
- Charge Collection and Processing Circuit (CCPC) : generates data, including charge collection electrode, CSA, ADC and so on
- Readout and Dara Routing Circuit (**RDRC**) : transmits their own data and forwards data from nearby sensors



#### The first version of readout network (FT-RDRC chip)

### **\***Detection

• Checking whether there are any faulty node in the network

## **Preliminary simulation results based UVM Testbench**



• The output of the network is transfer to the scoreboard by the serial bus function model (BFM) proxy. The input of each RDRC is monitored and then sent to scoreboard. The input of each RDRC is compared with the output of the network in the scoreboard.

# The new readout network chip (AFT-RDRC chip) design

Readout Network Chip

• Locating the faulty node if there are some faulty node

# **\***Configuration

• Some nodes closed to the faulty node are marked as unsafe nodes, a series of unsafe nodes forms a faulty block.

# **\***Routing

- The fault-tolerance XY routing follows the regular XY routing (first Y(X) then X(Y)) until the packet reaches a boundary node of a faulty block.
- The packet is routed around the block clockwise to pass through the faulty block if the packet reaches a boundary node of a faulty block.



# The new version of readout network

# **\***Motivation

- To prevent congested node from degrading the network throughput
- Improve the network performance (such as latency, chip area)
   The adaptive and fault-tolerance routing algorithm (AFT-XY)





- The readout network chip consists of a RDRC (the upper part) and a local model for chip test.
- The RDRC is mainly composed of five full-duplex interfaces, router, and internal register. The local interface is one of the interface exchanged data with local model (or CCPC), the other interfaces are used to data forwarding.
- According to the destination information carried in the incoming packet and local information, the routing direction is determined by the router.
- The pitch of those sensor is no more than 10mm. → The UART protocol is used to exchange data between nearby sensors.
- The Adaptive and Fault-Tolerance XY (AFT-XY) routing follows the FT-XY routing if the packet doesn't reach a node of congested area edge.
- The eastern (western) packet is routed to the next (previous) row to bypass congested area.
- The congested area can automatically enlarged or reduced according to the status of the nodes. The node is marked as congested node when the occupancy rate of the

ing path



	Core area	maximum hit-rate in worst case
FT-XY chip	$1.03$ mm $\times 0.89$ mm	$4.1 \times 10^3$ event/s
AFT-XY chip	0.68mm × $0.67mm$	$5.0 \times 10^3$ event/s

## **Conclusions and Outlook**

We propose a distributed, self-organizing, congestion awareness, and fault-tolerant readout network ASIC for the readout of a high-density electrode array. The design of the network and simulation results are presented.

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