

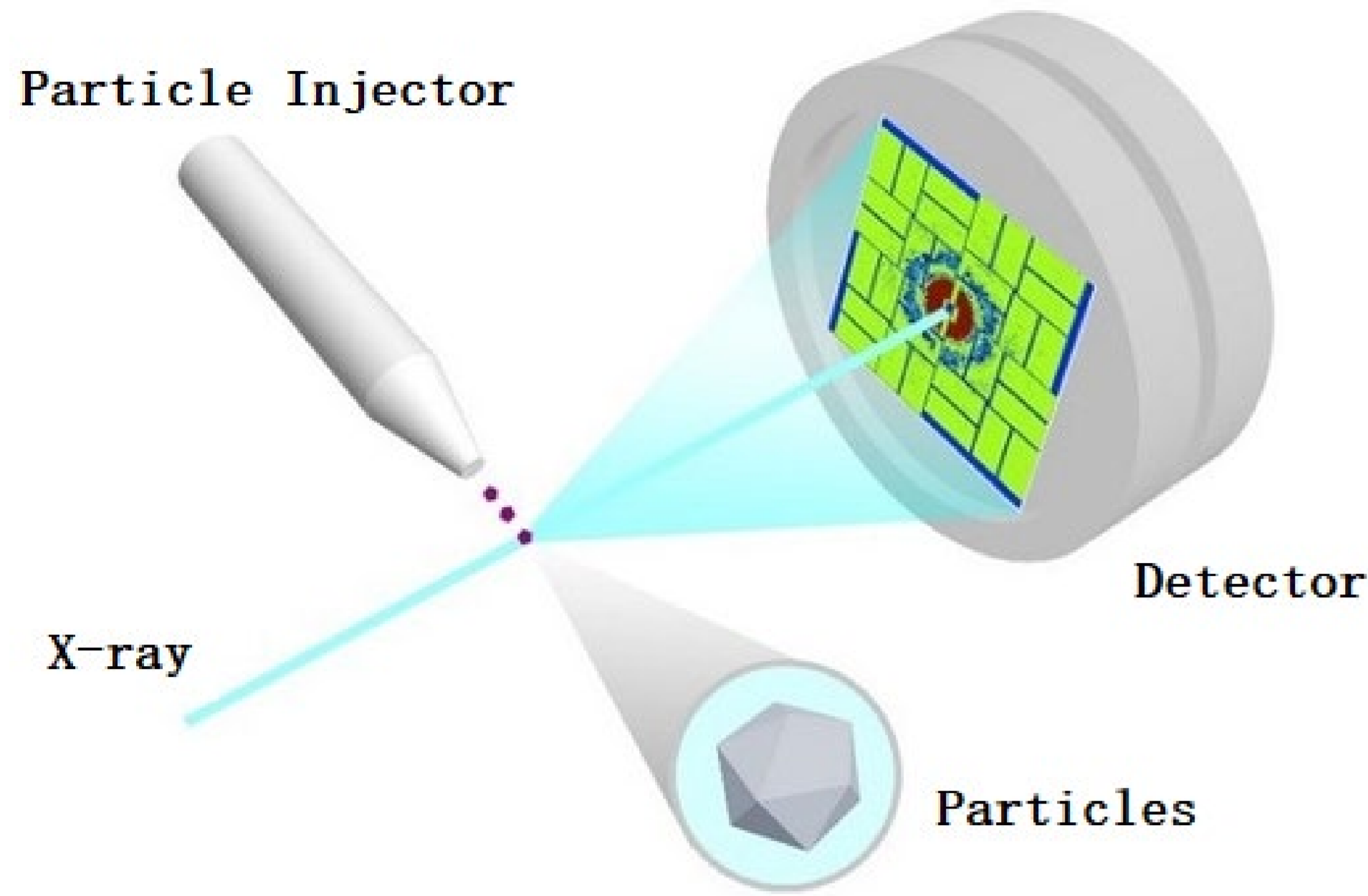
A hybrid pixel detector with 4D information for dynamic synchrotron radiation applications

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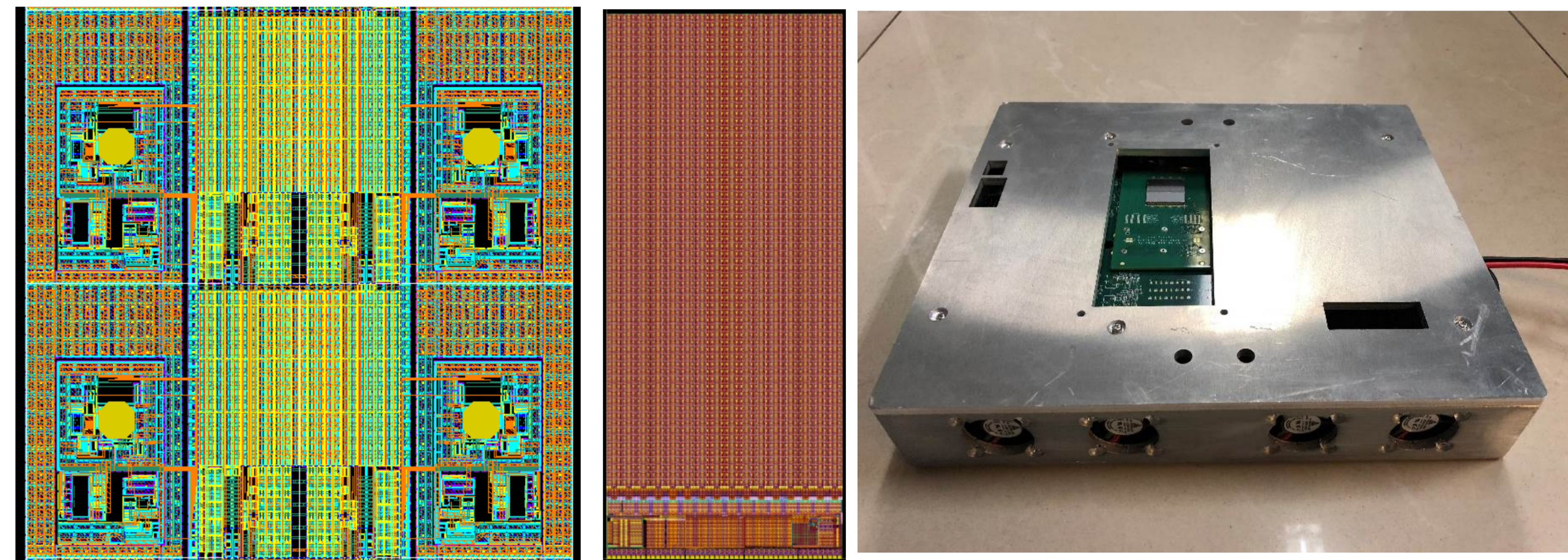
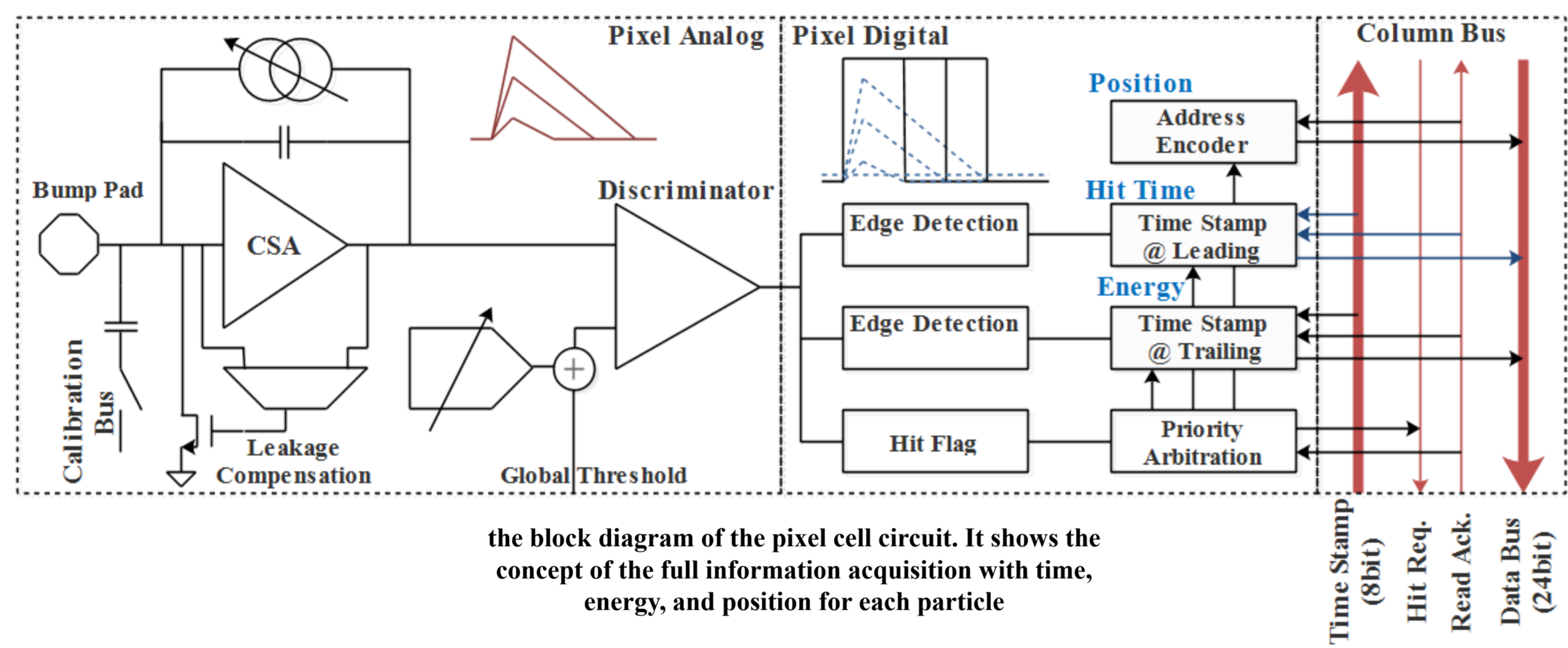


Dynamic applications in Synchrotron Radiations

The next generation of light source, High Energy Photon Source (HEPS), is under construction in Beijing, China. It proposes one of highest luminosity and emittance synchrotron radiation light source worldwide, and over 90 beamlines for various experiments are scheduled[1].

The photon counting detectors like PILATUS[2], MEDIPIX[3] has brought a great promotion of the performance of the beamline experiment, like the zero-noise imaging, PSF, frame rate and so on. However, these detectors are still not capable for single event distinguish in each pixel, so that high speed dynamic process like single pulse diffraction of the macromolecules[4] can not be observed only by frame refreshing in high counting rate circumstance.

We proposed a pixel readout chip based on hit driven that can readout the information of every single event. The arrival time, energy, plus the pixel location can be detected altogether via TOT method at the same time. Therefore a "lossless" and continuous imaging can be achieved after the data reconstruction. This makes this scheme suitable for the observation on transient dynamic process with sparse hits.



Layout of a 2x2 pixels

Layout of the full size chip

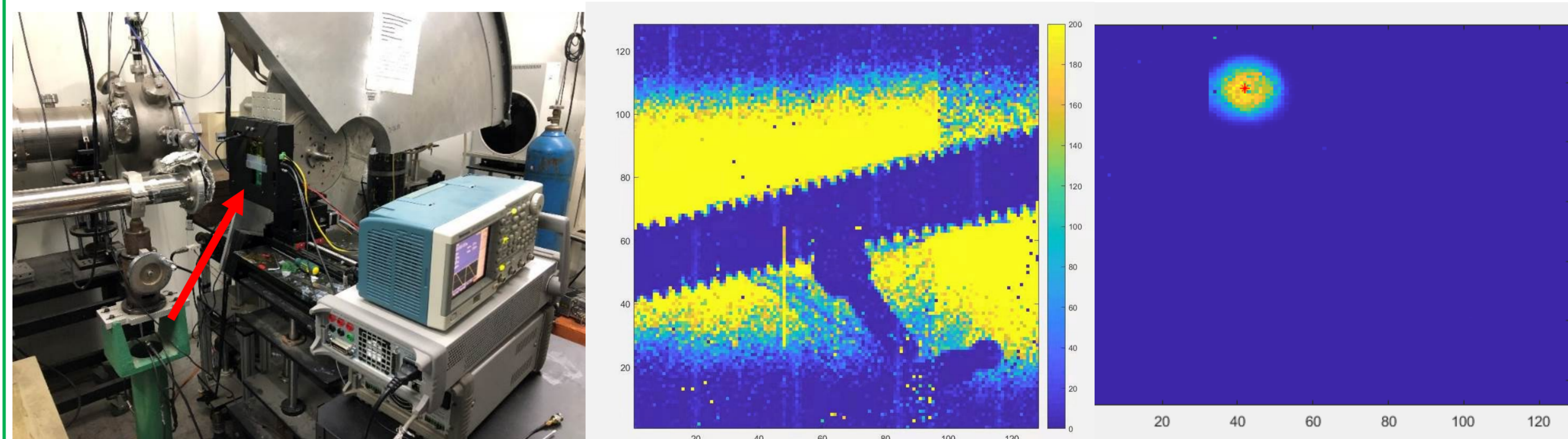
A photo of a detector module

Aiming for a 8~20keV energy range, a 300um-thick Si P-in-N sensor will be used. To keep the pixel compact, the ToT (Time over Threshold) structure was used[5]. The injection charge is converted to a triangular wave by a constant current source feedback of the charge amplifier. The width of the wave is proportional to the input charge. Then a discriminator and a TDC with global time stamps can easily digitize the analog output. Its leading edge gives the arrival time, and the time difference between the trailing and leading edge is proportional to the energy. Combined with an address encoder for pixel position, the full information of the event is thus acquired.

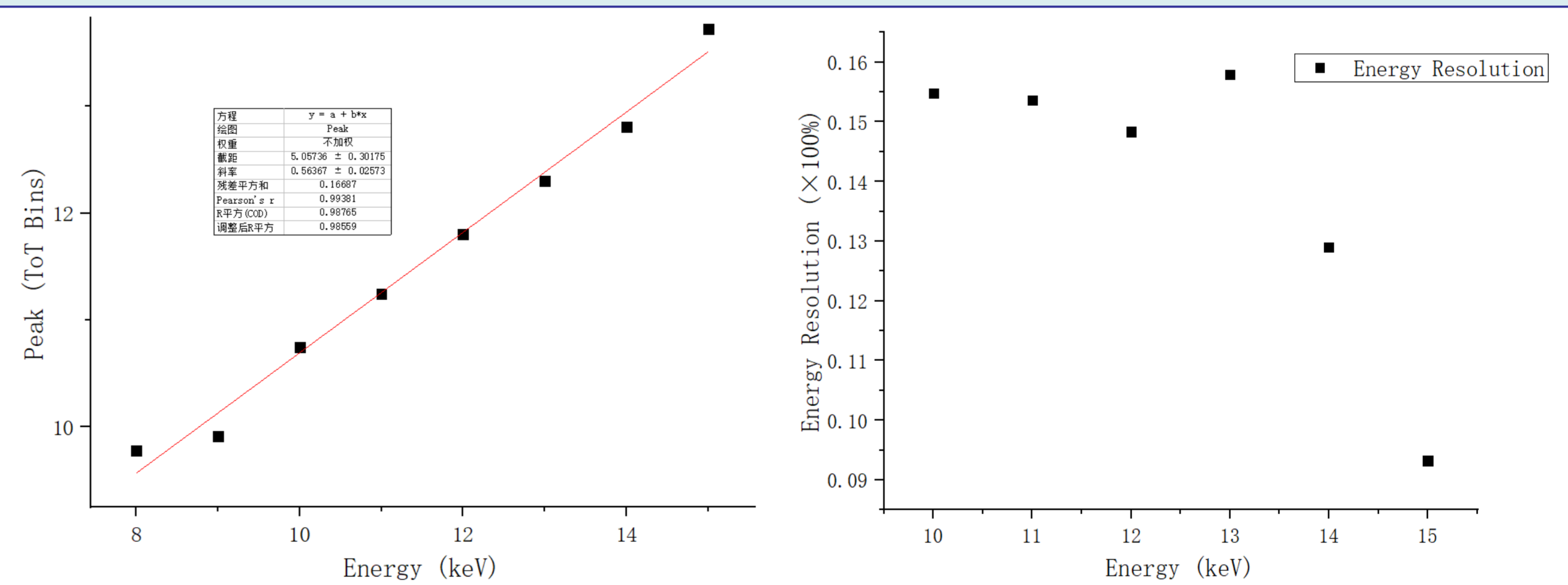
The pixel readout chip was designed in a Hit-Driven readout architecture for high hit rate. The pixel digital part was based on a FE-I3 like priority arbitrary logic[6]. The time stamps of both edges will be latched in pixel registers, and the hit flag will be sent by the Fast-Or bus to the periphery. Once a pixel was hit, the full column will be frozen for new hits. With a readout acknowledgement from the End-of-Column (EoC) logic, the latched bits of hit pixels, including two 8-bit time stamps of both edges, plus 8-bit address, will be sequentially readout to the EoC buffer, validating by priority token. After the hit flag was clear, this column was released for the new hits.

The pixel size is $150 \times 150 \mu\text{m}^2$, and the full size chip has been taped out with an engineering run, with a pixel array of 64×32 pixels. The chip is designed using a CMOS 130nm technology, measuring an area of $11.1\text{mm} \times 4.8\text{mm}$.

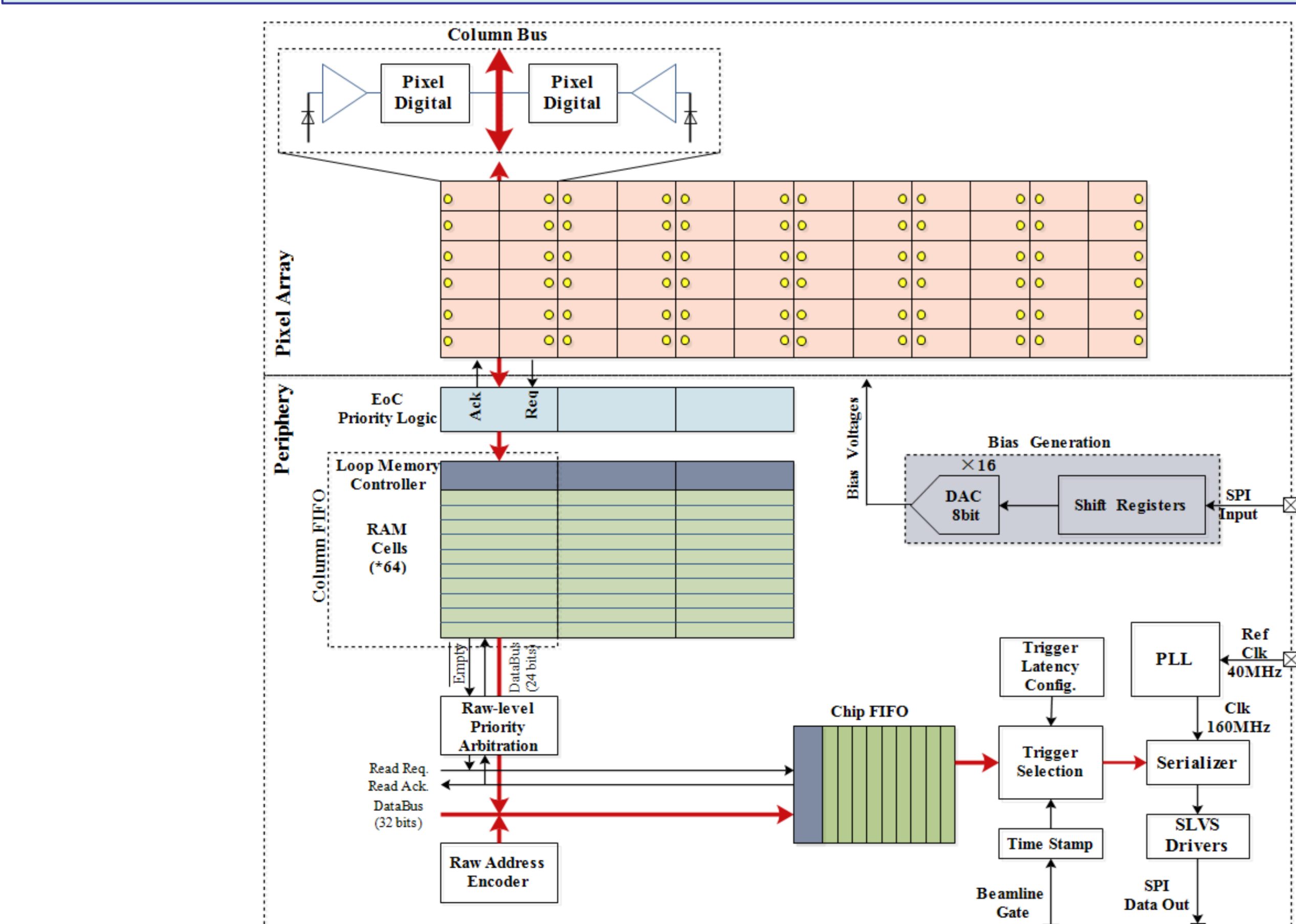
A 2×4 chip array is bump bonded with a sensor and a sensitive area of $2\text{cm} \times 2\text{cm}$ can be achieved. Data from multiple chips are first concentrated and packaged in FPGA, then the data are transmitted via SiTCP [8] interface to a PC.



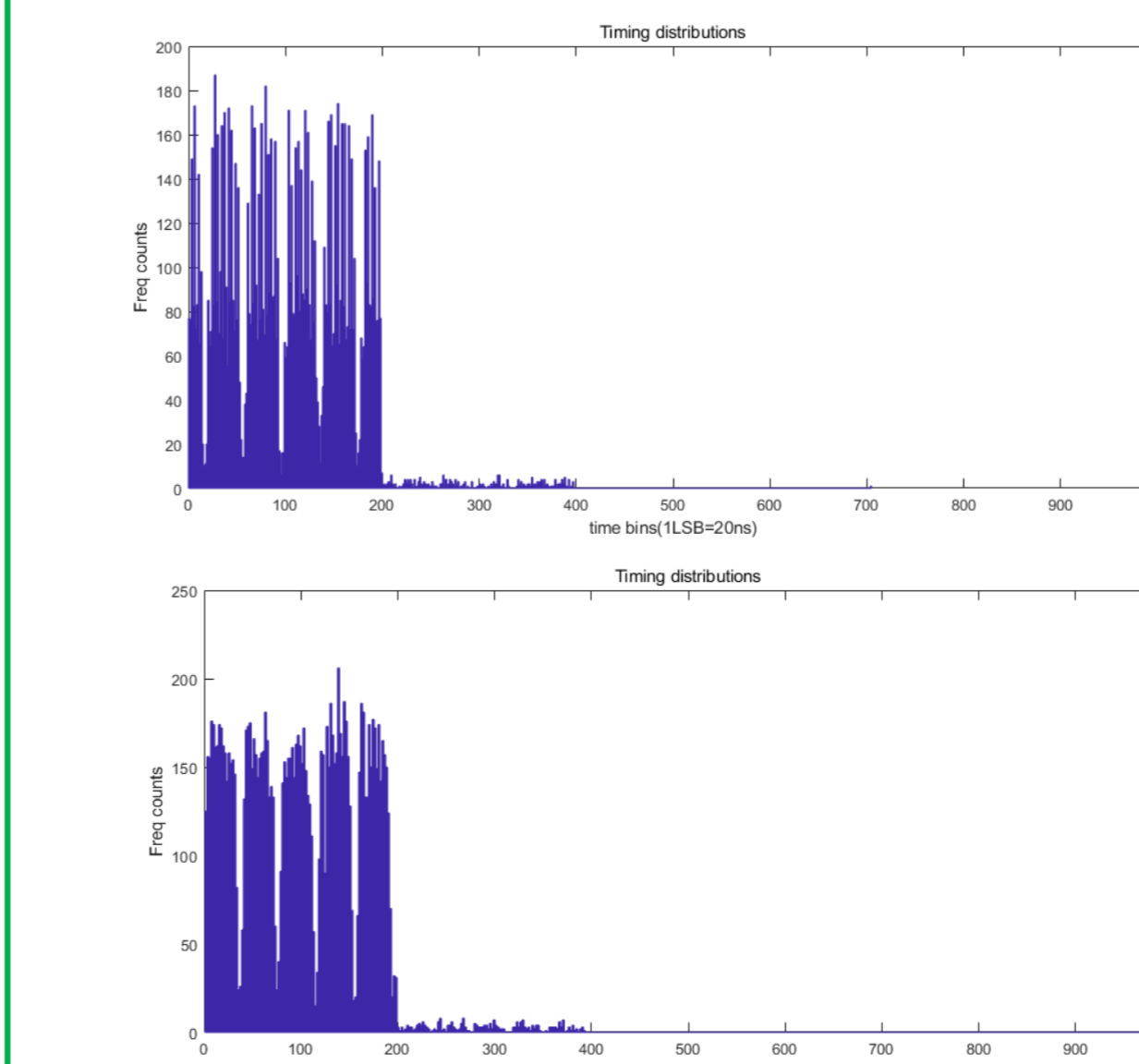
The module system was tested at BSRF (Beijing Synchrotron Radiation Facility) and both an X-ray imaging of a screw and an imaging of a beam spot was obtained. This shows the system is capable for classical applications for synchrotron radiations.



The energy measurement was tested by injecting monochrome light and data of the pixel in the center of the beam spot were analyzed. The fitted energy response over a range of 8keV to 15keV showed a nonlinearity less than $\pm 5\%$, and the energy resolution was better than 16% over the full range.



The chip architecture was designed in a two-stage FIFO style. The EoC event buffer was designed as a Looped-FIFO. Its depth was designed to be 64 words to cope with most of the applications. All the non-empty EoC FIFOs, plus the column address code, will be further sent to the chip periphery FIFO in a similar priority logic. It will be then readout via SLVS interface by high speed serializer.



By using a clock of 50MHz for TDC, the expected timing resolution is about 20ns. The beamline timing structure was observed by the system. It can be found in the picture that the fine distribution of 5 bunch, each with a 660ns duty cycle, can be distinguished. By adding a specific delay, the whole distribution was also shifted with the expected timing.

Reference:
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