High-performance HV-CMOS Sensors for Future Particle Physics Experiments

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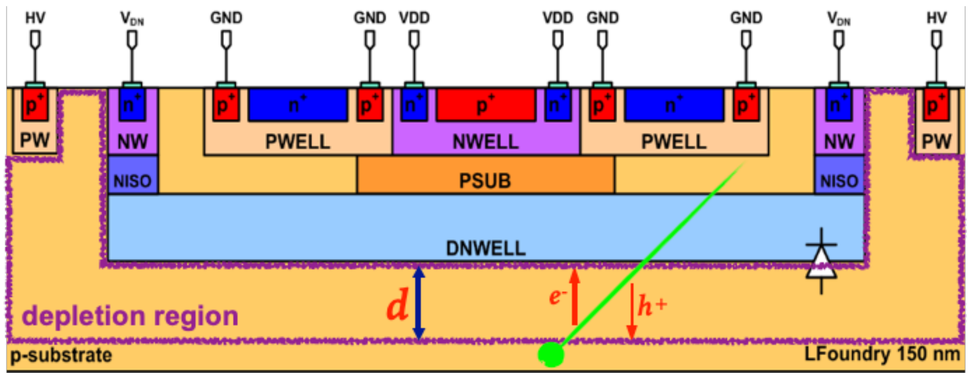
HV-CMOS Sensors



Cross section of an HV-CMOS sensor in LFoundry 150 nm process.

HV-CMOS sensors integrate both the silicon sensor and readout ASIC into the same silicon substrate forming a **one-layer structure**, eliminating the need for complex bump-bonding which is required by traditional hybrid silicon sensors (two layers).

Their substrates (often with high resistivity) are biased to **High Voltages** to create a wide depletion region with a strong electric field, which makes fast charge collection by drift and high radiation tolerance possible.

The feasibility of integrating analog and digital readout electronics into the same chip allows the production of fully **monolithic** HV-CMOS sensors.

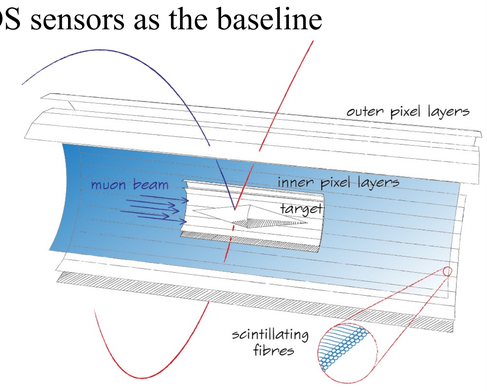
As a result, the HV-CMOS sensors have the following advantages:

- **Small material budget** (single piece of silicon, ~ 50 μm);
- **Low manufacture cost** (industry standard process, no need of bump-bonding);
- **High spatial resolution** (not limited by the size of bump bond);
- **Fast charge collection** (by drift due to high electric field);
- **High radiation tolerance** (high bias voltage and high substrate resistivity increase the depletion depth ($\boldsymbol{d \propto \sqrt{\rho \cdot V_{bias}}}$), making the sensor tolerant to radiation damages).

Future Experiments

Future particle physics experiments impose unprecedented requirements on detectors.

- The **HL-LHC** (High-Luminosity LHC) will increase the particle luminosity to the level of $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$, thus creating an extreme radiation environment. Pixel detectors are required to have radiation tolerance higher than $2\times10^{16}\mathrm{n_{eq}/cm^2}$. The LHCb Upgrade Ib/II has been considering using HV-CMOS sensors as the baseline technology for its new Inner and Middle trackers.
- The **Mu3e** experiment explores physics beyond the Standard Model by searching for rare decay of $\mu^+ \rightarrow e^+e^+e^-$. That requires pixel detectors to have high rate capability ($> 10^9$ muon/s), fine spatial resolution (< 200 μm), excellent time resolution (< 20 ns) and low material budget ($1.1\times10^{-3}\ X_0$/layer). The first large-scale application of HV-CMOS will be in Mu3e.



Central part of Mu3e experiment.

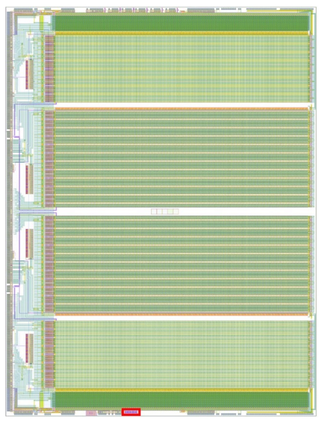
- The **CEPC** (Circular Electron Positron Collider) and future **linear colliders**, which adopt lepton collisions for precision measurements, need pixel detectors with low material budget and high spatial resolution. The HV-CMOS sensors have the potential to satisfy these two requirements.

Objectives

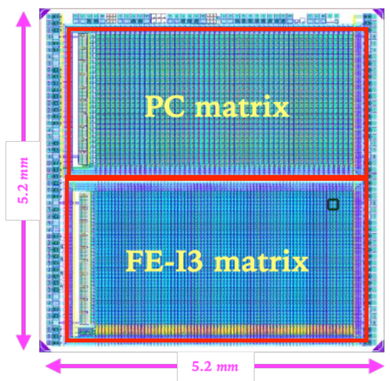
The main objectives of the R&D programmes in the HV-CMOS group at Liverpool are to push the boundaries of HV-CMOS sensors, especially in the following areas:

- **Radiation tolerance** by increasing the sensor breakdown voltage;
- **Spatial resolution** by decreasing the pixel size;
- **Time resolution** by reducing detector capacitance and enhancing readout electronics;
- **Hit rate capability** by improving data transmission speed.

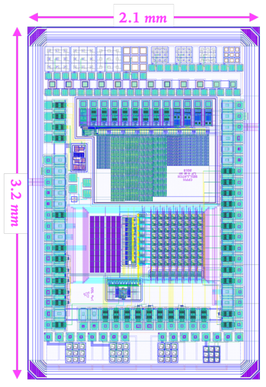
Several HV-CMOS prototypes have been designed and evaluated by Liverpool and the CERN-RD50 collaboration.



H35DEMO



RD50-MPW1



RD50-MPW2

Results

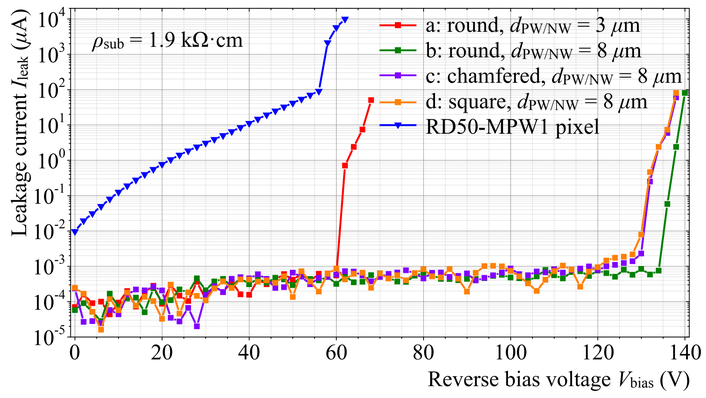
RD50-MPW1:

- Breakdown voltage V_{BD} = 55 V, which agrees with TCAD simulation.
- Leakage current was unexpectedly high.

RD50-MPW2:

- Breakdown voltage is increased to higher than 120 V.
- Leakage current is decreased by several orders of magnitude.

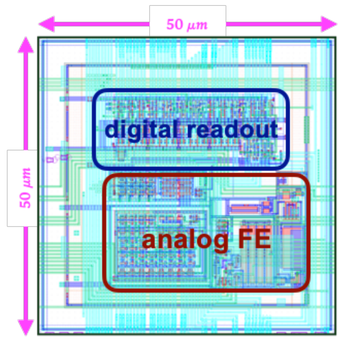
I-V curve



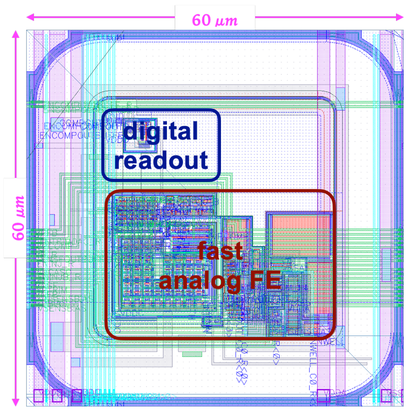
I-V curves of RD50-MPW1/2 pixels.

Pixel granularity

Fully monolithic HV-CMOS sensors have small pixel pitches (50 μm ×50 μm and 60 μm ×60 μm) with complex readout electronics (both analog and digital).



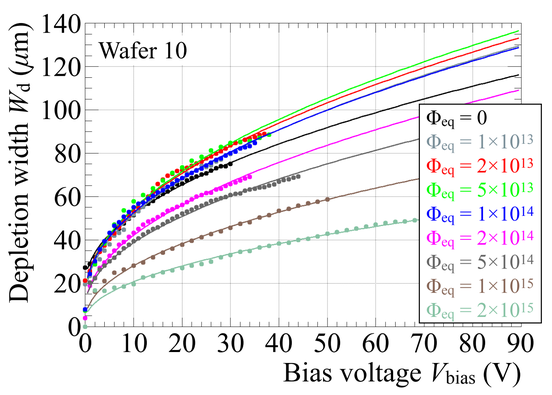
RD50-MPW1 pixel



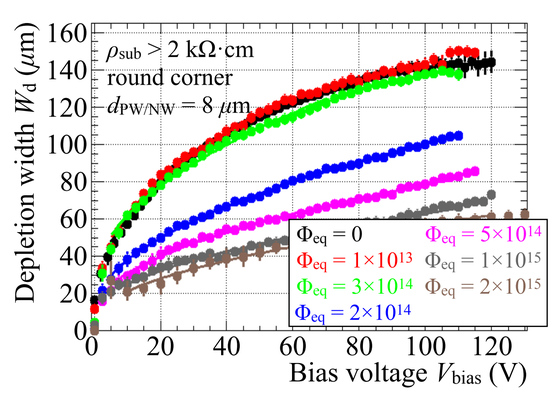
RD50-MPW2 pixel

Radiation tolerance

Due to the higher breakdown voltage, the depletion width of RD50-MPW2 can kept at an acceptable level after irradiation of the fluence of $2\times10^{15}\mathrm{n_{eq}/cm^2}$.



Depletion width of RD5-MPW1.

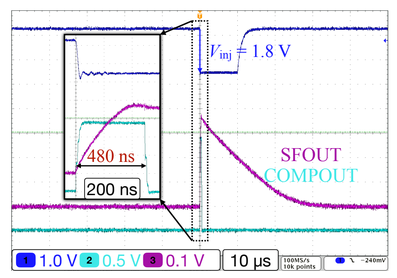


Depletion width of RD5-MPW2.

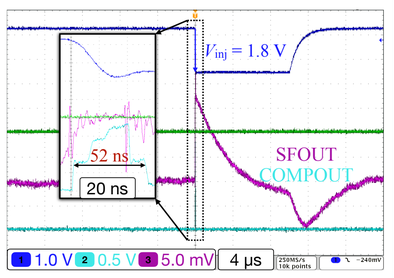
High-speed readout electronics

Two pixel flavours with fast analog front-ends.

For input charge of 35 ke$^-$, the continuous-reset and switched-reset pixels can process within 480 ns and 52 ns respectively.



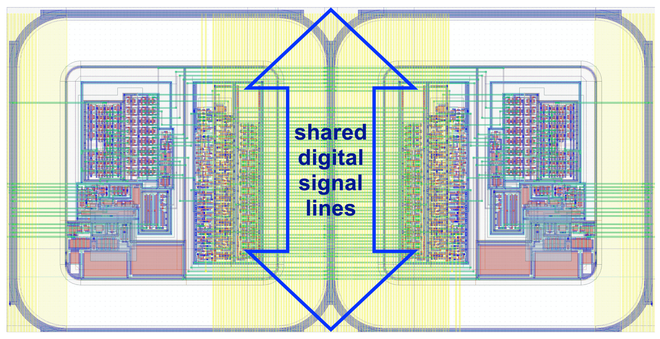
Continuous-reset pixel.



Switched-reset pixel.

RD50-MPW3, currently being designed by the RD50 CMOS Working Group has a more sophisticated pixel matrix with optimised digital readout electronics.

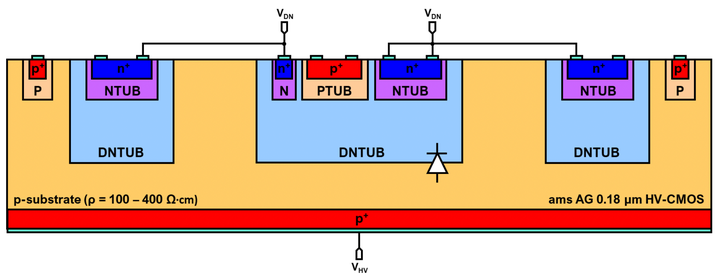
A **double-column structure** is used to share digital signal lines between pixel columns.



Double-column structure of RD50-MPW3.

Backside biasing

H35DEMO: an HV-CMOS prototype in AMS 0.35 μm process with backside biasing possibility. Its charge collection profile and depletion width after irradiation are measured using Edge-TCT.



Cross section of H35DEMO pixel.