CHARACTERISATION OF HV-MAPS ATLASPIX3 AND ITS APPLICATIONS FOR FUTURE LEPTON COLLIDERS

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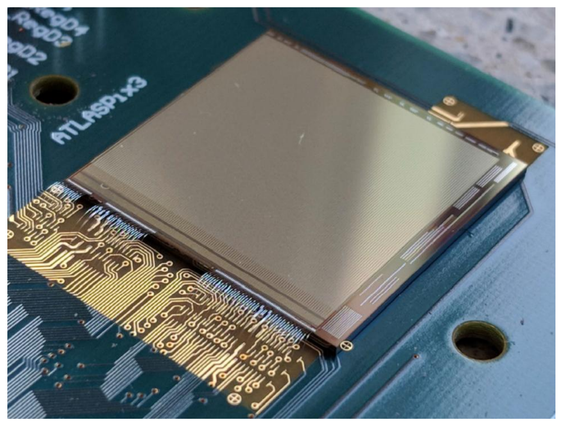
ABSTRACT

Depleted high voltage CMOS pixel sensors have been proposed in several future particle physics experiments for particle tracking. **ATLASPix3** is the first full reticle size high voltage Monolithic Active Pixel CMOS sensor, designed to meet the specifications of outer layers of the ATLAS inner tracker (ITk).

Its thin design, the excellent position resolution, high readout rate and high radiation tolerance make ATLASPix3 an ideal candidate for large-area tracking detector R&D of **future collider** experiments such as the Circular Electron Positron Collider (**CEPC**) silicon tracker.



Circular Electron Positron Collider (CEPC)

The **CEPC** is a 100 km circumference double-ring electron and positron collider proposed by the Chinese particle physics community, that will operate in three different modes[1]:

- **H**: e+e- → ZH 7 years – 240 GeV
- **Z**: e+e- → Z 2 years – 91 Gev
- **W**: e+e- → W+W- 1 year – 160 GeV

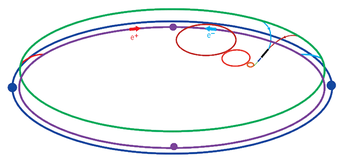


Fig. Structure of the CEPC.

The bottom quarks, charm quarks and τ-leptons produced in the decays of the Z bosons also make the CEPC an effective **B-factory** and **τ-charm factory**. The CEPC offers an unmatched opportunity for precision measurements and searches for **BSM physics**.

High Voltage Monolithic Active Pixel Sensors (HV-MAPS)

HV-MAPS are a novel type of CMOS depleted active pixel sensors for ionizing particles, implemented in standard CMOS processes.

In **depleted monolithic** sensors:

- The **sensor** element is the n-well/p-substrate diode. The sensor matrix and the readout are integrated in one single piece of silicon
- The **electronics** is embedded in shallow wells inside deep n-wells, isolated from the substrate. High voltage biasing increases the depth of depletion region, improving sensor properties as signal amplitude, charge collection speed (drift) and radiation tolerance

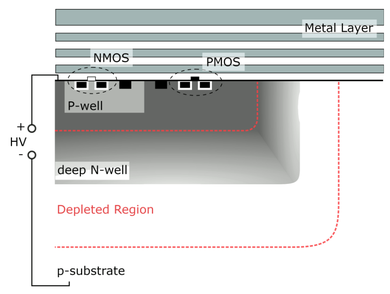


Fig. Monolithic pixel layout.

ATLASPix3: chip architecture and pixel structure

ATLASPix3 pixel detector is a system-on-chip implemented in a 180-nm high-resistivity HVCMOS technology[2]. ATLASPix3 features **132 × 372 pixels** each with an area of 150 µm × 50 µm, for a total chip area of 20.2 mm × 21 mm.

The **chip periphery** contains:

- Two readout control units
- PLL based clock generator
- Configuration registers, DACs
- Linear regulators and IO pads

The **pixel structure** includes:

- Charge sensitive amplifier
- Comparator
- Threshold tuning DAC

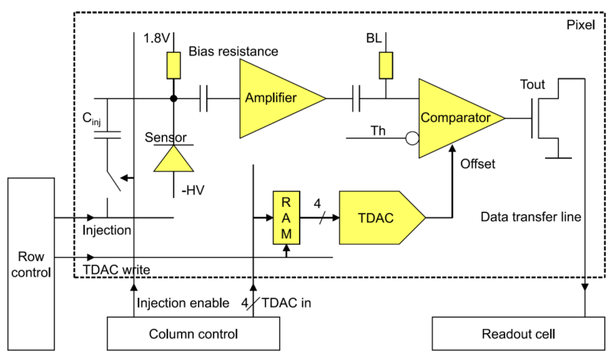


Fig. Representation of the pixel structure.

The asynchronous matrix is associated to less noise and configuration via single line with addressing (CMD) is also implemented.

ATLASPix3: digital circuits and readout structure

ATLASPix3 supports two **readout** modes: continuous and triggered readout. In the case of continuous readout, all data are transmitted. For triggered readout, only the data for the triggered events are written out sorted by event[3].

Digital circuits in ATLASpix3 perform several tasks:

- Timing with a 10 bit time stamp, amplitude measurement with additional 7 bit ToT measurement
- On-chip readout state machines for continuous and triggered readout with serialisers at 1.28 Gbit/s

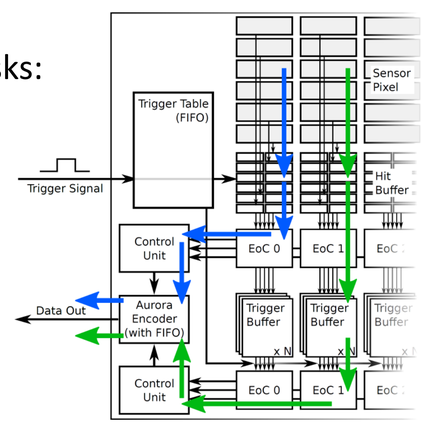


Fig. Block diagram of ATLASPix3 chip.

Experimental results: single chip card

Electrical tests and measurements with radioactive sources have been performed on the chip. For laboratory measurements, it is possible to have direct access to the amplifier output of part of the pixels, the comparator output of all pixels and debug signals for test signal generation.

The presence of the **injection circuit** allows for the extrapolation of thresholds' distributions via s-curve fitting and threshold tuning using the TDACs. Source data can be used to derive hit and ToT distributions.

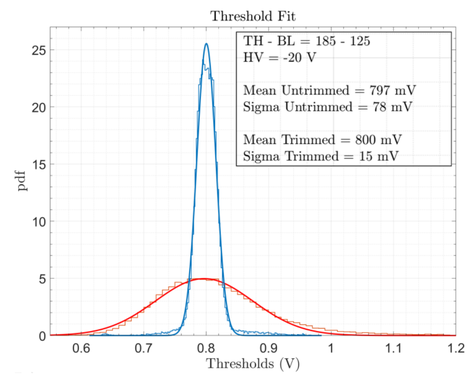


Fig. Threshold distribution before and after trimming.

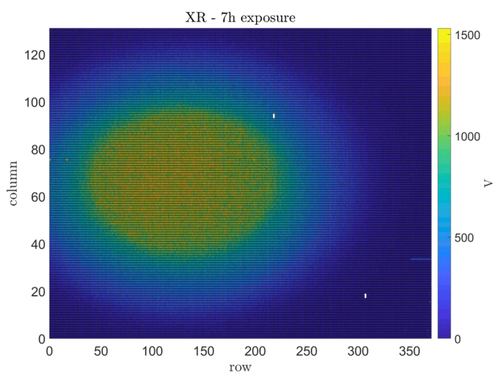


Fig. Hit map of a source run with ^{241}Am.

Increasing the **biasing voltage** causes:

- Shift of the average threshold value
- Decrease of the average noise
- Increase of detection efficiency
- Increase of the signal size for β-rays. For γ-rays the shift does not take place (same energy released).

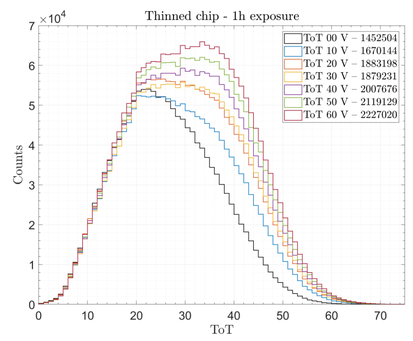


Fig. ToT spectrum shift with ^{90}Sr.

Experimental results: quad module

A quad module is the assembly of four chips glued and wirebonded onto a flex circuit. Configuration is done via a shared line with chip addressing and the chips use regulators to generate the necessary voltages on-chip from two low-voltage inputs.

Successful source runs have been performed on the 4th chip, the furthest from the power and data connections. The hit map shows the location of components on the flex. Tests on the other chips are ongoing.

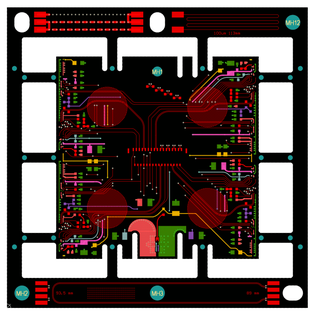


Fig. Scheme of the quad module flex.

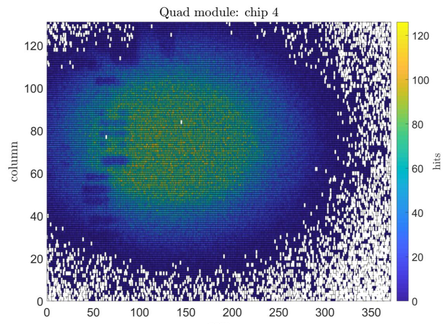


Fig. Hit map of a source run with ^{241}Am on chip 4.

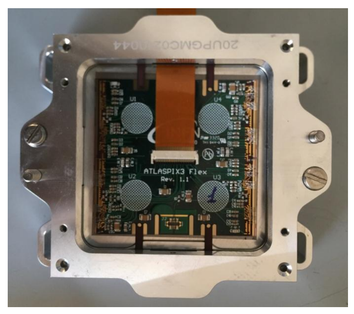


Fig. Image of the quad module.

Conclusions and bibliography

The chip has been successfully tested.

- γ source measurements revealed the homogeneity of the matrix after the tuning process
- HV scans with β sources allowed for amplitude measurements, proving the increase of the depletion volume
- Configuration over a bus with addressing confirmed the fitness for module building
- Tests on the quad module showed good responsiveness to source measurements

With the results obtained at KIT and collaborating universities also presented in previous work, fitness of ATLASPix3 for applications in detector systems, such as the CEPC silicon tracker[4], has been shown.

[1] CEPC, *"Future high energy circular colliders"*. http://cepc.ihep.ac.cn

[2] I. Perić *et al.*, "High-Voltage CMOS Active Pixel Sensor". *IEEE JSSC*, vol. 56, no. 8, pp. 2488-2502, Aug. 2021, doi: 10.1109/JSSC.2021.3061760.

[3] R. Schimassek *et al.*, "Test results of ATLASPIX3—A reticle size HVCMOS pixel sensor designed for construction of multi chip modules". *NIM A* 986 (2021): 164812.

[4] CEPC, *"The CEPC project"*. http://cepc.ihep.ac.cn/intro.html