Construction and Operations of the CMS Phase-1 Silicon Pixel Detector

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(for the CMS collaboration)

Phase-1 Pixel Detector

The pixel detector in CMS was replaced in 2017 with a new phase-1 pixel detector having improved features to cope with LHC data-taking conditions at higher rates.

- Faster digital readout chip (ROC) with enlarged buffer
- One extra layer in barrel and disk in endcap for more robust tracking
- Innermost layer closer to beam pipe (hence the interaction point)
- 66 M → 124 M channels (DC-DC converters for number of power cables)
- Reduced material budget with CO_2 based cooling system
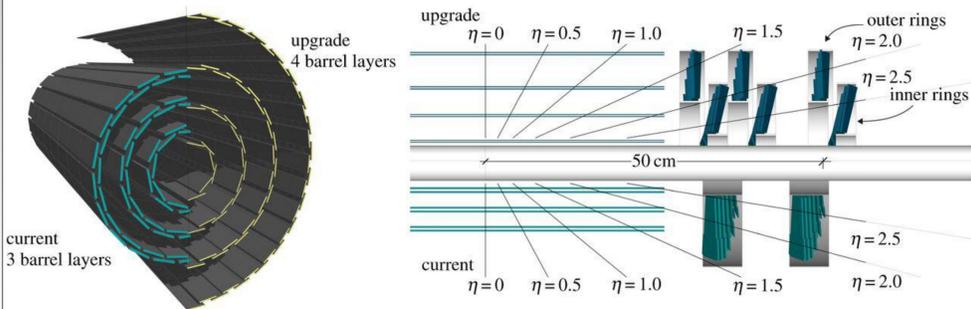
Module Construction
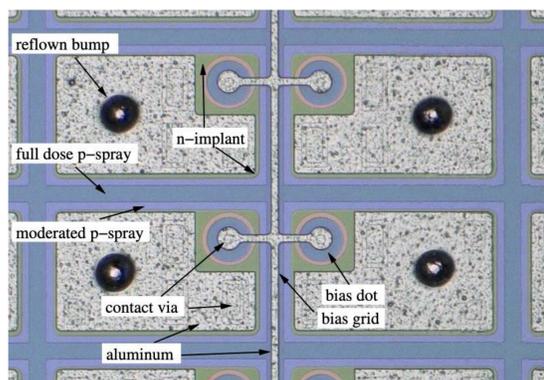
The "n-in-n" approach (n⁺ pixel implant in n substrate)
High signal at moderate voltages
- Pixel should respond to small signal (low capacity and noise)

Double sided processing
- All sensor edges on ground
- Inter-pixel isolation (p-spray)
- Punch-through bias dots define the pixel potential in case of missing bump bond connections

80 rows x 26 double columns

Double Column Periphery Time Stamp Buffer, Data Buffer

Control interface
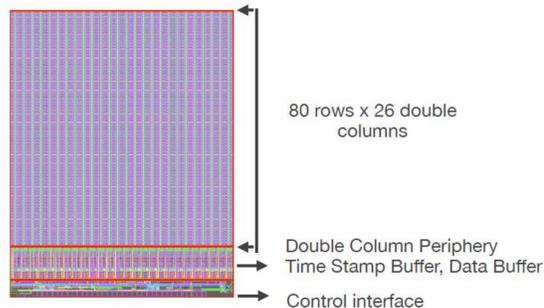
Number of pixels: 4160 (52 x 80), organized in double columns

Pixel size: 100 μm x 150 μm (rφ x z)

8 bit ADC for pulse height

Increased buffer size for time stamp (24) and data (80)

On chip digitisation, readout at 160 Mbps

Data rates
PROC600 (layer-1) 580 MHz/cm²
PSI46DIG (others) 150 MHz/cm²

- Silicon sensors with 100×150 μm² pixels, bump bonded to CMOS readout chips for DC connection.
- Signal goes to ROC through bump bonds - 16 ROCs per module.
- The Token Bit Manager (TBM) is the interface between ROCs and backend – disctributes clock, trigger and commands from backend to ROCs.
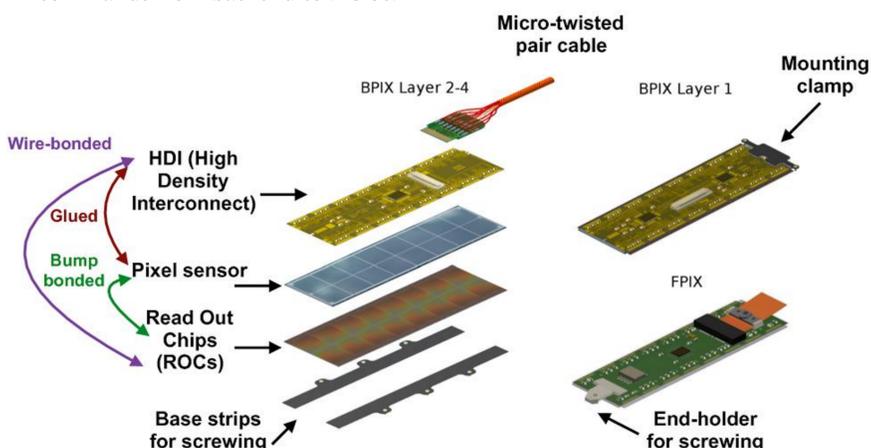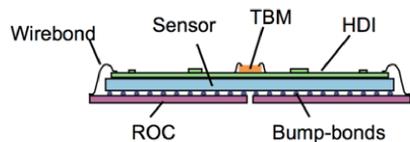
Performance
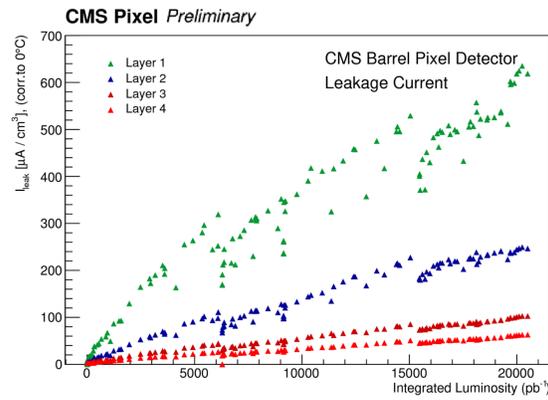
Average leakage current per ROC in pixel barrel detector normalised to active sensor volume (after radiation damage) is as expected.

Cluster charges are normalised by the track impact angle to sensor. Normalised on-track cluster charge distributions fitted by a Landau function convoluted with a Gaussian.
The cluster sizes observed across layers and disks are as expected.
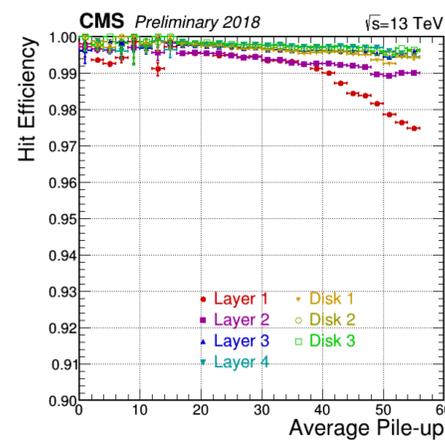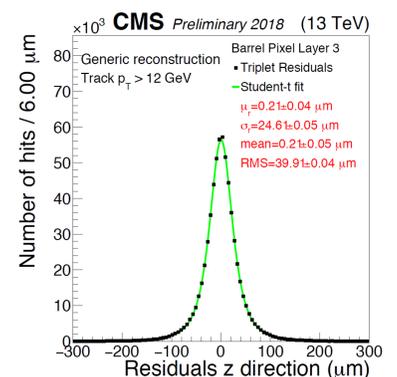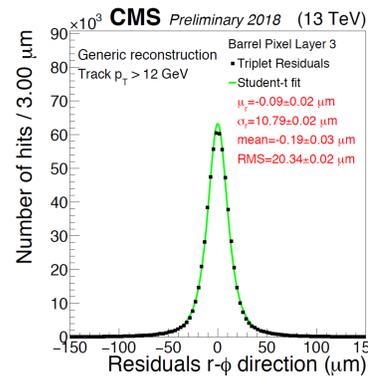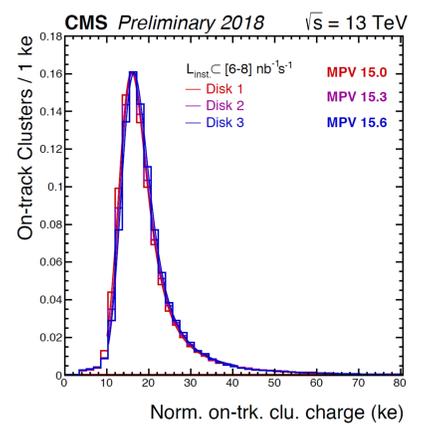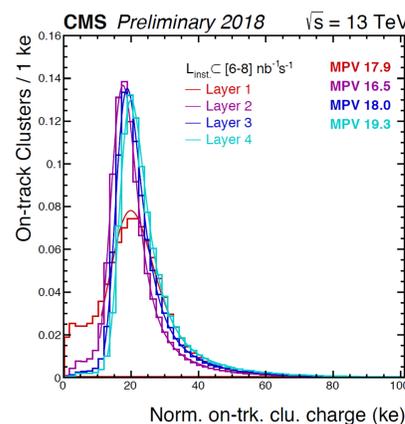
Triplet method used for the residual measurement.
Excellent position resolution observed.
r-φ direction: 10 μm   z direction: 24 μm

12 ns time difference between Layer 1 (PROC600) and Layer 2 (PSI46DIG) chips, but the two layers are in the same readout group.
The setting which maximises the efficiency for both layers chosen.

Excellent hit efficiency as a function of average pileup for different layers of Barrel and disks of Forward Pixel detector.

Summary

- The CMS Phase-1 Pixel Detector has successfully taken data at LHC Run-2
- The ROC for Layer 1 modules require higher charge threshold
- High hit efficiency and excellent position resolution observed
- Impact of radiation to the silicon sensors within expectations
- Expected ordering of cluster size observed across layers and disks
- Same level of performance as previous pixel detector with higher pileup

References

1. W. Adam et al, *JINST* 16 (2021) P02027 and all references therein
2. https://twiki.cern.ch/twiki/bin/viewauth/CMS/PixelOfflinePlots