Serial powering and signal integrity characterisation for the TEPX detector for the Phase-2 CMS Inner Tracker

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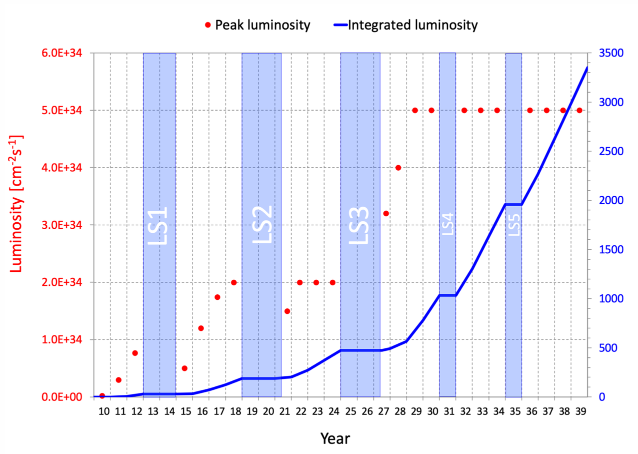
The High-Luminosity LHC

The LHC and its accelerator complex will be upgraded in order to provide more data to the experiments.

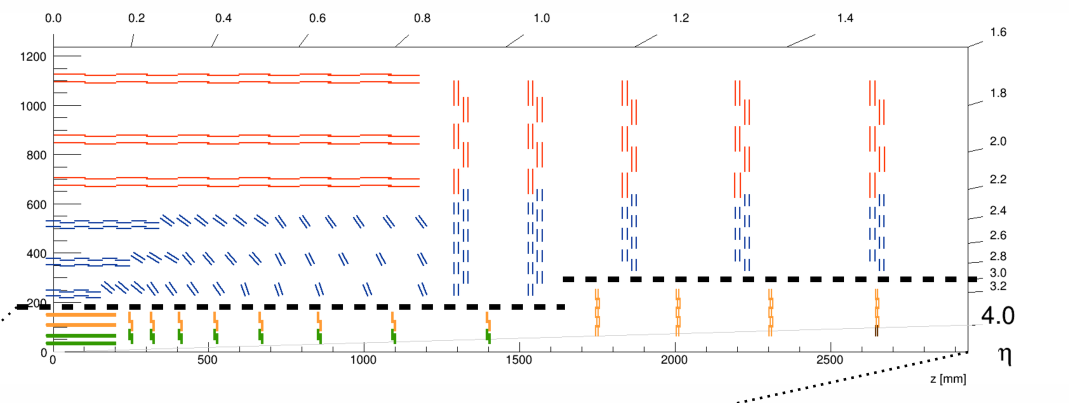
The HL-LHC is expected to deliver 4 ab^{-1} of collisions to the ATLAS and CMS experiments over its lifetime.

This extremely large dataset will allow for precision Standard Model measurements, even of rare processes such as 4-top production and rare higgs decays. Simultaneously, it will enable searches for new physics beyond the Standard Model.



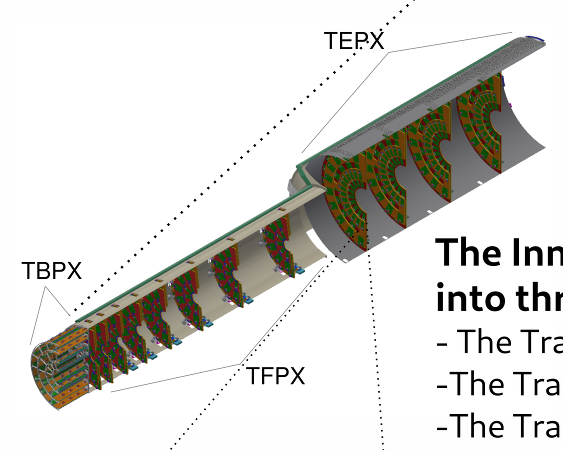
The CMS Phase-2 Inner Tracker

The CMS Tracker will be replaced with an upgraded system which will improve on the current system while also dealing with the high data-rate and radiation at the HL-LHC.



Outer Tracker:
2S (Strip-strip sensor modules)
PS (macro-pixel strip sensor modules)

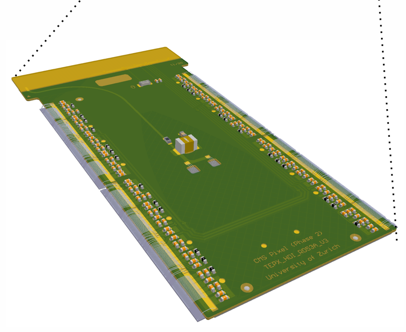
Inner Tracker:
2x2 pixel chip modules
2x1 pixel chip modules



The Inner Tracker is divided into three subsystems:
- The Tracker Barrel Pixels (TBPX)
-The Tracker Forward Pixels (TFPX)
-The Tracker End-Cap Pixels (TEPX)

System Overview

4.87 m^2 of active silicon
4352 modules
1.95 billion readout channels
40 kW front-end power



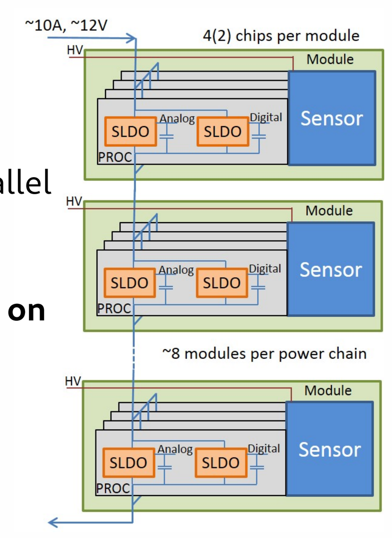
Individual pIxel modules consist of pixel sensors attached to either 2 or 4 readout chips and a flex circuit

Pixel sensors of thin n-in-p silicon with pixel sizes of either 25 x 100 or 50 x 50 microns are bump bonded to the readout chips.

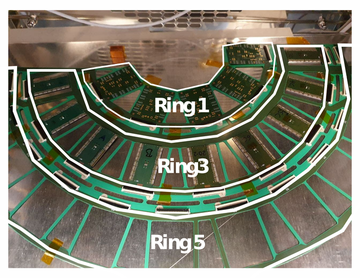
Module Powering Scheme

- **Modules powered in series**
- chips within each module powered in parallel
- High-Voltage delivered in parallel to the modules

A **Shunt-LDO regulator (SLDO) on each chip** provides voltage regulation for each chip while maintaining a constant current drain.



Communication Tests in the TEPX Disk



Establish powering and communication in the TEPX disk.
Tests performed on:
Ring 1: 5 Modules, 15 data lanes
Ring 3: 9 Modules, 9 data lanes

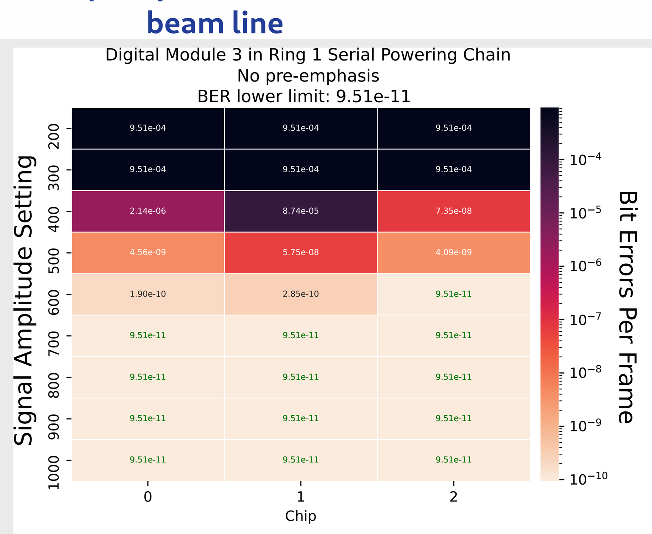
fewer data lanes at higher radius, due to lower pixel occupancy further from the beam line

Data transmission at 1.28 Gb/s

- **Most Chips establish communication with default settings**
- Sometimes adjustments of signal amplitude and pre-emphasis are required
- **Further improvements expected** in final setup with impedance matched cables
- On-going studies into cross-talk and interference between data lanes
- **Expanding to also test Ring 5**

On- chip registers are used to control the signal amplitude and pre-emphasis on the data streams.

Study the bit error rates (BER) as a function of amplitude and pre-emphasis settings

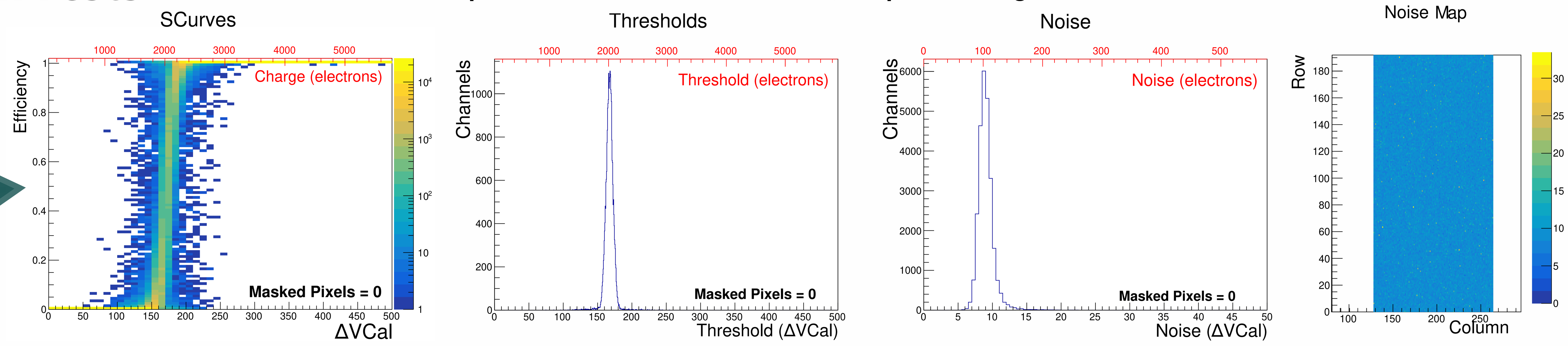


Module Tuning + System Tests

Tuning Procedure

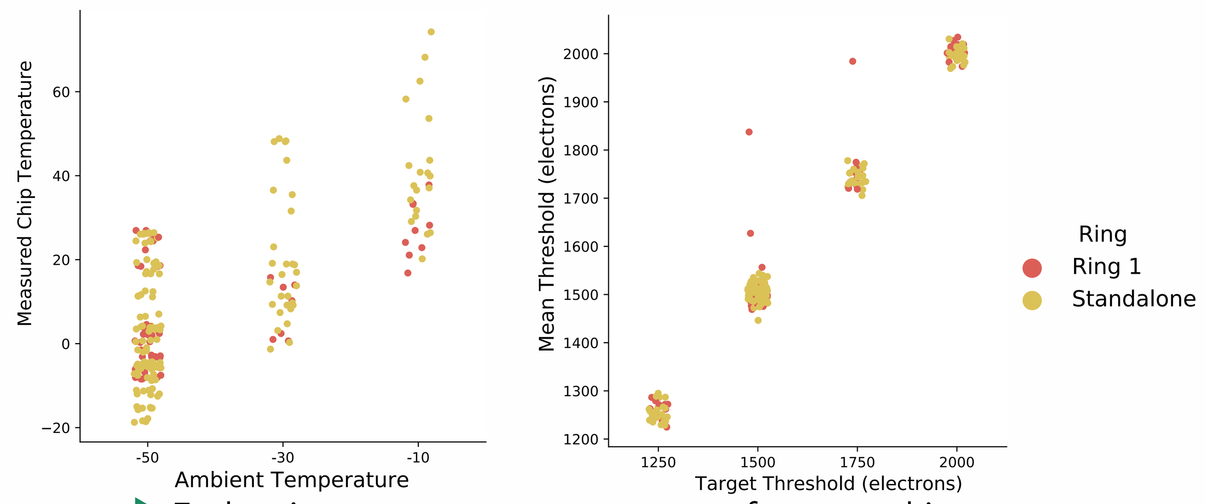
- remove unresponsive pixels
- equalize channels
- remove noisy channels
- adjust thresholds
- re-equalize channels
- remove noisy channels
- final SCurves

Example Results: Sensor Module #1, Chip #1 in Ring 1



Systematic Comparison of Module Tuning Performance : Standalone vs. Serial Powering Chain

Running Conditions



Each point represents a measurement from one chip

Test Setup:
Run automated calibration procedure for available modules under various conditions:

- Ambient Temperatures (inside climate chamber):
-50 C, -30 C, -10 C

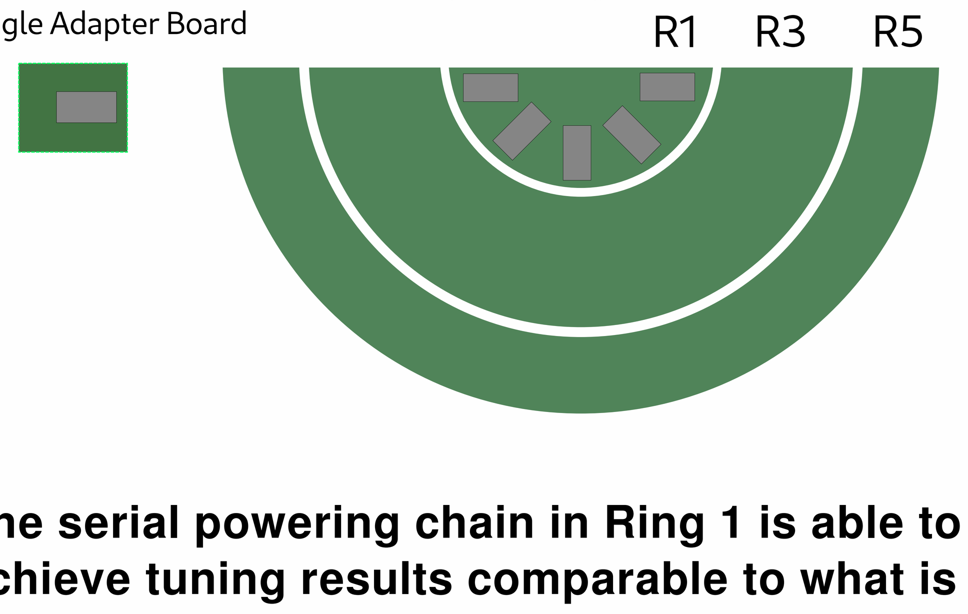
- Target Thresholds:
2000e, 1750e, 1500e, 1250e

- Standalone (Single Adapter Board) and in a Serial Powering Chain (Ring 1 with 5 modules)

Validate the module performance in the serial powering chain

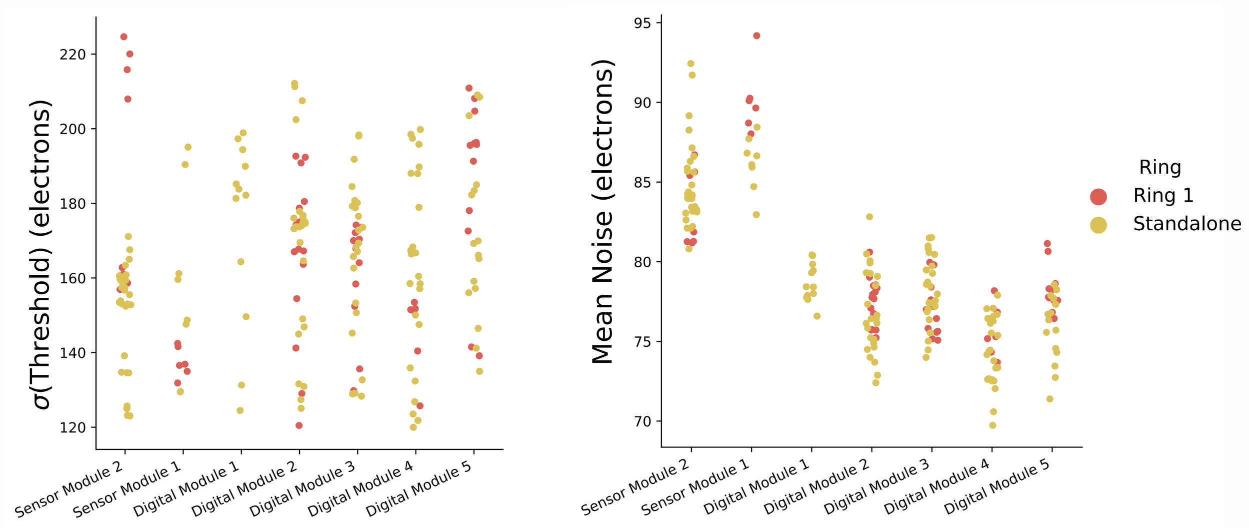
Comparisons made for 7 modules
(2 modules with sensors + 5 "digital" modules without sensors)

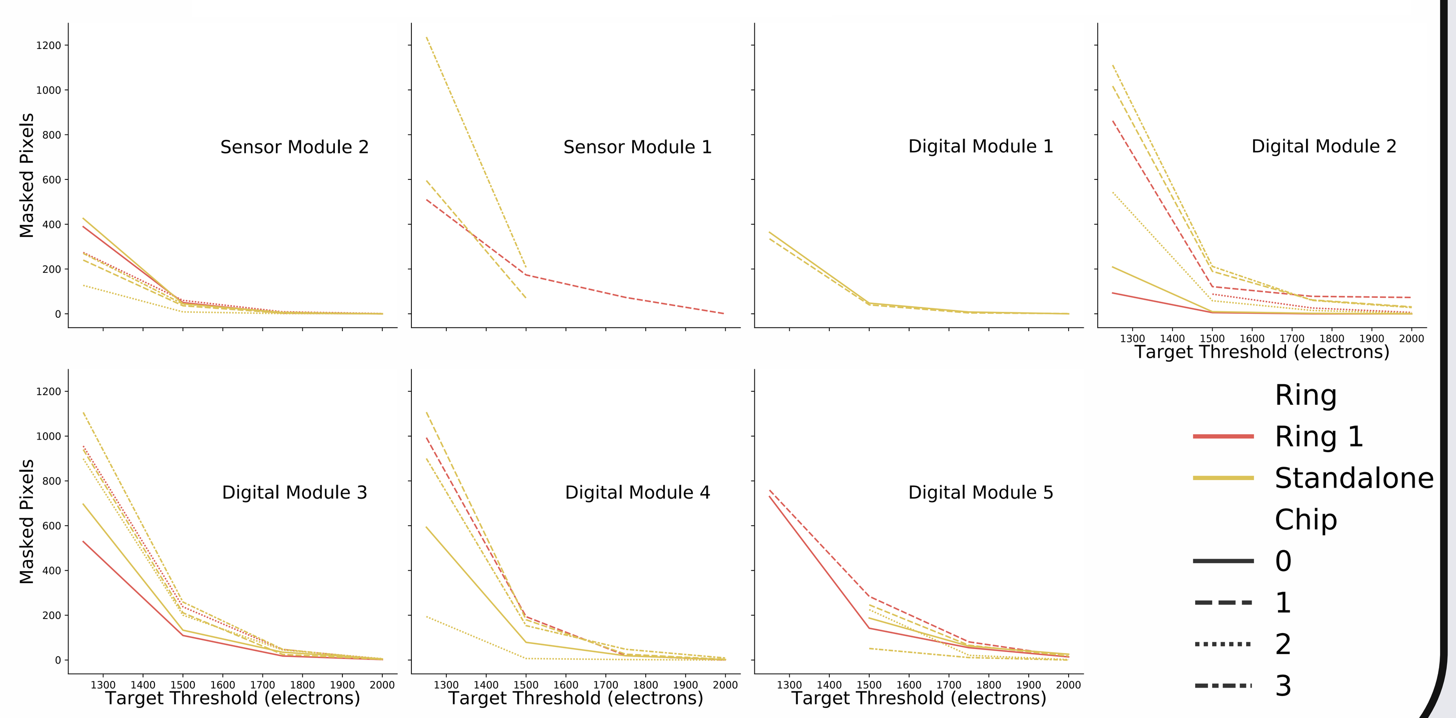
Sensor modules are biased with a voltage of -50V



The serial powering chain in Ring 1 is able to achieve tuning results comparable to what is achieved in a standalone setup

Tuning Performance





masked pixels at -50 C ambient temperature