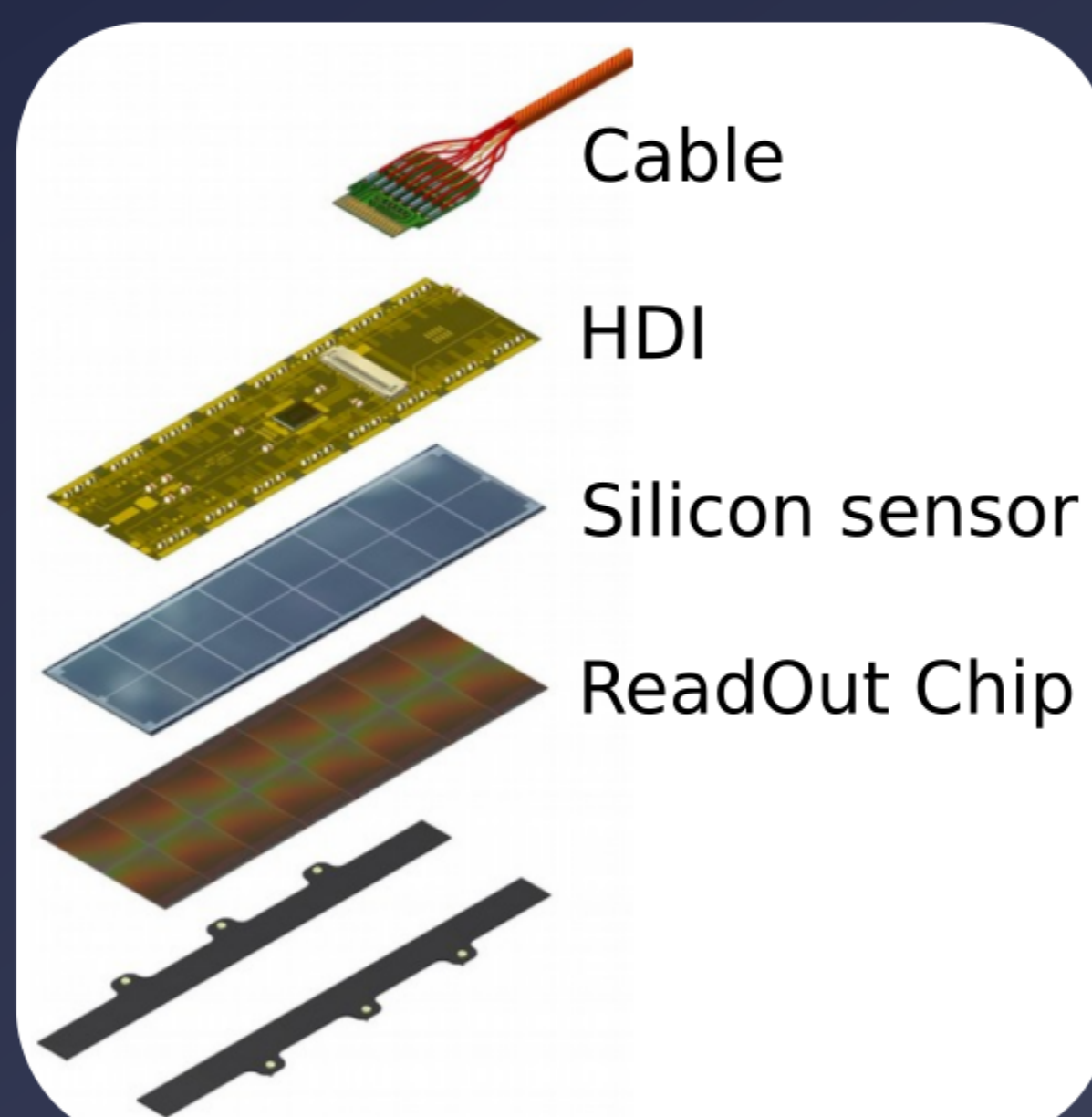


CMS Phase-1 Pixel detector refurbishment during LS2 and readiness towards the LHC Run-3

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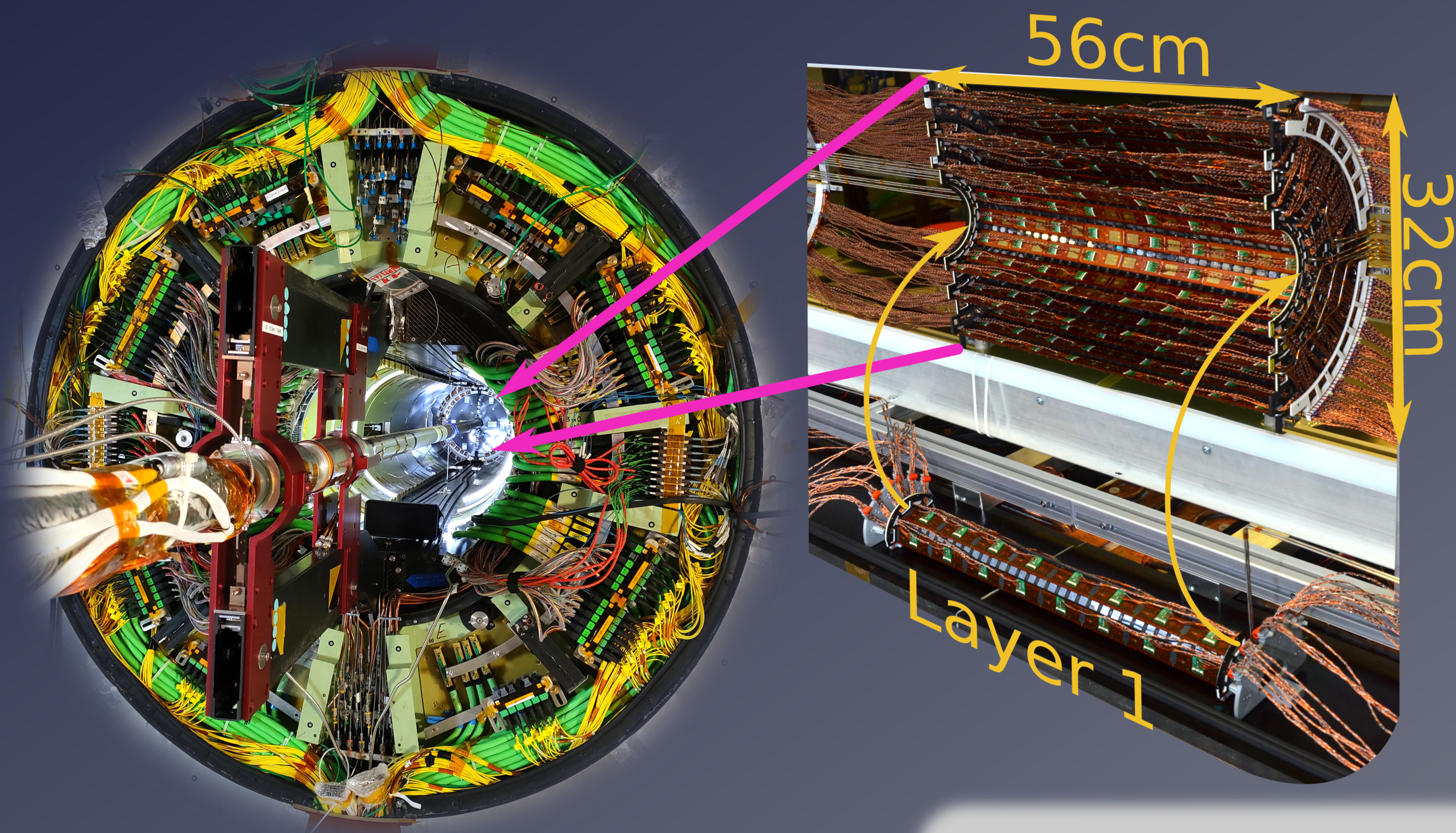
CMS Pixel Detector

- Closest subdetector to collision point
- Precise track position information
- Composed of 4-layer Bpix and 2x3 disks FPix
- 124 Mio. readout channels
- 40 MHz triggered readout
- 1184 pixel modules in BPix
- 672 pixel modules in FPix



Barrel Pixel Modules

- 285 μm thick planar silicon sensor
- 250 nm CMOS ASIC ReadOut Chips (ROCs)
- Pixel size 100 μm \times 150 μm
- Module readout rate of 400Mbit/s
- Layer 1 designed to withstand a particle rate of 600 MHz cm^{-2}
- Readout via unshielded twisted pair cables



**Pixel tracker working fraction:
Run 2 93.5% \rightarrow Run 3 > 99%**

Phase-1 pixel detector deployed in LHC Run 2 (2017 - 2018)

- About 120 fb^{-1} data taken
- Most radiation damage on layer 1 modules (closest to collisions)
- Layer 1 HV ramped from 150 V to 450 V

New layer 1 needed for Run 3

- More than twice as much data expected to be taken in Run 3
- Fluence in L1 would exceed operational limits

Design improvements in layer 1

- New layer 1 HV can be ramped upto 800 V
- Fixed data sync. loss issues in ROCs
- Lower thresholds through better electrical shielding in ROCs
- Protection against single-event upsets in Token Bit Manager

Refurbishments during LS2

- BPix extracted from the CMS detector
- Stored in a cold box
- New layer 1 was built (started in 2020) and assembled at PSI
- Extraction of old layer 1 from BPix
- Replacing single layer 2 modules
- Reassembling BPix
- New DCDC converters
- Repair of faulty connections

Checks done in the CERN clean room and after reinstallation

- Power + HV
- Optical fibers
- Electrical data links (programming and readout)
- Tested up to functioning pixel level
- Tested from approx. 20 $^{\circ}\text{C}$ to -20 $^{\circ}\text{C}$
- Further calibrations and cosmic data taking ongoing