A 4.6GHz to 5.6GHz Low Jitter ASIC in 55nm CMOS for High Energy Physics Experiments

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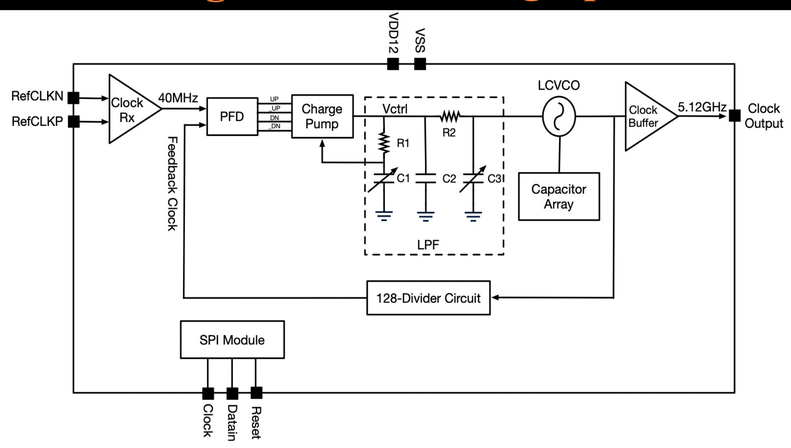
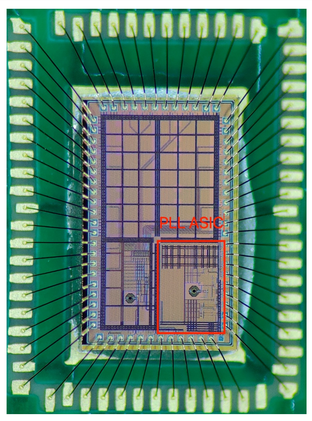
Introduction

Low jitter and radiation tolerant Phase-Lock-Loop (PLL) has been prevailingly researched and commonly used in high energy physics experiments. This paper presents the design and test results of a radiation tolerant, 4.5GHz to 5.6GHz PLL ASIC fabricated in 55 nm CMOS technology. This ASIC is part of the optical link ASICs in the Nuclotron-based Ion Collider Facility (NICA) front-end readout electronics. In order to obtain low DC leakage current and reduce dynamic mismatch, the charge pump uses two unity-gain feedback operational amplifiers to keep the output common mode voltage constant. To obtain a wide range of frequency, the LC voltage-controlled oscillator (LCVCO) can change the oscillation frequency by adjusting the capacitance value of the novel capacitor array. The tuning capacitor array consists of MOM capacitor units with three binary-controlled NMOS switches and two big resistors. Besides, the LCVCO can improve the Q factor degradation due to the source/ drain leakage current from the binary controlled NMOS transistor. All adjustable bits can be controlled by the SPI module, which is also strengthened with the Triple Modular Redundancy (TMR) structure for radiation tolerant consideration. The whole ASIC features a size of 1200 μm × 900 μm. The test results show that the PLL covers a wide-frequency range from 4.6GHz to 5.6GHz, consuming a total power of 36 mW. The peak-to-peak differential amplitude is 320 mV with the duty cycle of 51.8%. At 5.12GHz, the total jitter is 13.3 ps with the RMS jitter of 880fs and the phase noise is -108dBc/Hz @ 1MHz offset.

Block diagram and Photograph



Block diagram of PLL ASIC

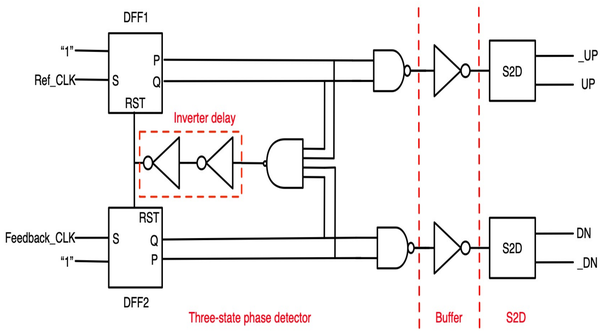


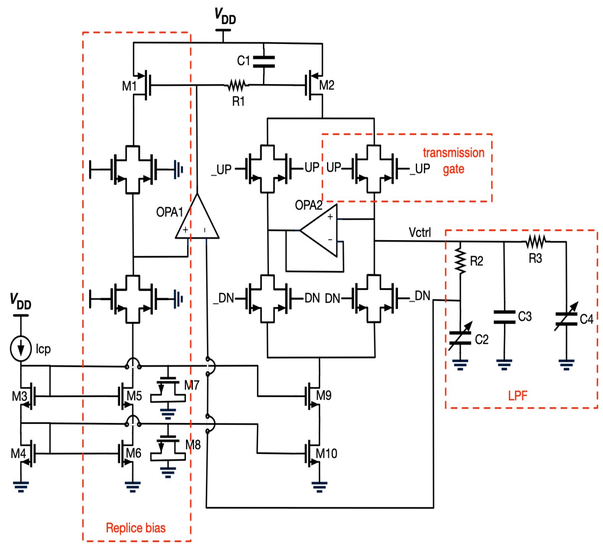
Wire-bonded chip under the microscope

◆ The PLL ASIC consists of a clock receiver circuit, a phase-frequency detector (PFD), a charge pump (CP), a low-pass filter (LPF), a LC voltage-controlled oscillator (LCVCO), a capacitance array, a 128-divider circuit and SPI module.

◆ The PFD detects the phase difference between the single clock signal and feedback clock signal, and then transforms it into an electrical signal. The CP controlled by the up or down signal generated by the PFD, will source current to the LPF or sink current from the LPF, resulting in the LCVCO control voltage. The control voltage is used to fine-tune change the oscillating frequency of the LCVCO and the capacitor array provides 8-bit digital coarse frequency tuning. Finally, the LCVCO feeds its output into the 128-divider circuit to maintain the closed-loop stability.

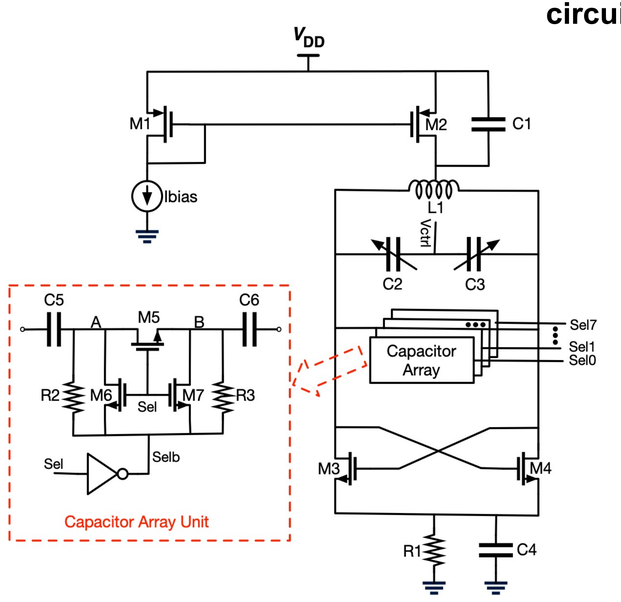
The design of VCSEL driver ASIC





PFD circuit

Charge pump circuit



LCVCO circuit

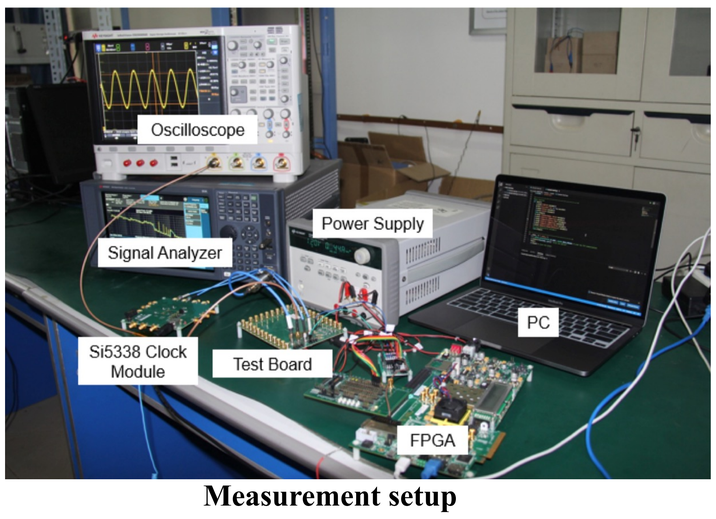
◆ To avoid the dead zone occurring when the phase errors are close to zero and reduce the LCVCO noise leakage due to the dead zone, the delay blocks implemented by inverters give a 700ps width to the PFD output pulses.

◆ In order to obtain low DC leakage current and reduce dynamic mismatch, the CP uses two unity-gain feedback operational amplifiers to keep the CP output common mode voltage constant.

◆ To obtain a wide range of frequency, the LC voltage-controlled oscillator (LCVCO) can change the oscillation frequency by adjusting the capacitance value of the novel capacitor array. The tuning capacitor array consists of MOM capacitor units with three binary-controlled NMOS switches and two big resistors. Besides, the LCVCO can improve the Q factor degradation due to the source/ drain leakage current from the binary controlled NMOS transistor.

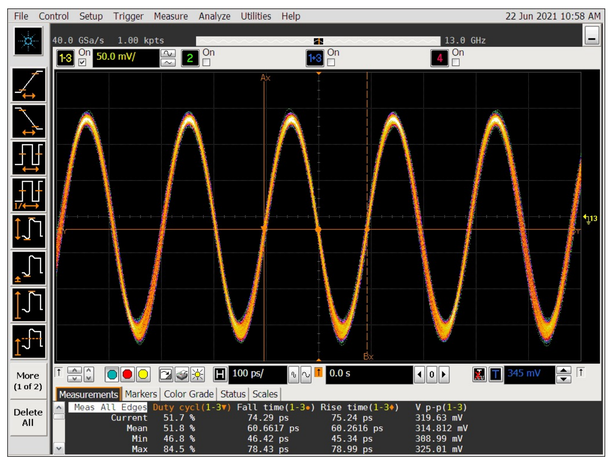
Measurement results

◆**Measurement setup**：During the test, the ASIC is wire bonded to a print circuit board. The input reference clock and the output clocks are transmitted through microstrips and SMA connectors. The input clock is frequency adjustable square wave signals generated by a clock module (Silicon Labs Si5338-EVM). The output clock is monitored using a real-time oscilloscope (keysight InfiniiVision DSOX6004A) and a signal analyzer (keysight EXA Signal Analyzer N90100).

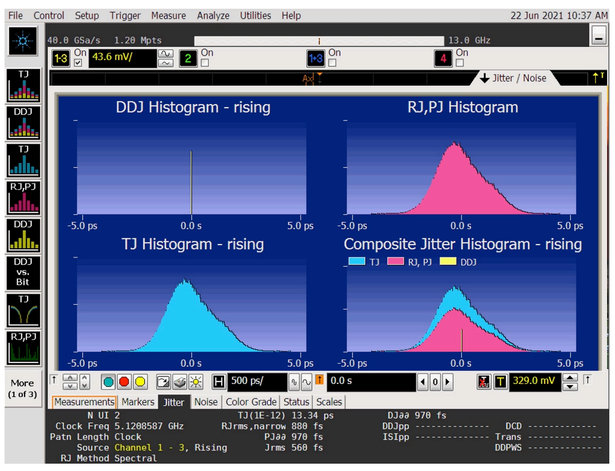


Measurement setup

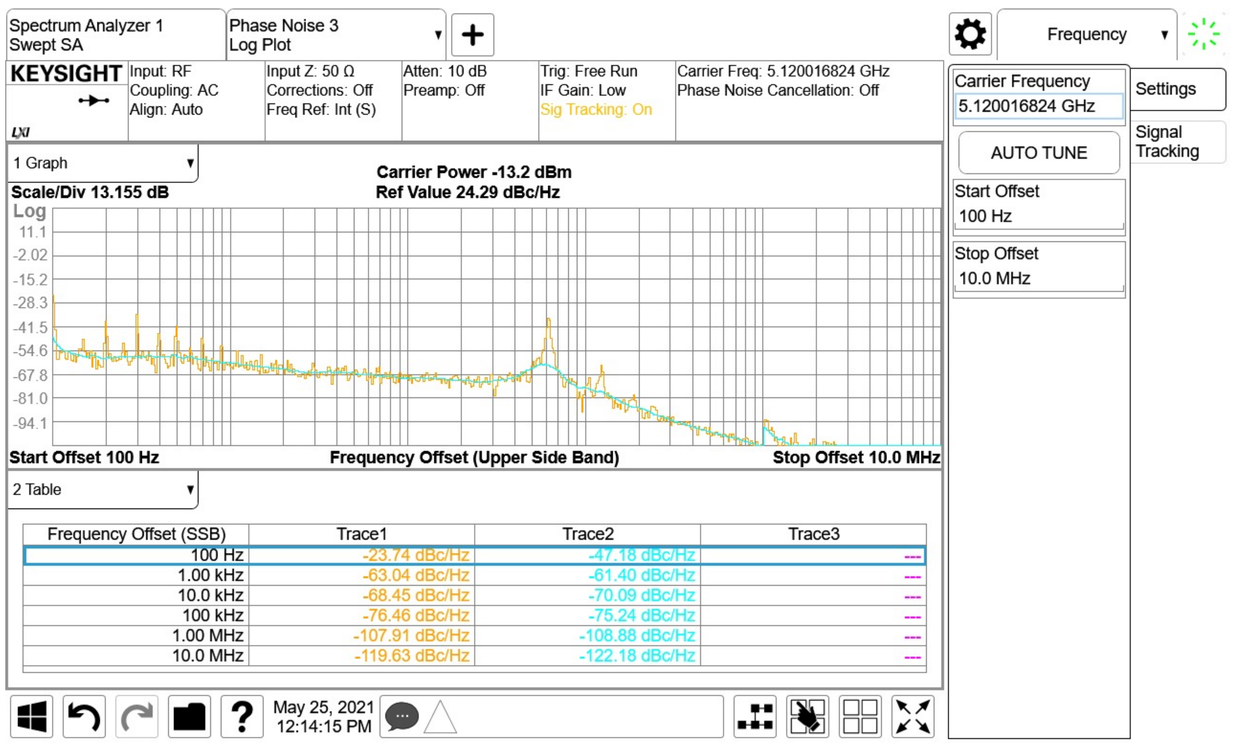
◆**Measurement result**：The test results shows that the peak-to-peak differential amplitude is 320 mV with the duty cycle of 51.8%. At 5.12GHz, the total jitter is 13.3 ps with the RMS jitter of 880fs and the phase noise is -108dBc/Hz @ 1MHz offset.



Waveform of the PLL output clock



Jitter analysis results



Phase noise performance result

Acknowledgments

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