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A radiation tolerant 16 Gbps 1:16 Deserializer for High-Energy Physics Experiments

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Deserializer with high speed and radiation tolerant features is used as key component of data transmission system in high-energy physics experiments. It is mainly used in the downlink transmission to realize serial-to-parallel conversion of data. This paper presents the design and test results of a 16 Gbps 1:16 deserializer chip fabricated in 55 nm CMOS technology. The chip adopts a tree-type tap structure, consisting of an input equalizer stage, four levels of half-rate 1:2, 2:4, 4:8, 8:16 Demultiplexer (DEMUX) modules, corresponding frequency dividers. The input equalizer stage is used to compensate for the high frequency loss caused by the transmission line on PCB and the bonding wire. The first 1:2 DEMUX receives the 16Gbps CML signals from the equalizer stage, performs the first 1:2 transform, then transmits to the following levels. The final 8:16 DEMUX outputs 16 parallel data with 1 Gbps. The frequency divider divides the externally input 8GHz clock to provide a half-rate clock for each stage of DEMUX. In order to improve the bandwidth of the high-speed 1:2 DEMUX and high-frequency divider, and save voltage margin, their latches adopt a CML structure without tail current source. We designed duty cycle correction circuit and clock alignment circuit to recover duty cycle and align clock edges in clock path.

The whole chip consumes 305 mW when working at 16 Gbps. The dimension of the designed deserializer chip is 2mmX3mm, including 58 PADs. The post-layout simulation results demonstrate that the whole chip work functionally at the target speed and 16 wide-open eyes are verified at the all output channels. The total jitter (TJ) of each output channel (1 Gbps/ch) is 28.2ps averagely. This chip has been taped out and the tests are planned to be conducted in this March. The test results will be reported in the meeting.

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