A radiation tolerant 16 Gbps 1:16 Deserializer for High-Energy Physics Experiments

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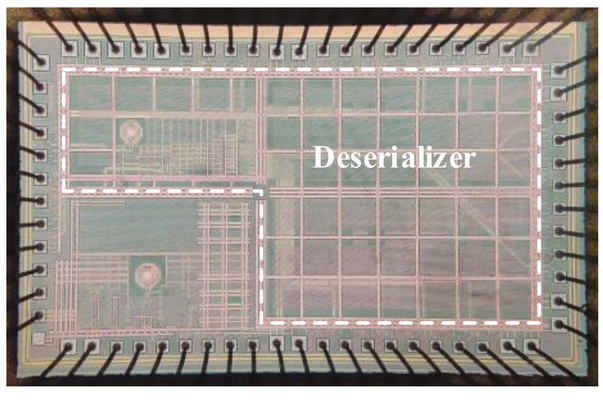
Introduction



16 Gbps 1:16 Deserializer

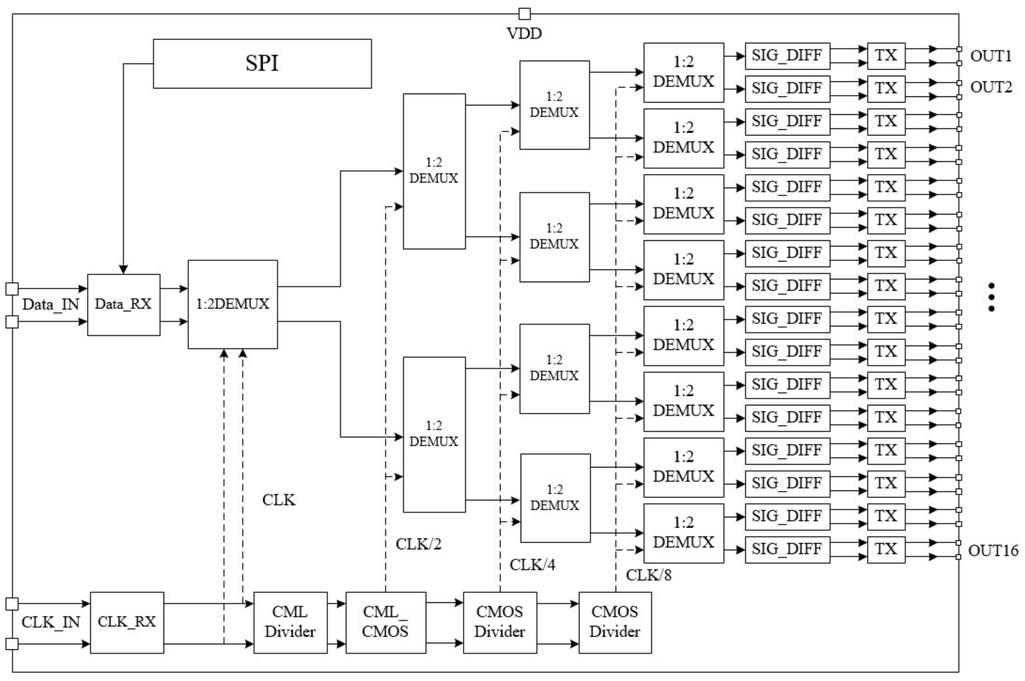
◆The 16 Gbps 1:16 Deserializer ASIC is used to realize serial-to-parallel conversion of data, which fabricated in 55 nm CMOS technology. The Deserializer with high speed and radiation tolerant features is used as key component of data transmission system in high-energy physics experiments.

◆The Deserializer adopts a tree-type tap structure, consisting of an input equalizer stage, four levels of half-rate 1:2, 2:4, 4:8, 8:16 Demultiplexer (DEMUX) modules, corresponding frequency dividers, and LVDS output drivers.

◆The dimension of the Deserializer is 2 mm × 3.33 mm, including 58 PADs.

◆The Deserializer has completed the output data logic test and eye diagram test at 10 Gbps and 13 Gbps, the total ionizing dose (TID) test will be performed.

The design of Deserializer

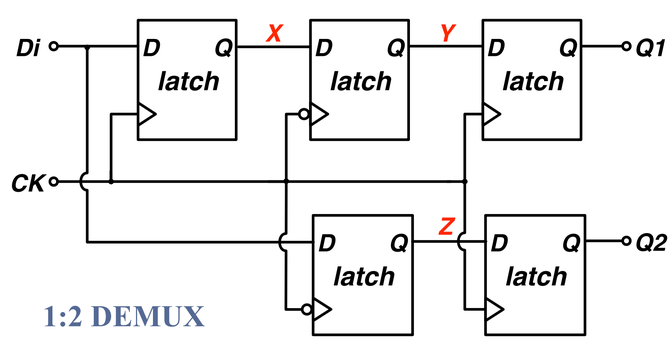


Block diagram of Deserializer

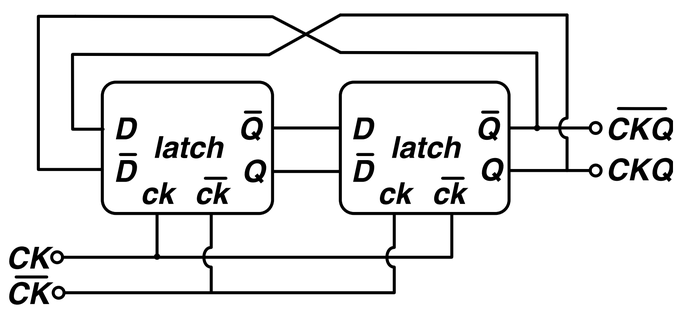
◆The Deserializer is mainly composed of 1:2 DEMUX and a divider-by-2 circuit.

◆ 1:2 DEMUX and 2:4 DEMUX are implemented by CML latches, 4:8 DEMUX and 8:16 DEMUX are realized by the CMOS latches.

◆The divider-by-2 of first stage adopted a D flip-flop (DFF) formed by two CML latches to realize, and the latter two divider-by-2 are realized by CMOS structure.

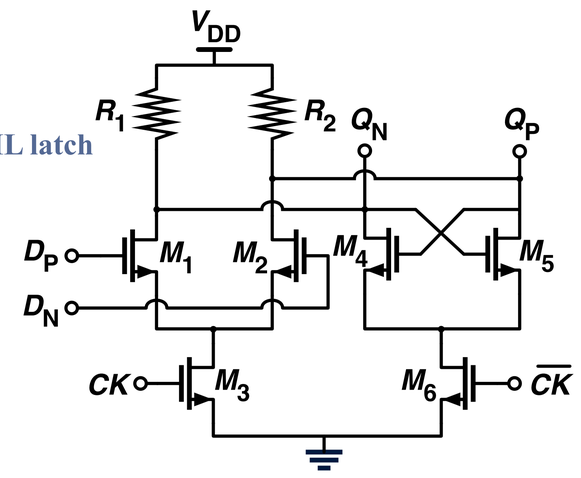


1:2 DEMUX



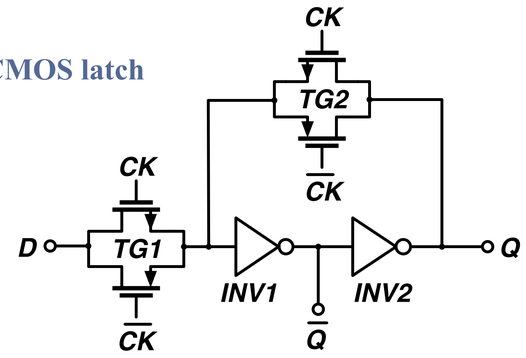
Divider-by-2 with CML latch structure

CML latch



◆The 1:2 DEMUX is consist of five latches. Both high-speed 1:2 DEMUX and low-speed 1:2 DEMUX use the same structure, the difference is that they are implemented by CML latches and CMOS latches respectively.

CMOS latch

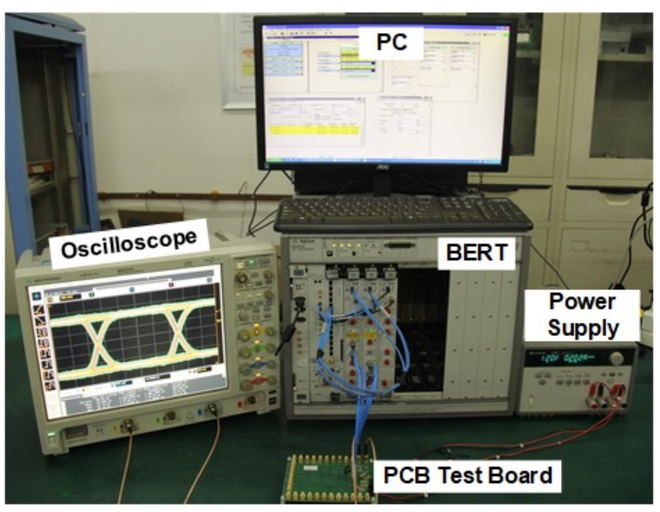


◆In order to improve the bandwidth of the high-speed 1:2 DEMUX and high-frequency divider, and save voltage margin, their latches adopt a CML structure without tail current source.

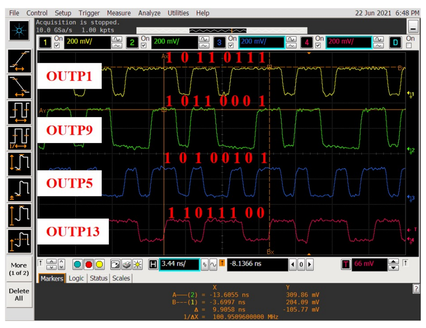
◆The low-speed 1:2 DEMUX and low-frequency divider use CMOS latches to minimize power consumption.

Logic and eye diagram testing set up and test results of Deserializer

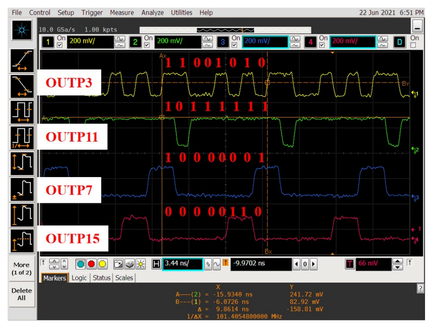
Input data:1111111000000100000110000101000111100100010111001110101001111101000011100010010011011010110111101100011010010111011100110010100



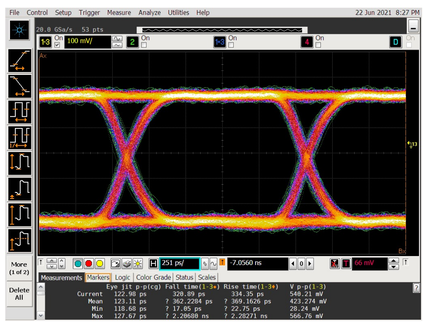
16 Gbps 1:16 Deserializer testing set up



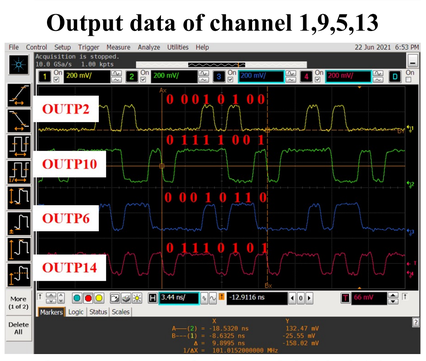
Output data of channel 1,9,5,13



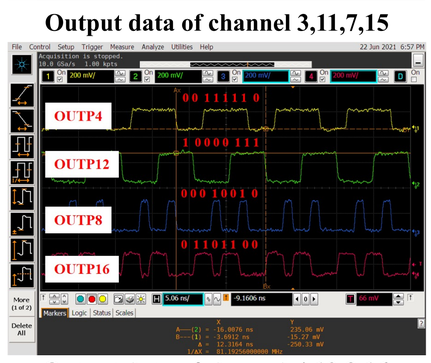
Output data of channel 3,11,7,15



Eye diagram of OUTP2 @812.5MHz



Output data of channel 2,10,6,14



Output data of channel 4,12,8,16

Channel	Theoretical output data	Measured output data
OUTP1	10110111	10110111
OUTP9	10110001	10110001
OUTP5	10100101	10100101
OUTP13	11011100	11011100
OUTP3	11001010	11001010
OUTP11	10111111	10111111
OUTP7	10000001	10000001
OUTP15	00000110	00000110
OUTP2	00010100	00010100
OUTP10	01111001	01111001
OUTP6	00010110	00010110
OUTP14	01110101	01110101
OUTP4	00111110	00111110
OUTP12	10000111	10000111
OUTP8	00010010	00010010
OUTP16	01101100	01101100

◆Due to the limitation of the maximum rate of the test instrument, the maximum input data rate can only up to 13Gbps.

◆**Logic Test:** Enter a string of determined data at 13 Gbps, and then test the output data of 16 channels.

◆**Eye Diagram Test:** Input a string of PRBS codes at a rate of 13 Gbps, and then test the eye diagram of each output channel.

Conclusion

◆The Deserializer has completed output data logic test and eye diagram at 13 Gbps input data rate.

◆The irradiation test of Deserializer will be carried out later.

Acknowledgments

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