

# A 14-Gbps VCSEL Driving ASIC in 55 nm for Particle Physics Experiments

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Low power consumption, high bandwidth and radiation tolerant VCSEL driving ASICs have been prevalently researched and used in particle physics experiments. This paper presents the design and the test results of a 14-Gbps VCSEL driving ASIC fabricated in 55 nm CMOS technology.

The whole ASIC includes four independent channels, and each channel has the fixed channel height of 250  $\mu\text{m}$  to keep the whole ASIC as the array form fitting with a four channel VCSEL array. The 14-Gbps VCSEL driver is implemented as one of the four channels. The 14-Gbps VCSEL driver ASIC consists of an equalizer stage, a pre-driver stage and a novel output driver stage. The equalizer stage adopts the Continuous Time Linear Equalizer (CTLE) structure to compensate for the high frequency loss. To obtain the high bandwidth, a shared inductance-peaking technique is used in the pre-driver stage. The proposed novel output driver stage raises the supply voltage and employs the stacked PMOS current source structure to increase the swing amplitude of the driving current to the VCSEL. Besides, two feedforward compensation capacitors are utilized to improve the bandwidth of output driver stage.

The whole ASIC features a size of 2 mm x 2 mm. The 14-Gbps VCSEL driver has a size of 2 mm x 0.25 mm. Widely-open 14-Gbps eye has been observed at the typical settings of 2 mA bias current and 5 mA modulation current in the post layout simulation. The chip has been taped out and the tests are planned to be conducted in this May. The driver ASIC will use chip on board (COB) measurement setup, and is wire bonded to an 850 nm VCSEL. The optical test, electrical test and total ionizing dose (TID) test will be performed. The test results will be reported in the meeting.

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