A 14-Gbps VCSEL Driving ASIC for Particle Physics Experiments

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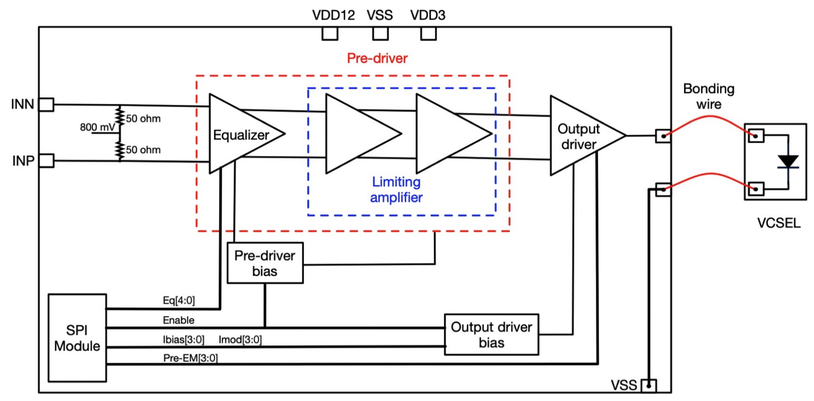
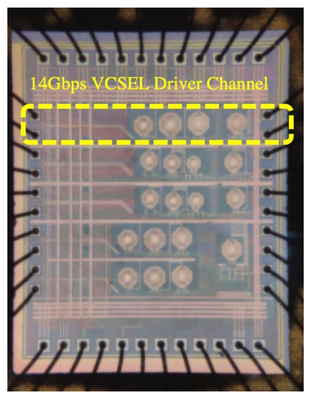
Introduction

Due to the advantages in density, bandwidth and radiation performance of VCSEL-based array optical transmission system, it has been prevailingly researched and used for the front-end data acquisition in high-energy physics experiments. This paper presents the design and the test results of a 14 Gbps Vertical-Cavity Surface Emitting Lasers (VCSELs) driving ASIC with a novel output driver structure fabricated in 55 nm CMOS process. The output driver stage realizes the combination of high power supply and low voltage core MOS transistors (1.2 V), so that the driver chip has a large output voltage headroom, while avoiding the use of high voltage MOS transistors, effectively guarantee the high bandwidth of the output driver circuit. Besides, two feedforward compensation capacitors are utilized to further improve the bandwidth of output driver stage. The test results indicate that the peak-to-peak jitter of 14 Gbps and 10 Gbps optical eye diagram are 16.43 ps and 15.34 ps, respectively. The optical test and total ionizing dose (TID) test will be performed.

Block diagram and Photograph



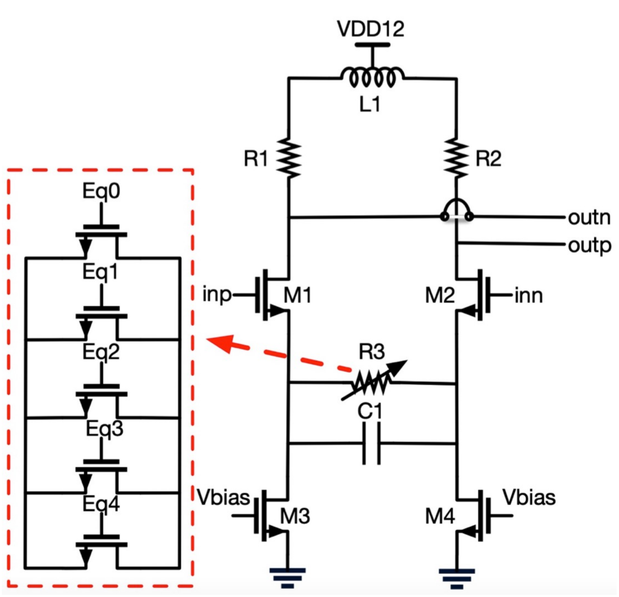
Block diagram of 14 Gbps VCSEL Driver ASIC



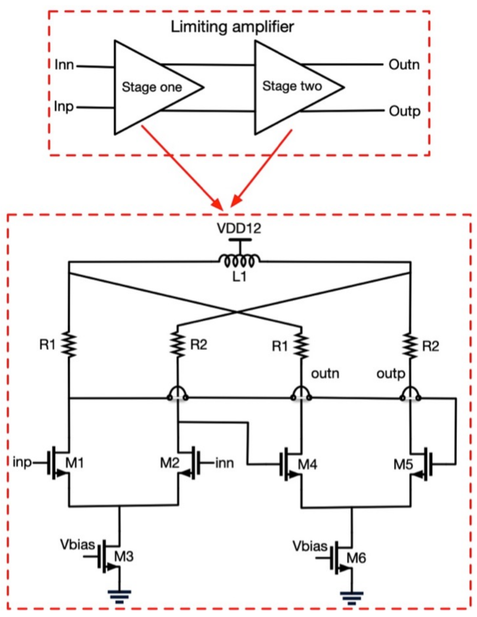
Wire-bonded chip under the microscope

- The 14 Gbps VCSEL driver ASIC is composed of a pre-driver stage, an novel output driver stage and SPI module.
- The input equalizer stage adopts continuous-time linear equalizer (CTLE) structure to compensate the high frequency losses. To obtain sufficient swing and high bandwidth, the pre-driver uses the passive shared inductor structure.
- The output driver stage realizes the combination of high power supply and low voltage core MOS transistors (1.2 V) to increase the output voltage headroom.

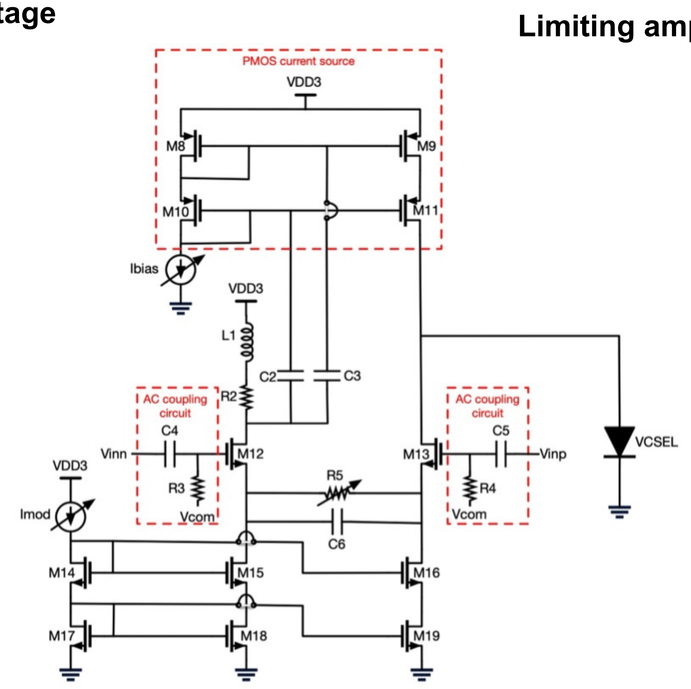
The design of VCSEL driver ASIC



Equalizer stage



Limiting amplifier

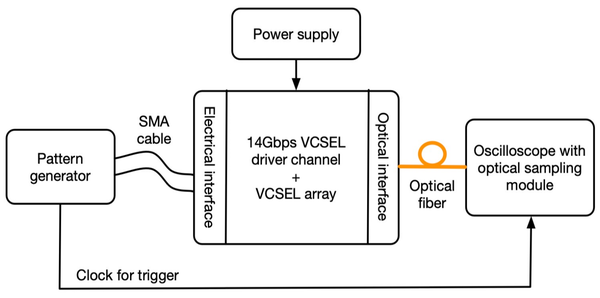


Output driver stage

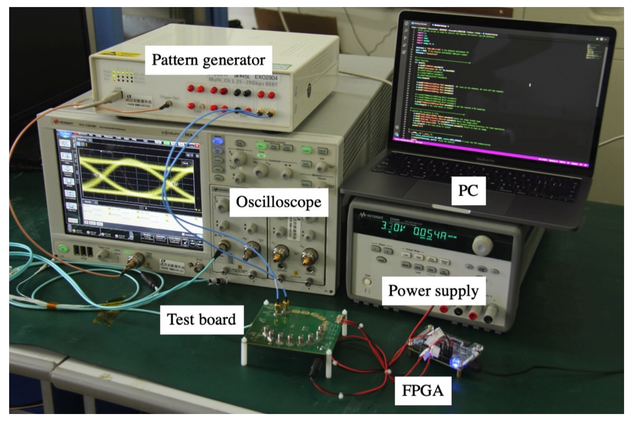
- The input equalizer stage adopts a 5-step continuous-time linear equalizer (CTLE) structure to compensate the high frequency losses from the system level including PCB traces, bonding wires and pads. The CTLE offers the peaking frequency point of 10 GHz while providing a DC gain range of 6.7 dB.
- To obtain sufficient swing and high bandwidth, the pre-driver uses the passive shared inductor structure and active feedback circuit.
- The output driver stage realizes the combination of high power supply and low voltage core MOS transistors (1.2 V), so that the driver chip has a large output voltage headroom, while avoiding the use of high voltage MOS transistors, effectively guarantee the high bandwidth of the output driver circuit.

Measurement results

◆**Measurement setup**：During the test, a pattern generator (EXOSIHT EX02904) provides the high-speed Pseudo-Random Binary Sequence (PRBS) signals with different data rate. The eye diagrams of the 14 Gbps VCSEL driver channel are captured by the oscilloscope with optical sampling module(Keysight DCA-X 86100D). The DC power supply (Keysight E3648A) is used to provide the power supply for the test board.

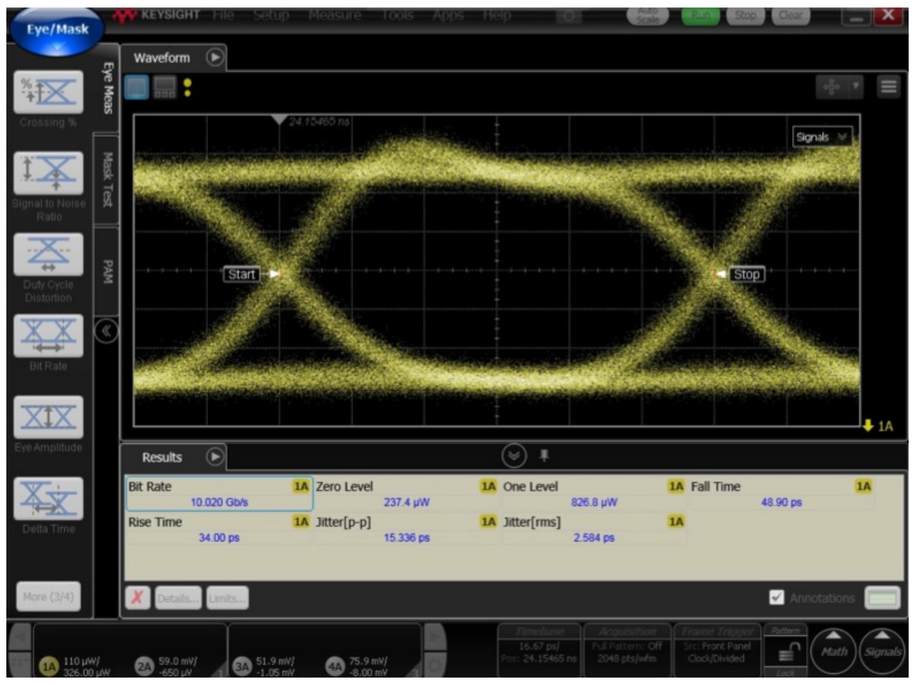


Block diagram of the electrical test

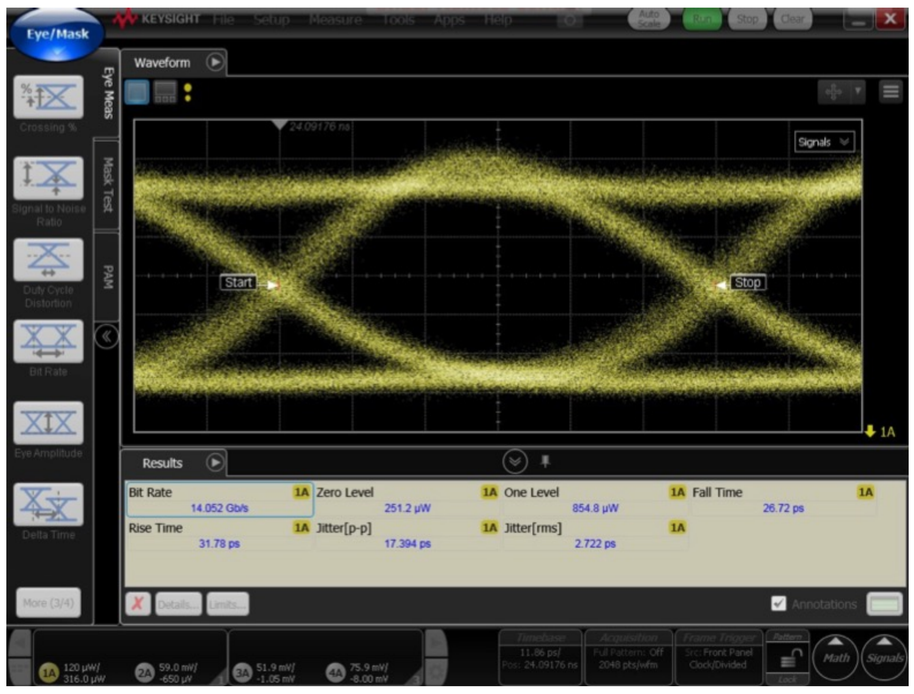


Measurement setup

◆**Eye diagram test**： Wide-open eyes were observed at both 10 Gbps and 14 Gbps. The measured rising and falling edges of the 14 Gbps optical eye were 31.78 ps and 26.72 ps, respectively. The measured RMS jitter was 2.72 ps, and the peak-to-peak jitter was 17.39 ps.



10 Gbps Optical eye



14Gbps Optical eye

Acknowledgments

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