Development of a single-photon imaging detector with pixelated anode and integrated digital readout

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for the 4DPHOTON team

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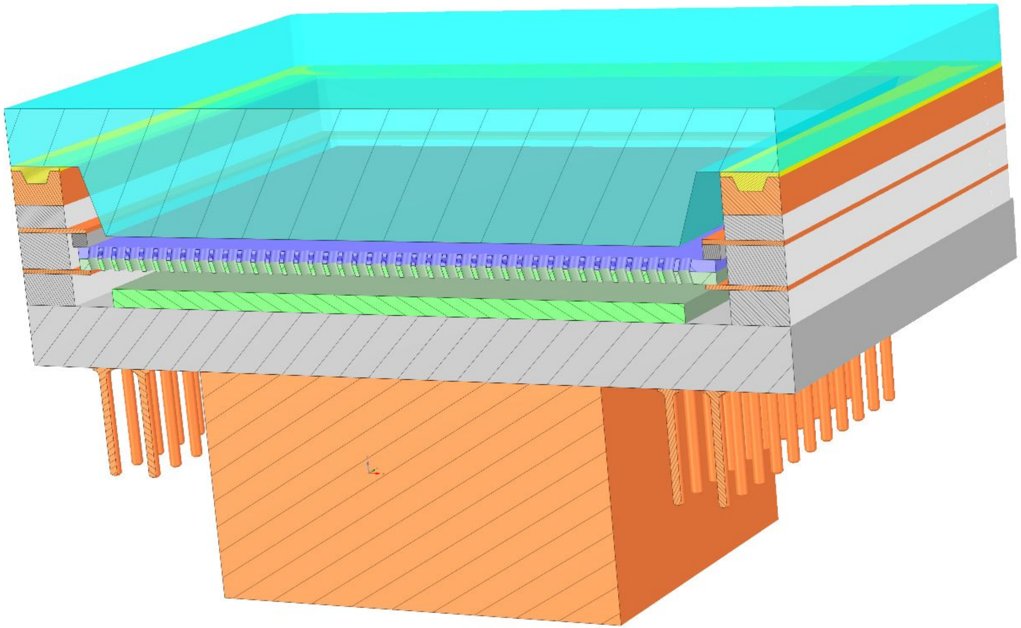
Overview

- The hybrid detector concept
- The Timepix4 ASIC
- Expected performance
- Design status
- The DAQ system



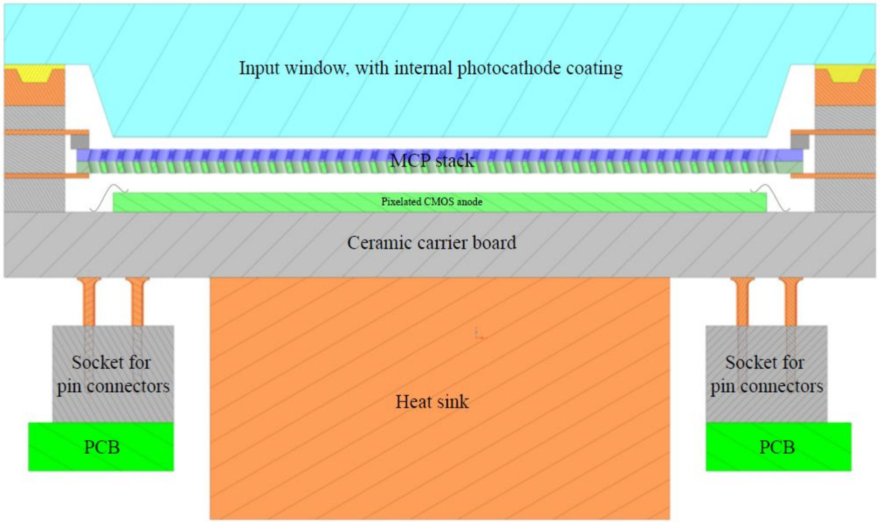
The ‘hybrid’ detector [M. Fiorini et al, JINST 13 (2018) C12005]

We are developing a single-photon detector:

- based on a vacuum tube
- transmission photocathode with high QE in the spectral region of interest
- dual micro-channel plate stack
- a pixelated CMOS read-out anode with integrated front end electronics

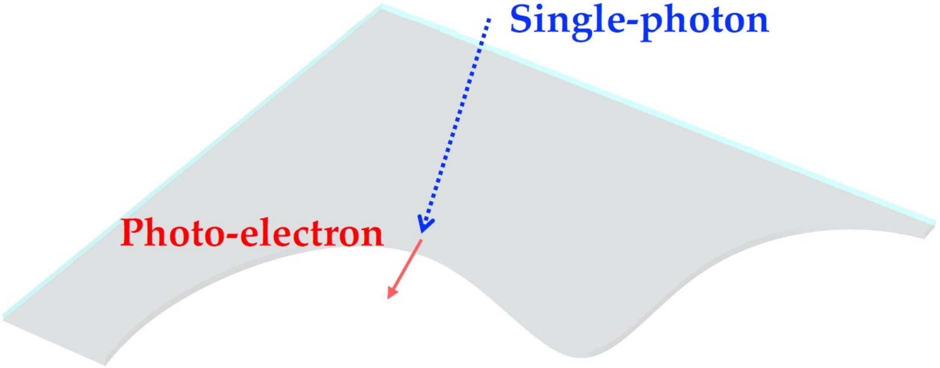
Timing resolution	few 10 ps
Position resolution	5-10 μm
Maximum rate	10^9 hits/s
Dark count rate	10^2 counts/s
Active area	~7 cm^2
Channel density	0.23 M channels

The detector assembly



- Vacuum-based detector
  - Assembly under high vacuum (10^{-10} mbar)
- Assembly and bonding to minimize distance between components
- High-speed connections through pins in ceramic carrier board
  - custom PGA - 2.54 mm pitch
  - socket for detector I/O and low voltage
- Heat sink under AISC
  - Assembly < 21° C with ASIC @ peak power
- PCB allows connection to FPGA-based DAQ system

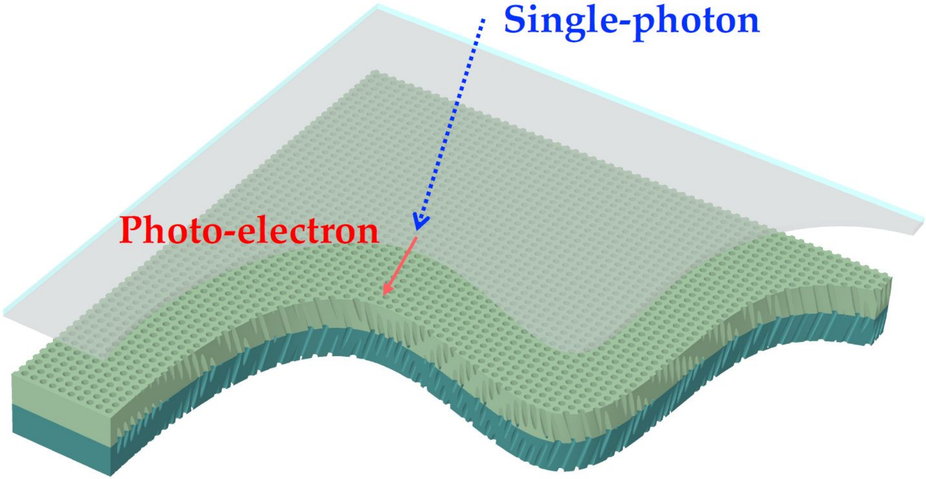
The hybrid detector: entrance window + photocathode



Photon conversion using high Quantum Efficiency (QE) Photocathode

- E.g. bialkali photocathode
  - 40-50% QE
  - 10^2 Hz dark count rate @300 K
  - Best for timing
- Flexible design allows to use different photocathodes

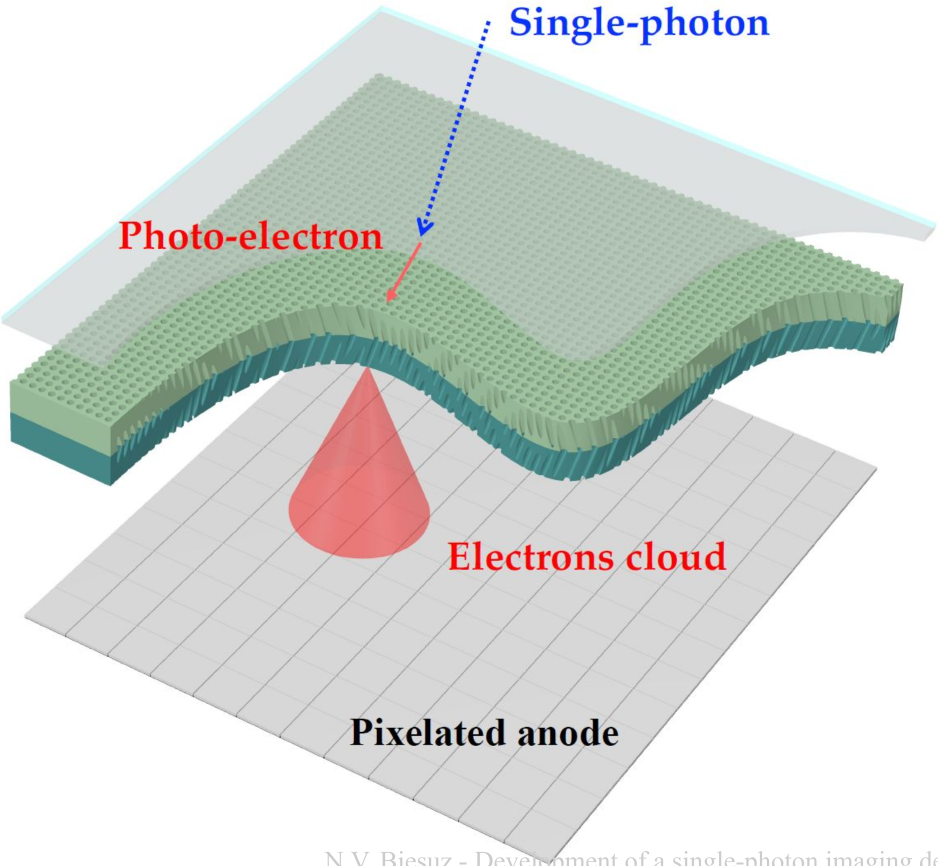
The hybrid detector: microchannel plate stack



Microchannel plate stack (chevron)

- $> 10^4$ gain
- 5 µm pore size
- Atomic layer deposition for increased lifetime:
  - >20 C/cm^2
- Short distance from MCP to cathode and anode for best time and position resolution

The hybrid detector: pixelated anode

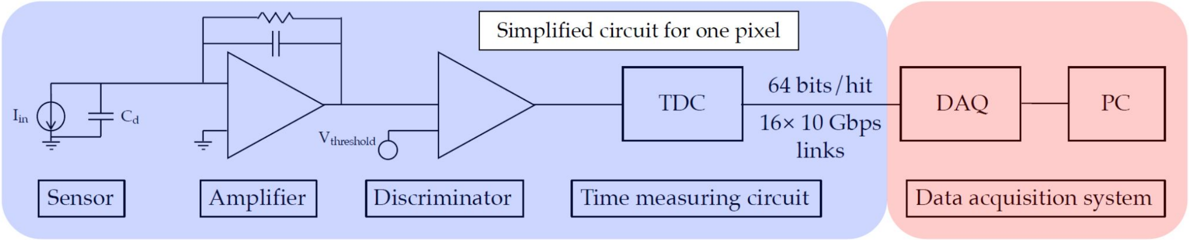


Pixelated anode

- Electron cloud spread over a number of pixels
- Anode is an ASIC
- it integrates digital and analog front-end
  - pixels coordinates
  - pixels Time of Arrival
  - pixels Time over Threshold
- Output:
  - 64 bits of data per event and per pixel with 64B/66B encoding
  - transmitted on 16 high speed links @ 10 Gbps

The Timepix4 ASIC

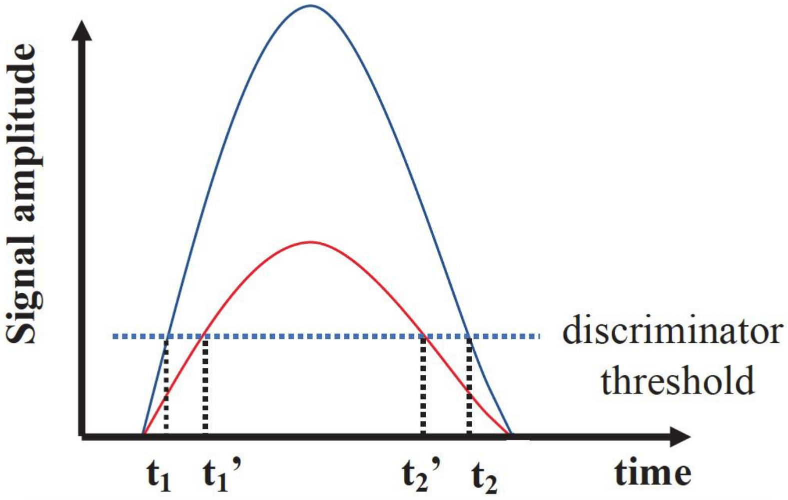
- Timepix4 ASIC in 65nm CMOS
  - Developed by the Medipix Collaboration for hybrid pixel detectors



- 512 x 448 pixels (use bump pad as anode)
  - square pitch: 55 μm
- Integrates Time to Digital Converter (TDC)
  - 195 ps bin size (56 ps rms resolution)
- High data rate capability
  - 160 Gbps
  - $5\ 10^9$ hits/mm^2/s
- Large Active Area: 6.94 cm^2

The Timepix4 ASIC: improving resolution

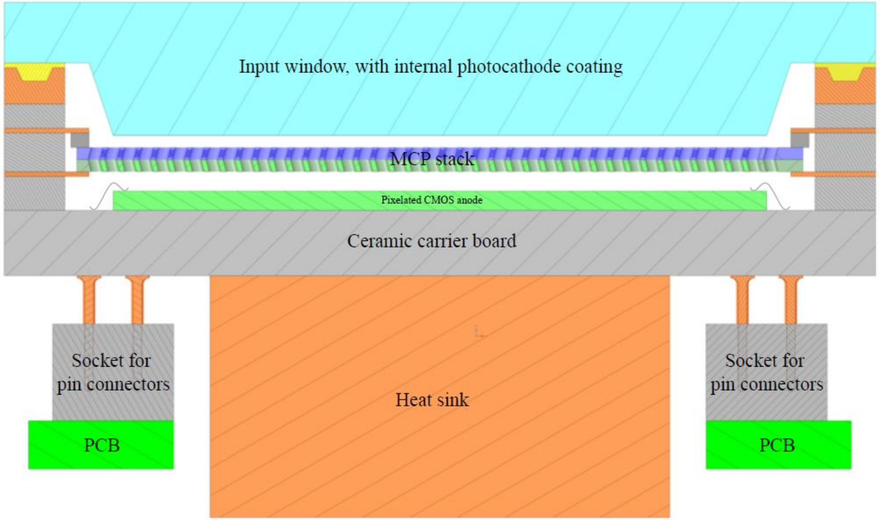
- For each pixel, it provides combined measure of:
  - Time-of-Arrival [t_1]
  - Time-over-Threshold [t_2 - t_1]
- Time over Threshold used to:
  - Correct for time-walk effect [t_{1-} t_1']
  - Improve resolution on cluster centroid
    - ~16μm → ~5μm
  - 3D clustering (space and time)
    - Improve timing resolution by multiple sampling
    - Cluster Time of Arrival Resolution few 10s ps



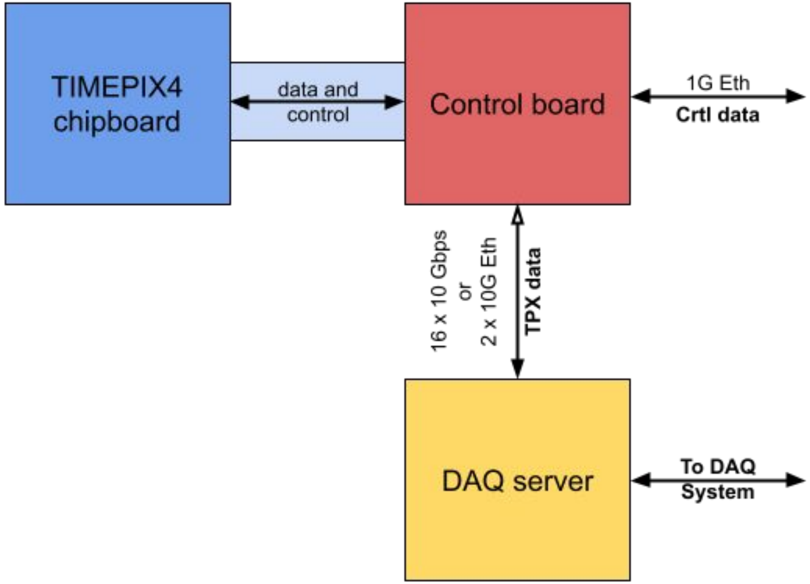
Design status

- 2nd version of the Timepix4 ASIC available by the end of the year
  - 2021 dedicated to study of the ASIC
- ceramic carrier and tube design ongoing
  - estimated production 2022

Assembly and production of tubes foreseen in 2022



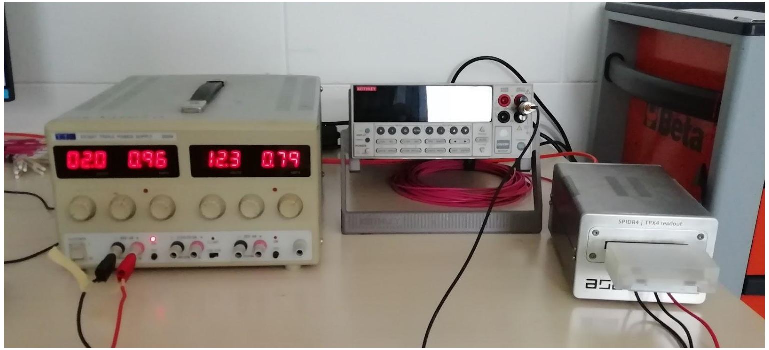
The Data Acquisition system architecture

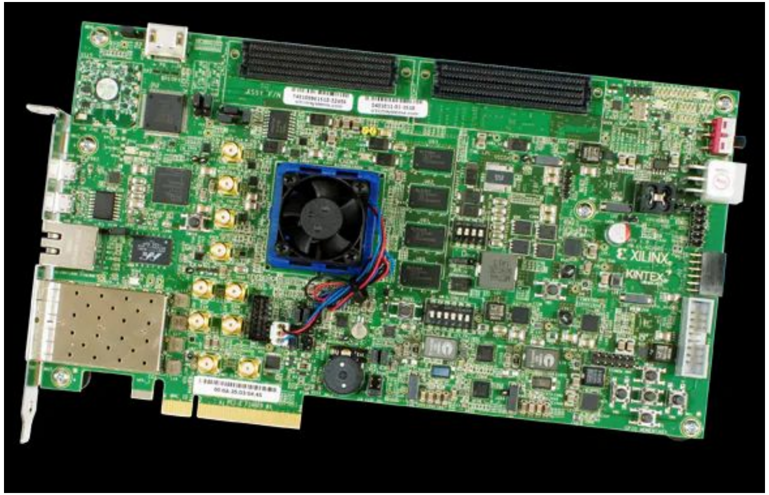


The project includes the design of a dedicateds socket and Data Acquisition (DAQ) system

- Front-end electronics architecture is data driven
  - 64 bit for each pixel hit
  - 16 x 10.24 Gbps serial links
- The detector is hosted on a dedicated carrier board
- A FPGA-based control board:
  - hosted far from detector
  - used for configuration and serial data decoding
  - sends pre-processed data to server for storage and post-processing

The Data Acquisition system





Currently the SPIDR4 read-out system developed by Nikhef is used for testing the ASIC

Development of own “general purpose” DAQ system in progress

- based on Xilinx dev kit
  - custom board foreseen for the future
- uses standard protocols
  - 1G ethernet for configuration data from controller
  - 10G ethernet for detector data to storage
  - FMC for detector communication
- Enough resources for minimal pre-processing and monitoring
  - TBD based on use-case

Summary

We are developing a detector for visible single photons:

- based on a vacuum tube
- a bare Timepix4 CMOS ASIC (anode)
- a Micro Channel Plate stack

This detector will allow the detection of up to 10^9 photons/s with simultaneous measurement of time and position with excellent resolutions

- Fully exploit both timing and position resolutions of a MCP
- High-performance data acquisition (up to ~160 Gbps)

The project foresees the development of a dedicated DAQ system

4DPHOTON Team

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