UNIVERSITÉ DE GENÈVE

EPFL

A monolithic silicon pixel sensor in SiGe BiCMOS for the FASER high granularity pre-shower detector

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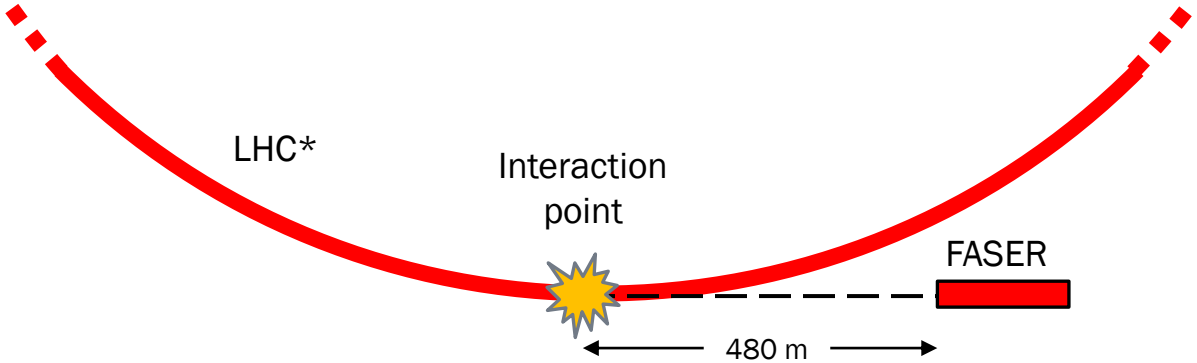
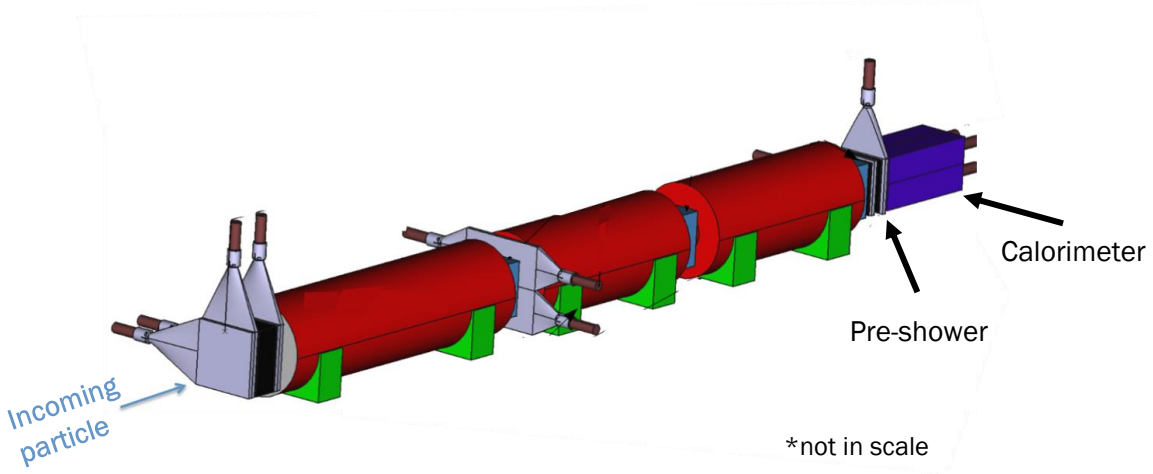
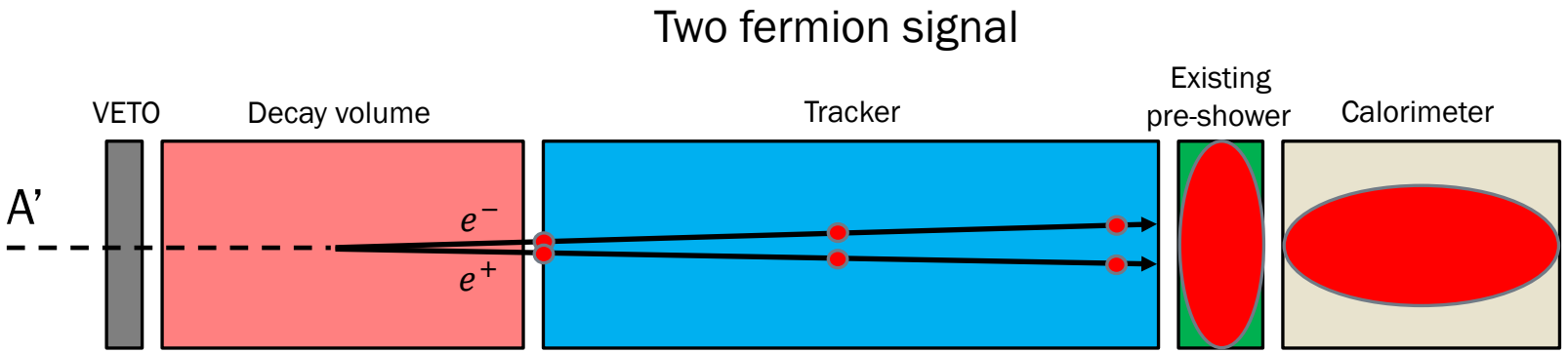
FASER experiment

- Main goal: research on the dark matter through detection of Long Lived Particles (LLP).
- Extension of the physics program of other experiments at LHC.
- Exploiting the huge pion source provided by LHC ($N_{\pi} \approx 10^{17}$).
- Collaboration among 20 institutes.





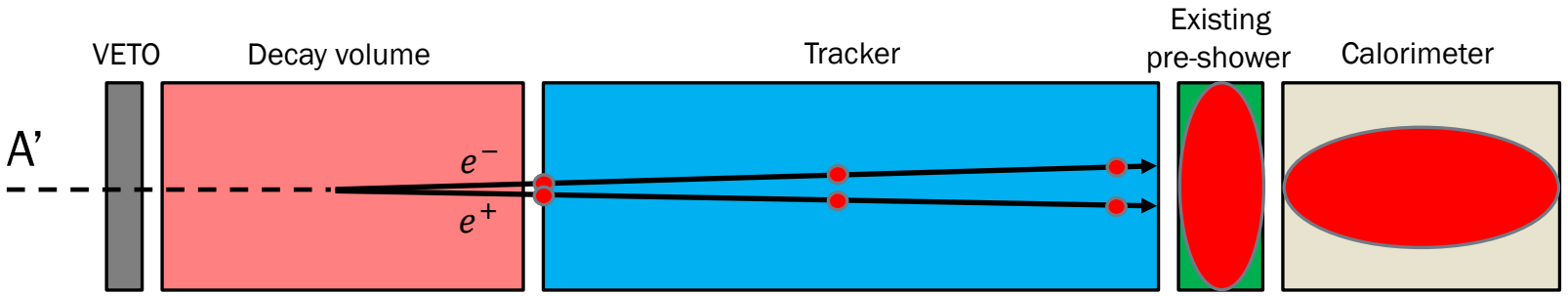
FASER experiment: signals



Produced by the decay of dark photons

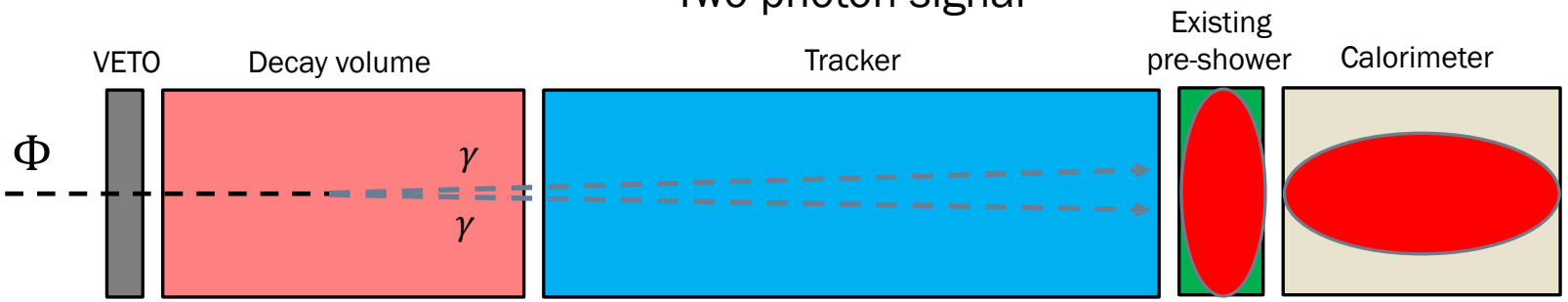
FASER experiment: signals

Two fermion signal



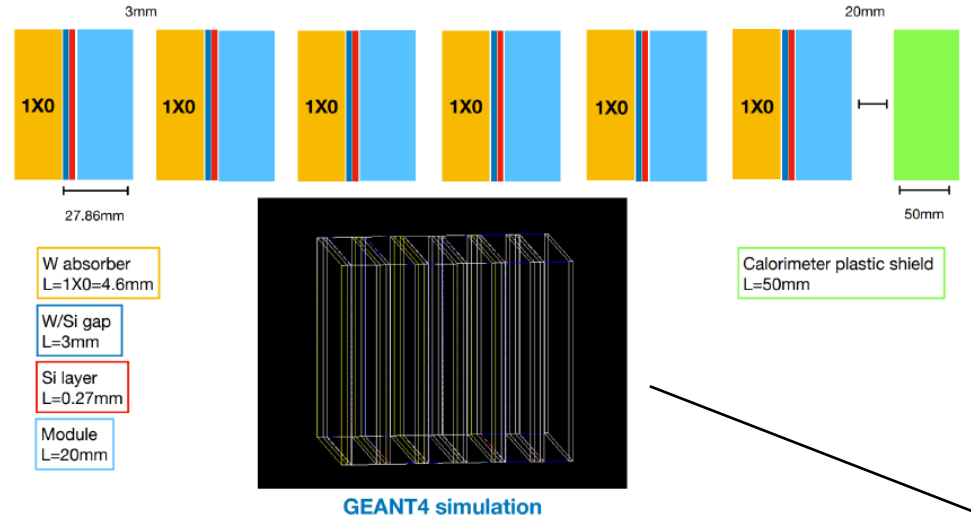
Produced by the decay of dark photons

Two photon signal

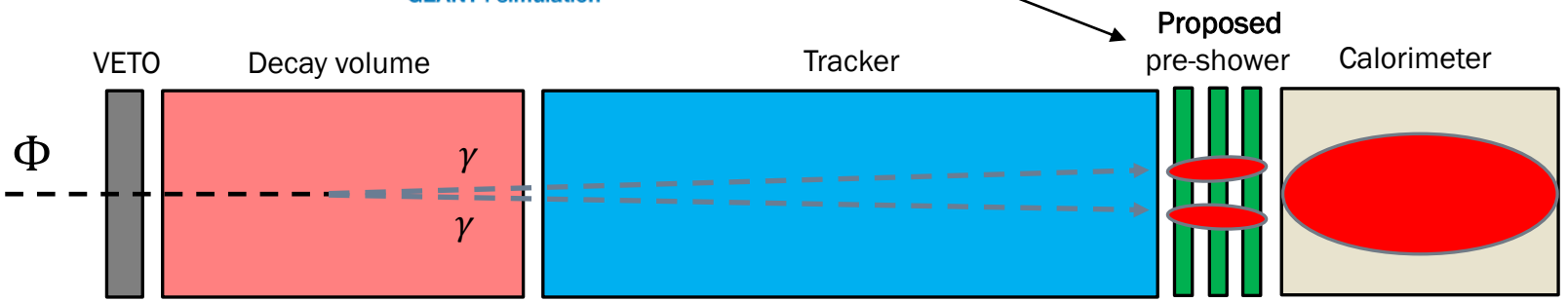


Possible indication of the existence of Axion Like Particles (ALP).
NOT detectable with current FASER system.

FASER experiment: proposal

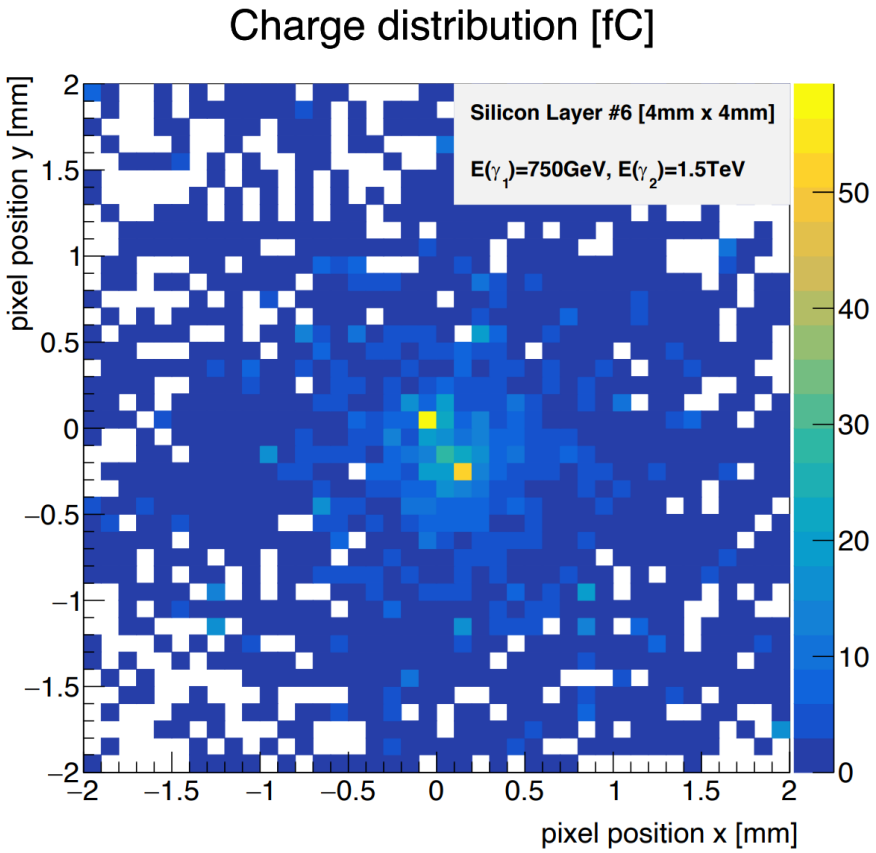


- Replacing the current pre-shower with a 2D timing detector featuring conversion layers (tungsten, lead).
- The timing information will be exploited to extract the direction of the incoming particles.
- Target Time resolution: **100 ps.**



Improved FASER detector

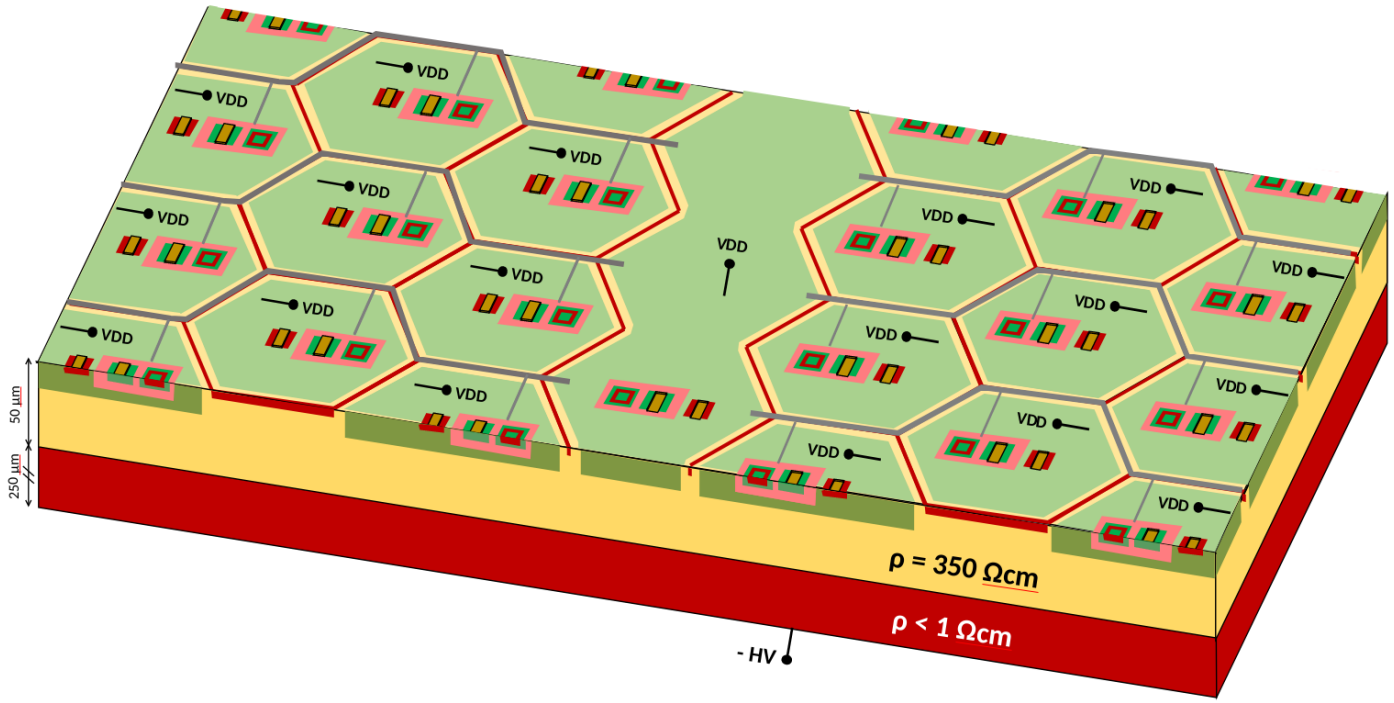
Pixel characteristics and reconstruction



- In order to better reconstruct the electromagnetic showers, we need the ability to reconstruct clusters of hits.
- Charge information for each pixel needs to be recorded and acquired.
- Our choice: 65 μm side hexagonal pixels.
- Hexagonal shape in order to reduce the peak electric field at the edges.

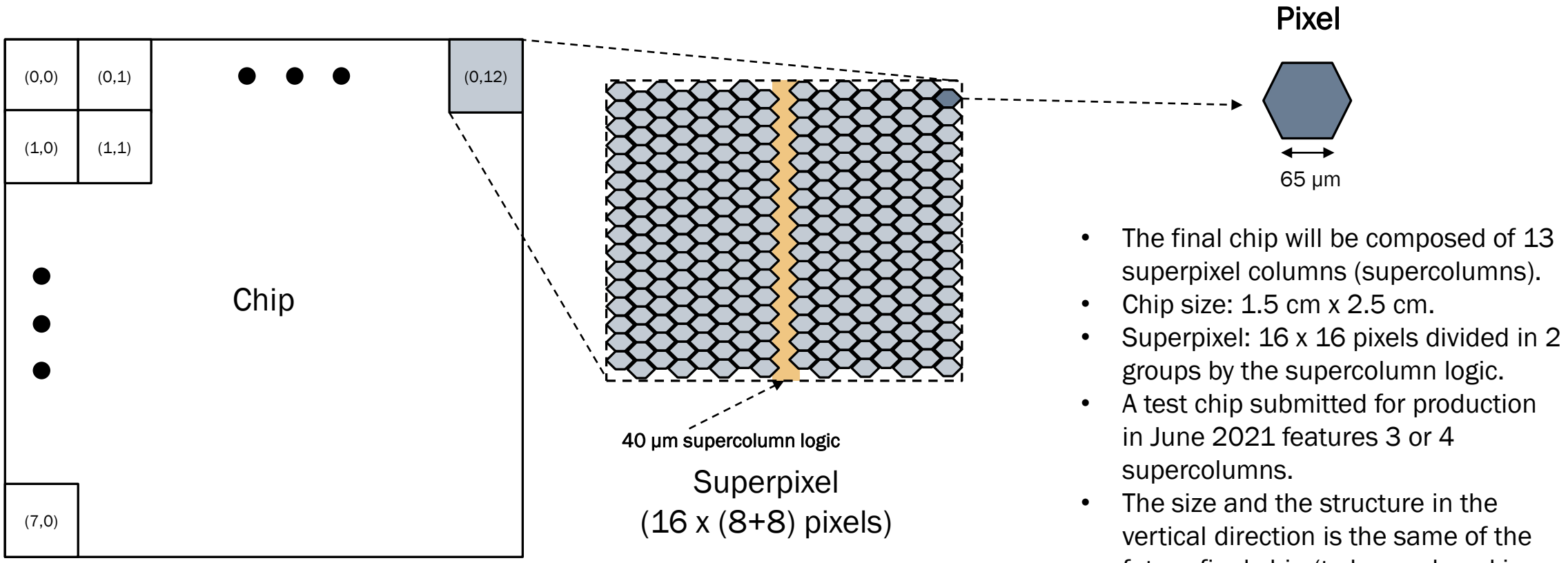
- GEANT4 simulations highlighted that photon signals can produce input charges in a few fC to various tens of fC range.

Sensor cross-section and technology



- Monolithic pixel detector.
- 130 nm SiGe BiCMOS technology provided by IHP Microelectronics.
- Custom high-resistivity 50 µm EPI layer. HV=-120 V, complete depletion.
- Pixels integrated as triple-wells.
- Front-end electronics integrated in pixel.

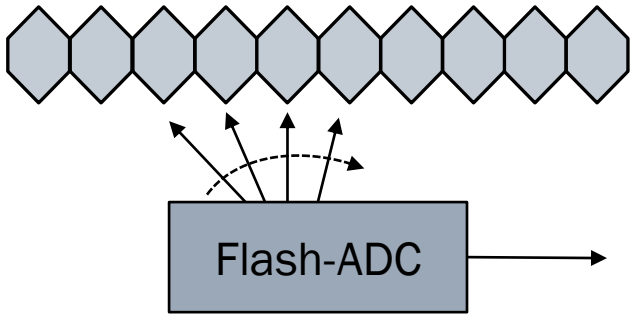
Chip architecture



- The final chip will be composed of 13 superpixel columns (supercolumns).
- Chip size: 1.5 cm x 2.5 cm.
- Superpixel: 16 x 16 pixels divided in 2 groups by the supercolumn logic.
- A test chip submitted for production in June 2021 features 3 or 4 supercolumns.
- The size and the structure in the vertical direction is the same of the future final chip (to be produced in 2022).

Polling and analog memory

- The charge needs to be measured for each pixel.
- The idea is to store the data on a capacitor (via a sample and hold) in each pixel and convert it on the fly with a flash ADC. 256-to-1 MUX.
- The capacitor is charged with a constant current during the TOT.
- The same ADC will poll all the pixels in a superpixel and convert them as needed.



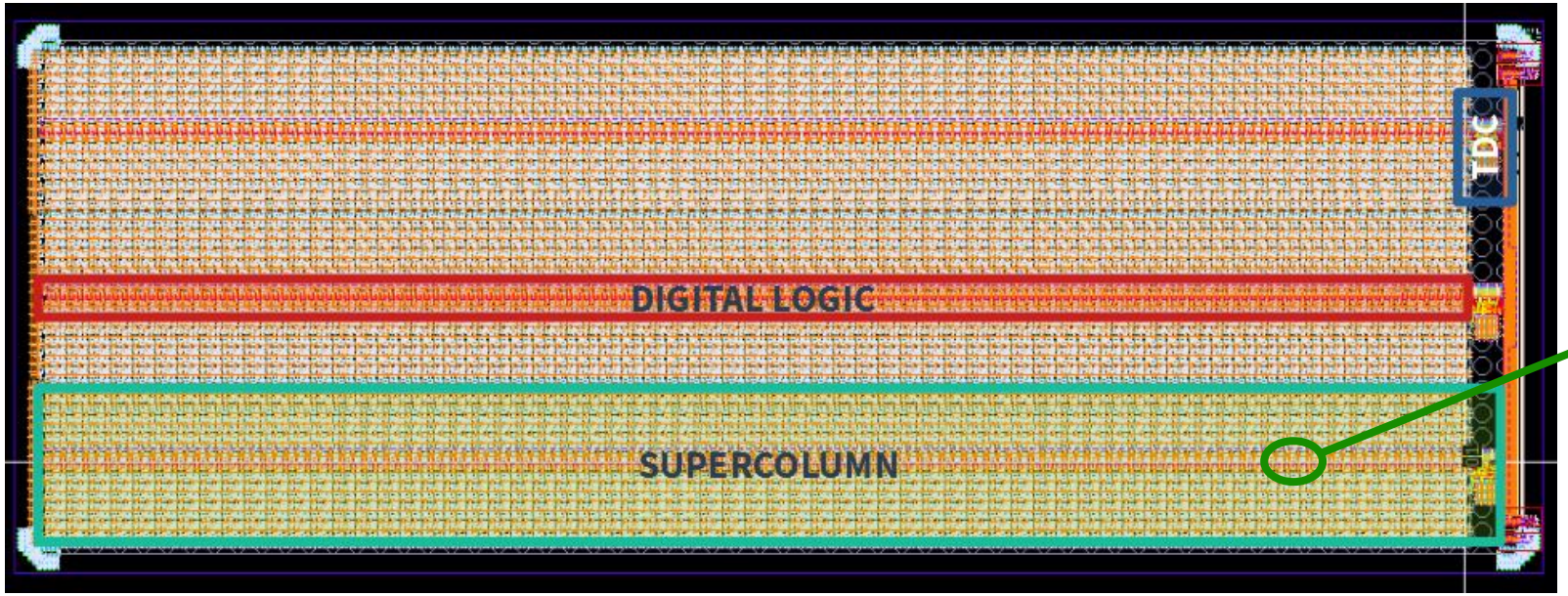
Pre-production chip specs

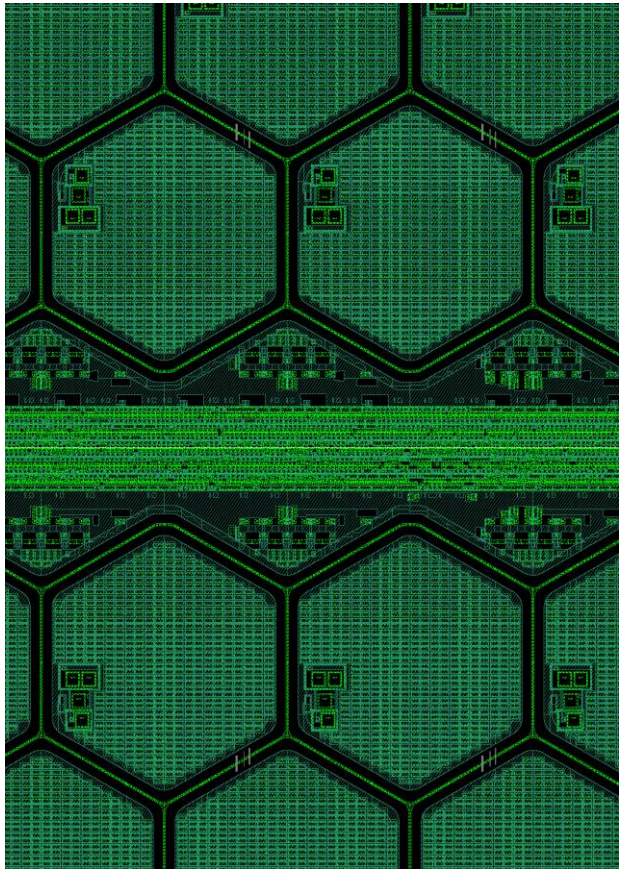
Technology	IHP 130 nm SiGe BiCMOS
Pixel size	65 µm side – hexagonal
Matrix size	64 by 128 (7.2 by 15.3 mm)
Positive supply	1.2 V
Current consumption (Analog)	24 mA
Current consumption (Digital)	26 mA
Power consumpion	7 µW/pixel
Input charge dynamic range	1 fC to 64 fC
Readout time	~26 µs (typical)

Chip floorplan and supercolumn logic

- The chip is divided in “supercolumns” (128 by 16 pixels) with a ~40 μm slice of digital logic in between.
- The digital logic includes the MUX, the flash ADC, a small programming logic to mask the pixels and the entire readout logic for all the pixels in the supercolumn.
- Moreover, a data pruning system is implemented to increase the speed of the readout.
- The physical design of this block presented some challenges as its aspect ratio is very unusual (1.5 cm by 40 μm).

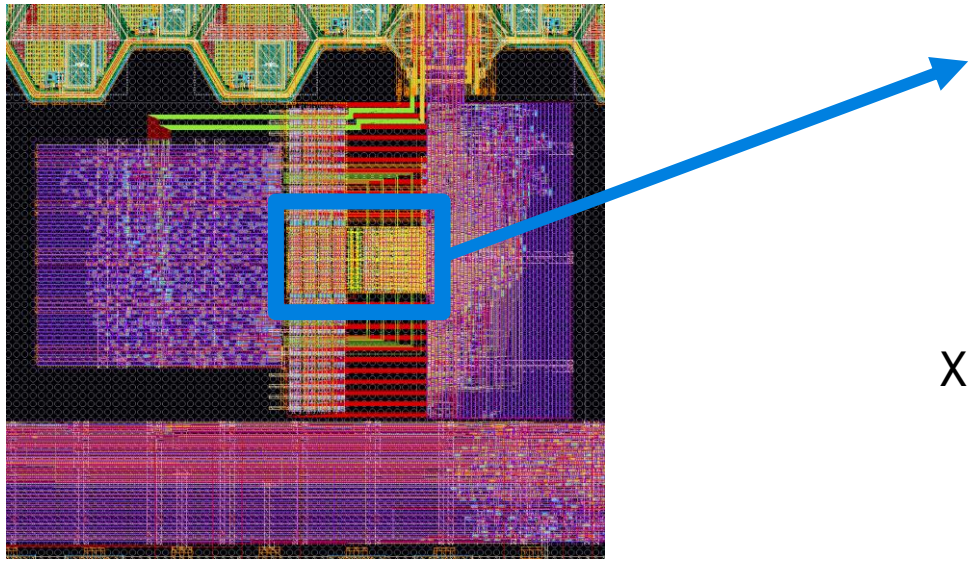
Chip floorplan and pixel layout

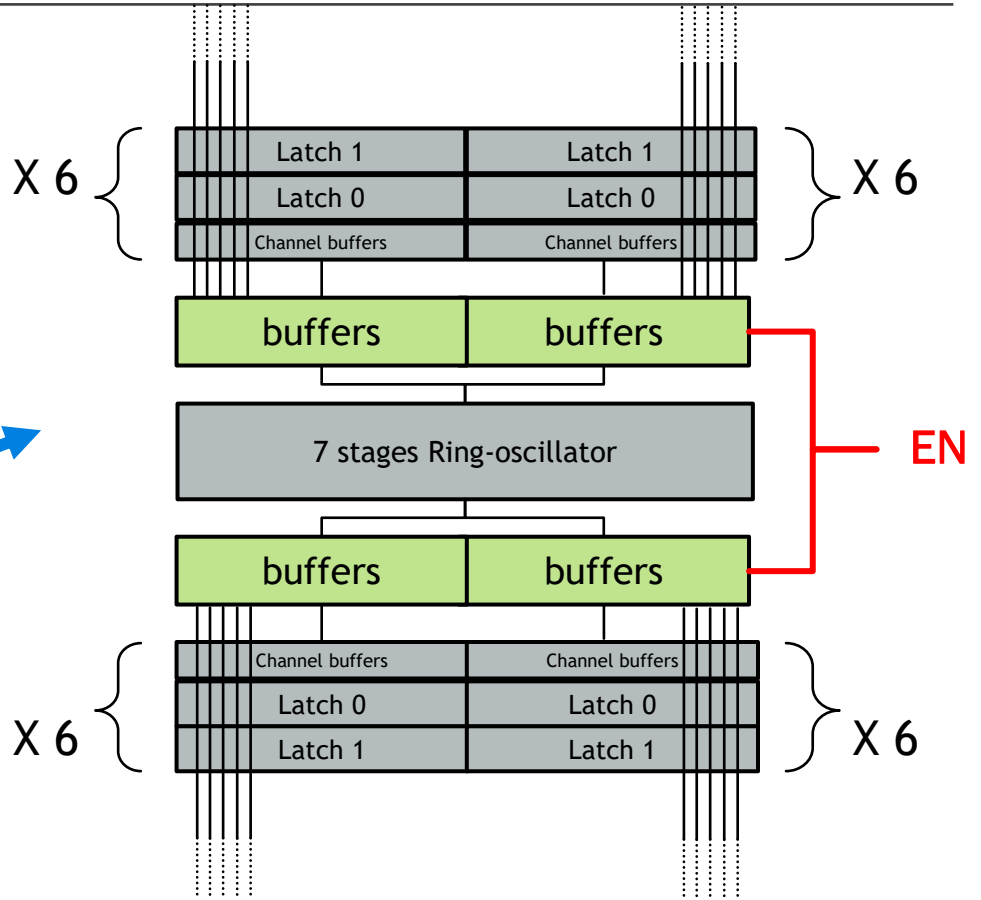




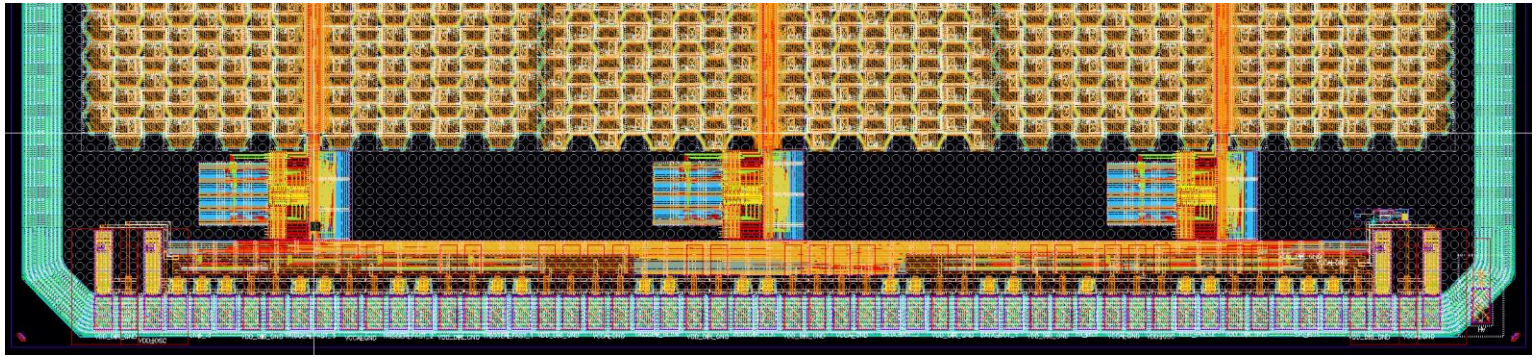
TDC

- 7 stages ring oscillator-based TDC.
- 24 channels with 2 set of D-Latches each.
- Less than 100 ps binning.
- The TDC features a clock gating system: **~ 500 µW if no event occurs instead of ~ 26 mW.**
- Counters are used for the coarse component of the measurement.





End of column and periphery



- The TDC outputs are fed into an end-of-column block to be read out.
- The end-of-column block connects the supercolumn logic with the periphery.
- SPI slow control to mask individual pixels and control biases
- Double LVDS 200 Mb/s output link.
- Bandgap, global DACs to provide biases (the chip has no analog input).
- **The periphery logic is agnostic to the number of supercolumns: the design can easily be resized with minimal changes.**

Conclusions and next steps

- 3 different test chip have been submitted and will be available for testing in the next few months.
- We prioritized making the chip easily testable (standard I/O, common pinout).
- We also chose a easily scalable architecture, a fundamental feature to reduce the design time.

- The scaled up version with 13 supercolumns should be submitted in March 2022.

Appendix

MUX solution characteristics

Pros

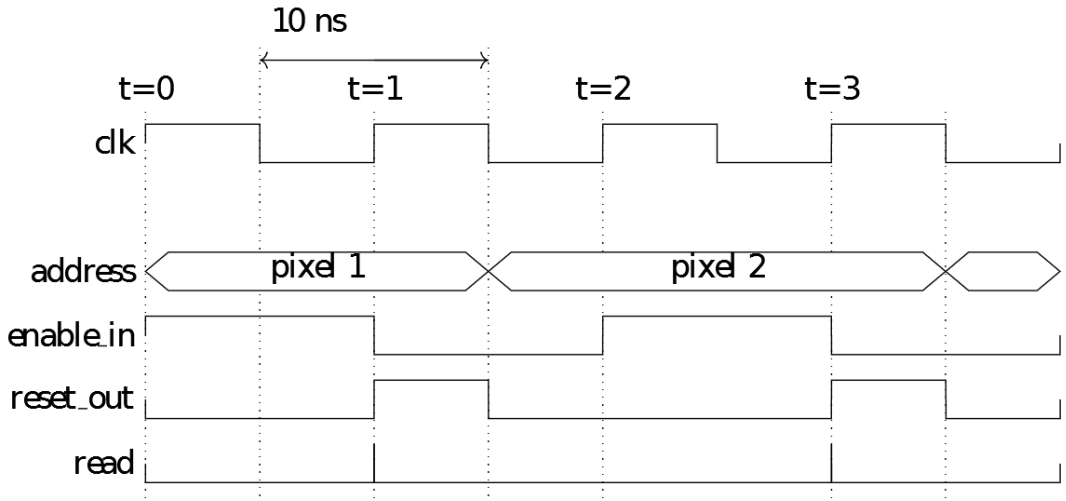
- This architecture is much smaller than using a TDC channel for each pixel.
- It cuts the amount of memory by a factor 256 (pixels in a superpixel).
- A 256-to-1 multiplexer is less than 5 μm wide.
- The flash ADC is a very simple design (as long as we do not need great accuracy, 4 bits is fine for us).

Cons

- The time to complete a readout is critical as the capacitors cannot store the charge indefinitely.
- Unfortunately a 256-to-1 analog multiplexer poses challenges.

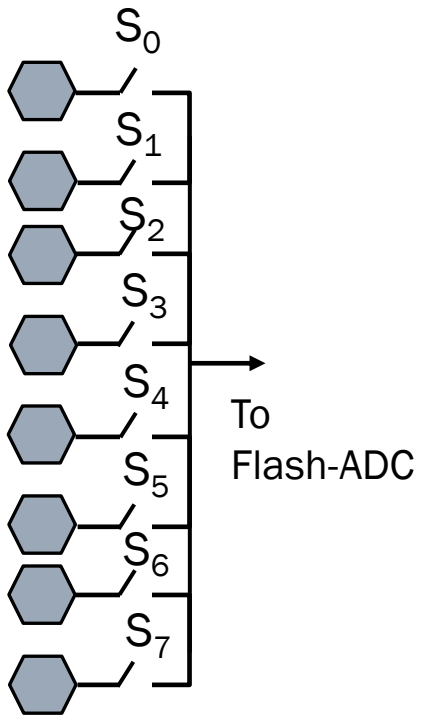
MUX: challenges and solutions – 1

- When switching between codes we have to make sure pixels are not short-circuited.
- The analog MUX has a certain capacitance associated to its active path. It needs to be discharged before reading the next pixel.
- When **reset_out** is 1, the input of the ADC is charged to VDD.
- **enable_in** added to avoid activating unwanted addresses during readout.
- Careful timing needs to be introduced to manage the switching, making it at least 2 clock cycles per switch.

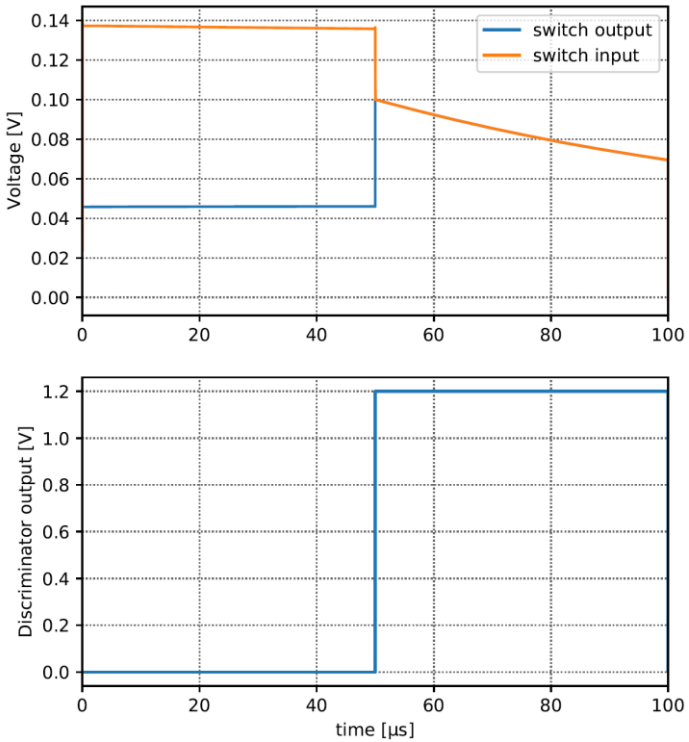


MUX: challenges and solutions – 2

- **Naive approach** for the MUX design: a switch per pixel, all connected to the same line.
- **Problem**: due to the large capacitance connected to each switch, half of the charge will be lost during switching.

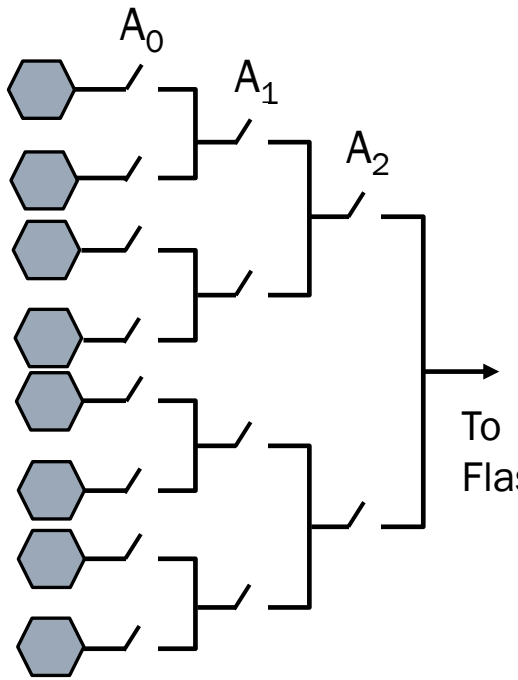


2^3=8 pixels example

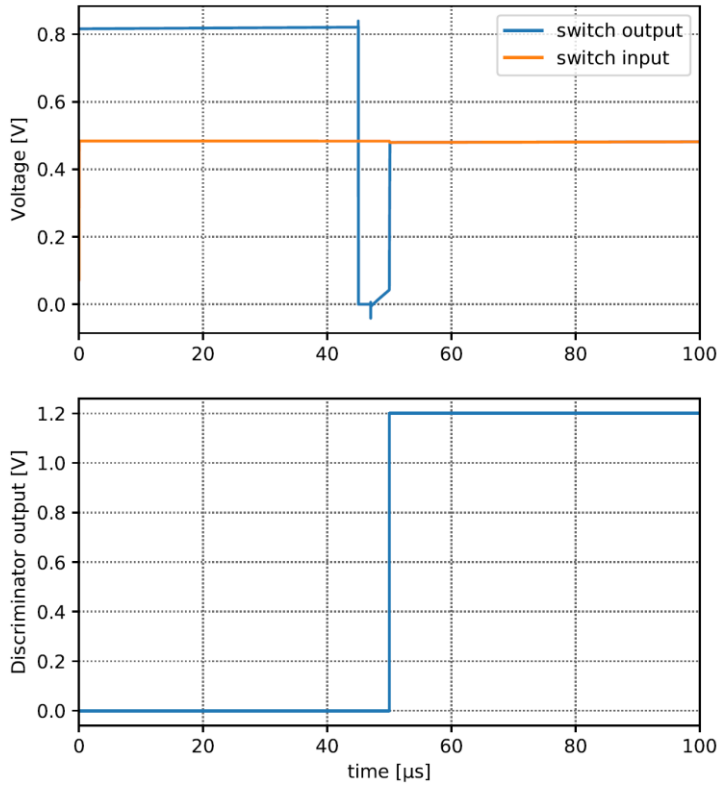


MUX: challenges and solutions – 3

- **Proposed design**: multi-stage approach.
- 8 stage of 2-to-1 MUXs in series.
- **Lower capacitance** seen at each node.

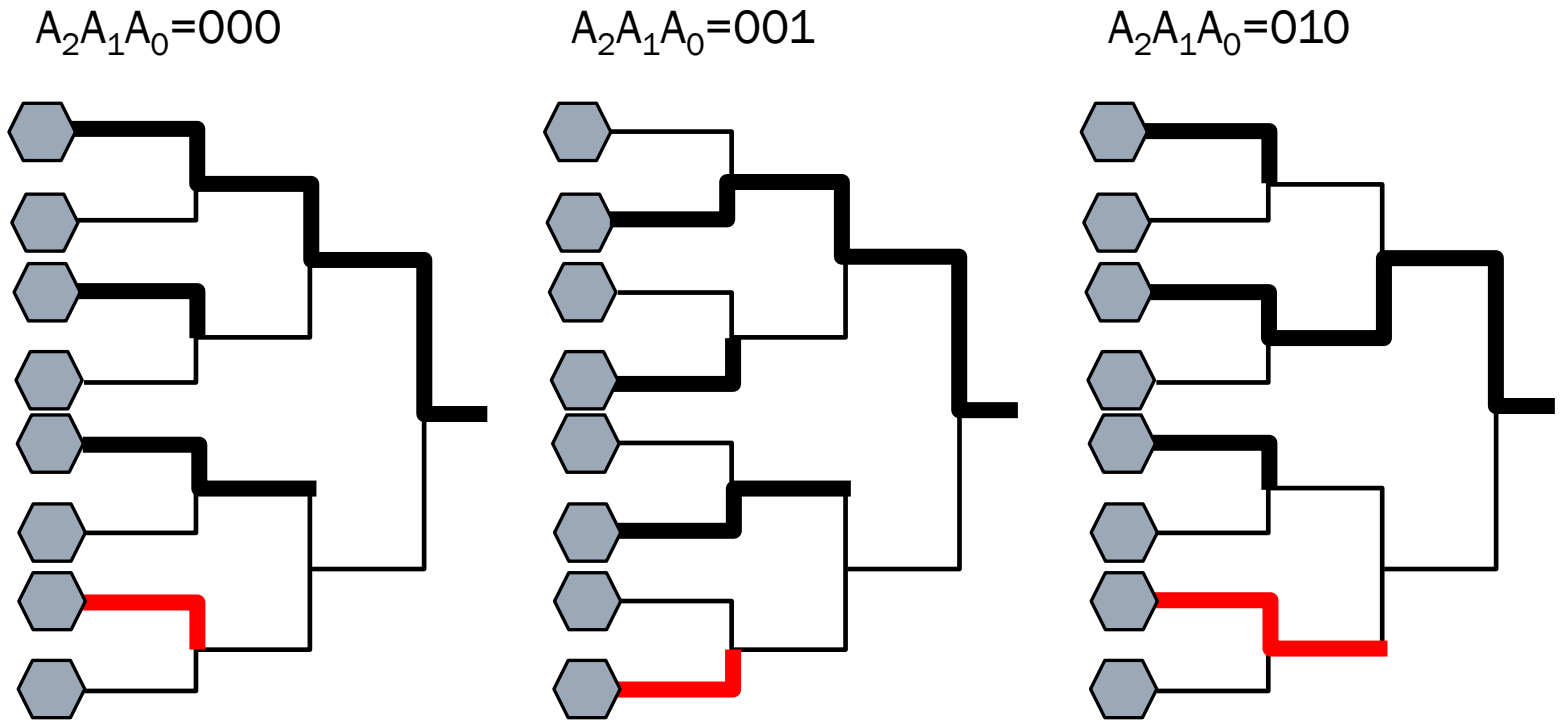


2^3=8 pixels example



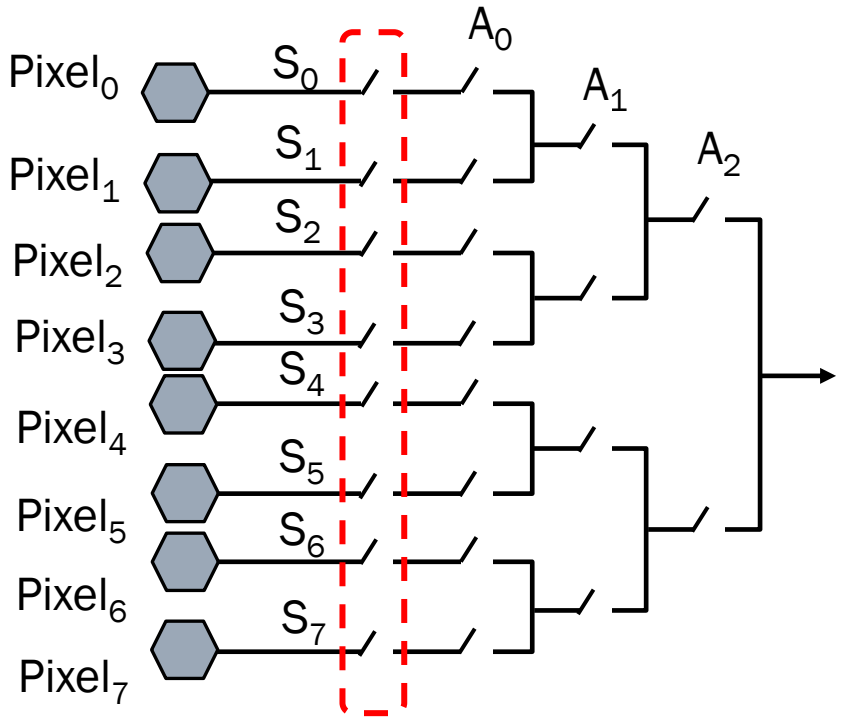
MUX: challenges and solutions – 4

- **Problem of the proposed design:** the polling leads to the sharing of the charges of the pixels with ‘higher’ addresses.
- This is due to the switching of the LSB of the address (A_0 in the example).
- **Solution**: additional switches connected to the MUX inputs.



MUX: challenges and solutions – 5

- **Solution**: additional switches connected to the MUX inputs.
- For this example:
  - $Pixel_{2\text{-}3}$: $S_{2\text{-}3}$ AND with A_1
  - $Pixel_{4\text{-}5}$: $S_{4\text{-}5}$ AND with A_2
  - $Pixel_{6\text{-}7}$: $S_{6\text{-}7}$ AND with A_1,A_2

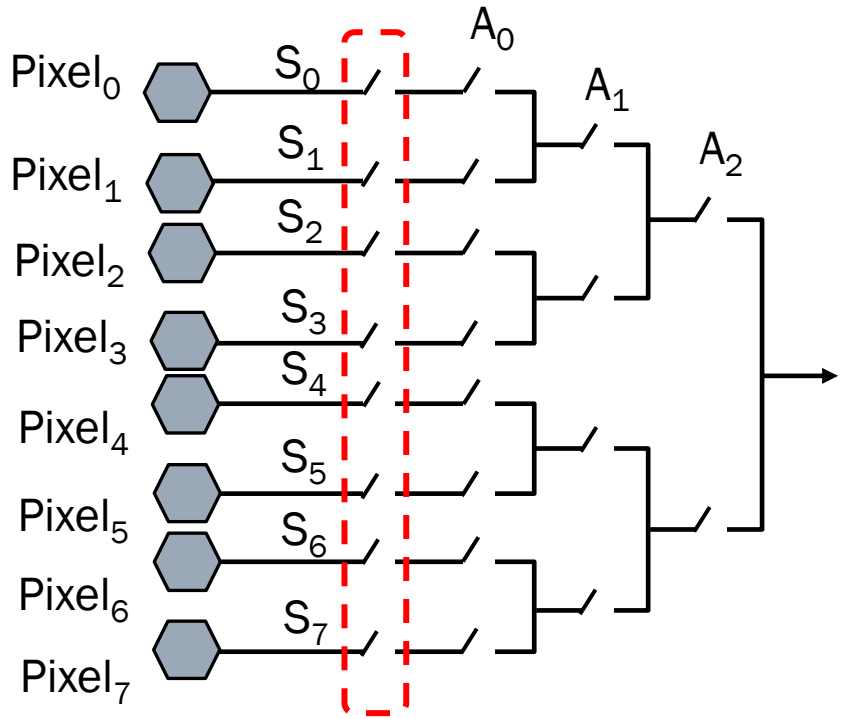


MUX: challenges and solutions – 6

- In a N-bit case, there will be 2^{N-1} couples of pixels.
- The couples can be coded in binary words C of N-1 bit.
- It is possible to demonstrate that the i-th couple needs a number of AND inputs equal to the number of 1s in the corresponding word C.
- In the N=8 case the number of additional AND inputs needed will be:

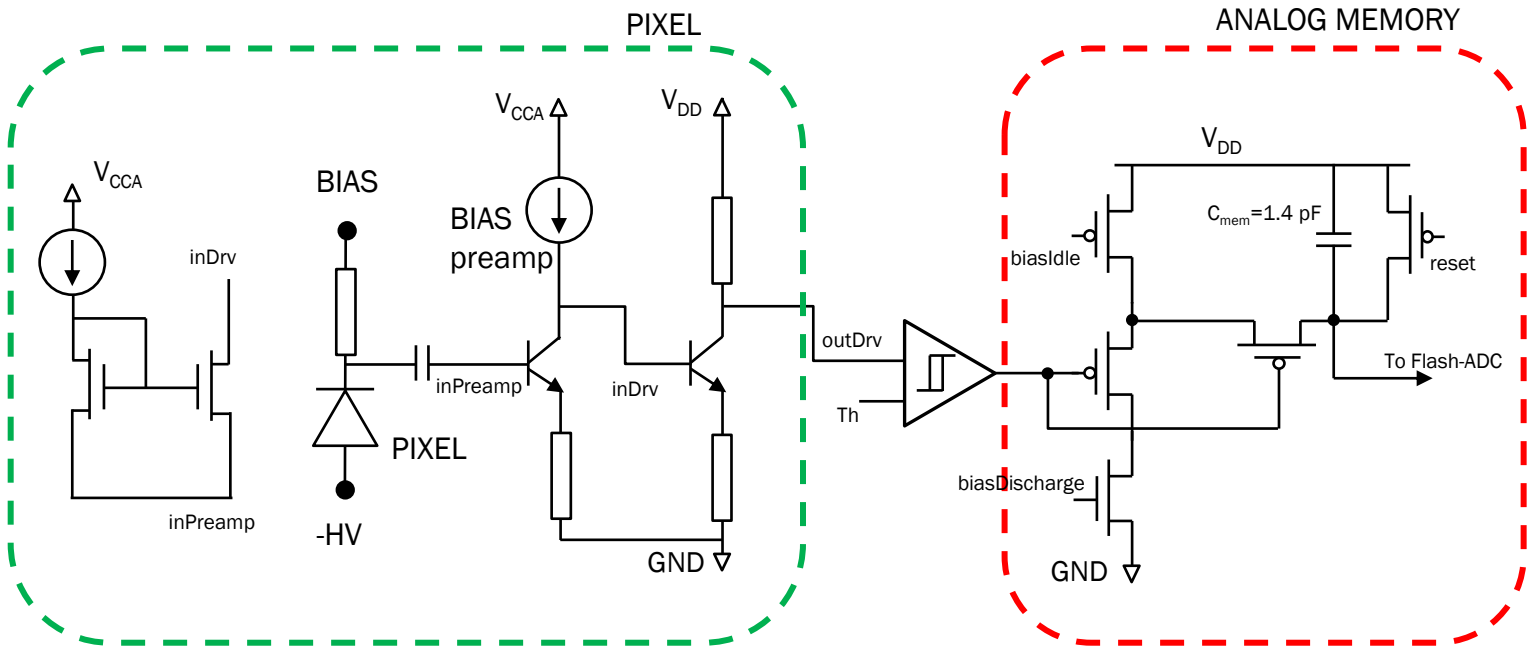
$$\binom{7}{1} + \binom{7}{2}2 + \binom{7}{3}3 + \binom{7}{4}4 + \binom{7}{5}5 + \binom{7}{6}6 + \binom{7}{7}7 \approx 400$$

- In the token ring solution, 256 **D-flip-flops** are required.



Front-end architecture

- BJT-based preamp with MOS feedback
- Low-power discriminator (that can be outside of the pixel area)
- Analog memory
- Discriminator output activates the charging of the capacitor C_{mem}.
- reset and biasIdle are used to discharge C_{mem} when no hit occurs and to deal with leakage respecively.



Test chip variants

Three chips were submitted:

- A **4-supercolumn reference design**.
- A **3-supercolumn variant** with BJT-based discriminators featuring lower pixel-to-pixel mismatch.
- A **3-supercolumn variant** with counters instead of mux + ADC (safe).
  - This version has triple the dead area compared to the other two. The supercolumn logic is 3 times thicker due to the addition of LFSR counters replacing the analog memory system.
- The periphery and readout logic is unchanged among them.

Pixel Calibration

- The limiting factor for the dynamic range at the low end is the pixel-to-pixel threshold mismatch.
- The issue could be solved with a local tuning DAC, but there was no space for it and for its configuration register.
- 8 thresholds are distributed to different areas to reduce this effect through 8 bit DACs.
- The version with BJT-based discriminators are designed to solve this issue: BJTs are '**vertical**' with **sharper** and **more precise doping profiles.**