

Development of CMOS Pixel Sensor prototypes for the high-rate CEPC vertex detector

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The proposed Circular Electron Positron Collider (CEPC) imposes new challenges for the vertex detector in terms of material budget, spatial resolution, readout speed, and power consumption. CMOS Pixel Sensor (CPS), as one of the promising candidate technologies, has been studied within the CEPC vertex detector R&D activities since 2015. According to the latest collider design and study on the beam-induced background, the highest hit rate for the vertex detector is expected to be $\sim 107/\text{cm}^2/\text{s}$. The TaichuPix chip is a CMOS Pixel Sensor being developed to meet the highest hit rate requirement of CEPC vertex detector. Two small scale prototypes capable of achieving a hit rate up to $36 \text{ MHz}/\text{cm}^2$, were developed in a 180 nm CMOS process. This talk presents the dedicated improvements on the design of in-pixel readout to achieve a pixel pitch of $25 \mu\text{m}$ and a fast readout capability of 40 MHz. Two new fast in-pixel digital readout designs, benefiting from the FE-I3 and ALPIDE approaches, have been implemented. The readout of the pixel array is based on a new proposed “column-drain” architecture. Pixels are arranged in double columns, with priority encoder within column and timestamp recorded at the end of double column (EOC). All the double columns are read out in parallel, in order to minimize the dead time. When a hit is detected in one of the pixels, the end of column circuitry stores the current time stamp with a resolution of 25 ns. The data whose timestamp matches with the trigger (with a time window of 175 ns) are buffered for output in case of trigger mode. The two TaichuPix prototypes were characterized with electrical and radioactive sources in laboratory. The test results on the chip functionality and the noise and threshold performance before and after ionizing radiation are reported.

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