环形正负电子对撞机
Circular Electron Positron Collider

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Institute of High Energy Physics
Chinese Academy of Sciences

Development of CMOS Pixel Sensor prototype for the high-rate CEPC vertex detector

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On behalf of the CEPC MOST2 Vertex detector design team

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POSITION SENSITIVE DETECTORS

Hosted by
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Outline

- Project introduction and TaichuPix chip overview
- Small scale prototypes design and test results
- Full scale prototype design
- Summary

CEPC Vertex detector requirements (CDR)

Circular Electron Positron Collider (CEPC) proposed as a Higgs factory.

- **Efficient tagging of heavy quarks (b/c) and τ leptons**

  ➔ Impact parameter resolution,

$$\sigma_{r\emptyset} = 5 \oplus \frac{10}{(p \cdot sin^{3/2}\theta)} \ (\mu m)$$

Physics driven requirements		Running constraints	Sensor specifications	
$\sigma_{s.p.}$	2.8 μm		Small pixel	***~16 μm***
Material budget	0.15% X_0/layer		Thinning to	***50 μm***
		Air cooling	low power	***50 mW/cm²***
r of Inner most layer	16 mm	beam-related background	fast readout	***~1 μs***
		radiation damage	radiation tolerance	***≤3.4 Mrad/ year***
				≤6.2×10¹²n_{eq}/ (cm² year)

Baseline design parameters for CEPC vertex detector

	R (mm)	$\lvert z \rvert$ (mm)	$\lvert \cos\theta \rvert$	σ (μm)
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4

Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector, http://cepc.ihep.ac.cn/

MOST2 project requirements on pixel chip

Silicon Vertex Detector Prototype – MOST (2018–2023)

Sensor technology CMOS TowerJazz

- Design sensor with large area and high resolution
- Integration of front-end electronic on sensor chip

Benefit from MOST 1 research program

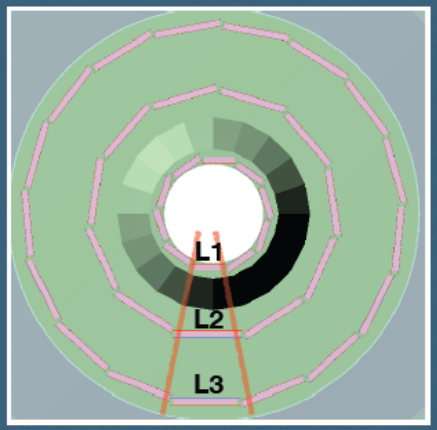
Double sided ladder

Layer 1 (11 mm x 62.5 mm)
Chip size: 11 mm X 20.8 mm

3 X 2 layer = 6 chips

Ref: Introduction to the Pixel MOST2 Project, Joao Costa, 2018.6

3-layer sector



Baseline MOST2 goal:
3-layer prototype

Default layout requires different size ladders

Keep it simple for baseline design

3-layers
same size
same chip

Goals:
1 MRad TID
3-5μm SP resolution

Integrate electronics readout

Design and produce light and rigid support structures

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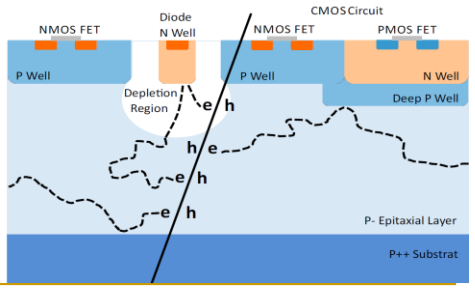
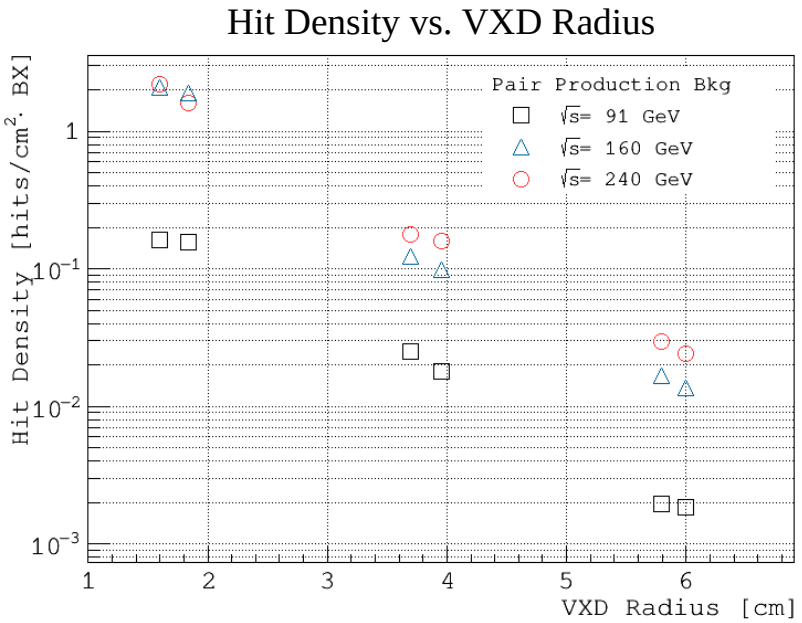
- **Motivation for TaichuPix chip design**
  - Large-scale & full functionality pixel chip
  - Fit to be assembled on ladders with backend Elec. & DAQ



CMOS pixel sensor

Main specs of the full scale chip for high rate vertex detector

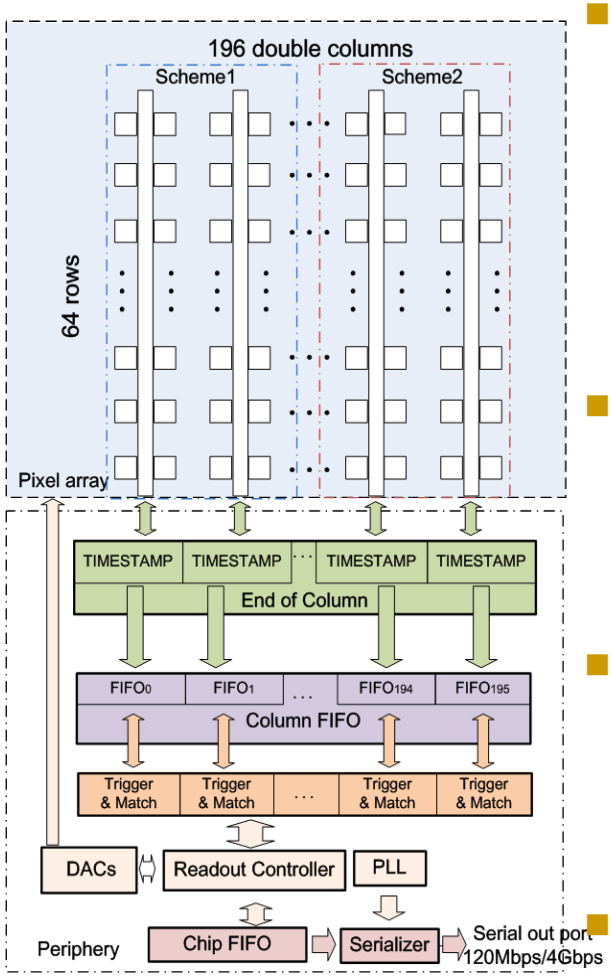
- **Bunch spacing**
  - Higgs: 680 ns; W: 210 ns; Z: **25 ns**
  - Max. bunch rate: 40 M/s
- **Hit density**
  - 2.5 hits/bunch/cm^2 for Higgs/W; 0.2 hits/bunch/cm^2 for Z
- **Cluster size: ~3 pixels/hit**
  - Epi-layer thickness：~18 μm
  - Pixel size：25 μm × 25 μm



Ref: CEPC Conceptual Design Report, Volume II

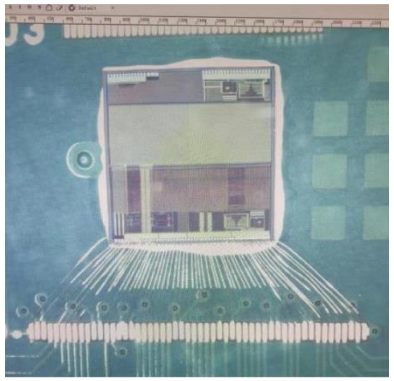
For Vertex	Specs	For High rate Vertex	Specs.	For Ladder Prototype	Specs.
Pixel pitch	≤ 25 μm	Hit rate	120 MHz/chip	Pixel array	512 row × 1024 col
TID	>1 Mrad	Date rate	**3.84 Gbps** --triggerless **~110 Mbps** --trigger	Power Density	< 200 mW/cm^2 (air cooling)
		Dead time	< 500 ns --for 98% efficiency	Chip size	~1.4 cm×2.56 cm

TaichuPix architecture

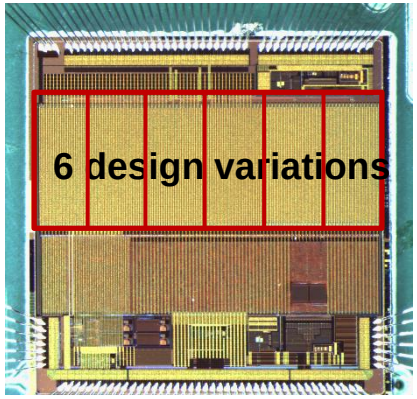


- **Similar to the ATLAS ITK readout architecture: "column-drain" readout**
  - Priority based data driven readout, zero-suppression intrinsically
  - Modification: time stamp is added at EOC whenever a new fast-or busy signal is received
  - Dead time: 2 clk for each pixel (50 ns @40 MHz clk)
- **Two parallel pixel digital schemes**
  - ALPIDE-like: Readout speed was enhanced for 40 MHz BX
  - FE-I3-like: Fully customized layout of digital cells and address decoder for smaller area
- **2-level FIFO architecture**
  - L1 FIFO: In column level, to de-randomize the injecting charge
  - L2 FIFO: Chip level, to match the in/out data rate between the core and interface
- **Trigger readout**
  - Make the data rate in a reasonable range
  - Data coincidence by time stamp, only matched event will be readout

TaichuPix small prototypes overview



TaichuPix-1
Chip size：5 mm × 5 mm
Pixel size：25 μm × 25 μm

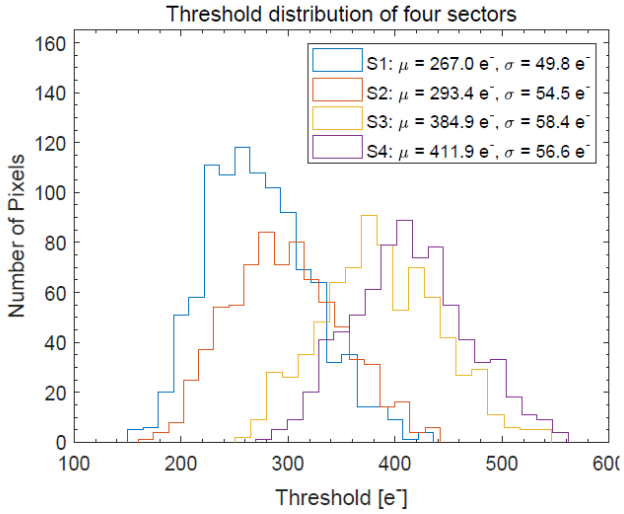


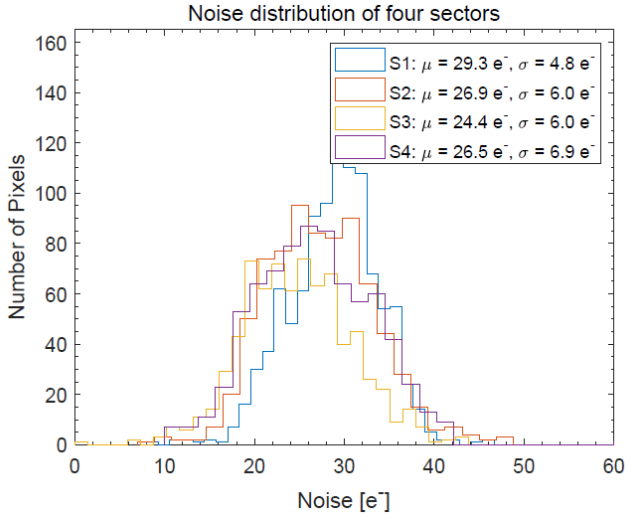
TaichuPix-2
Chip size：5 mm × 5 mm
Pixel size：25 μm × 25 μm

- **Two MPW chips were fabricated and verified**
  - TaichuPix-1: 2019.06~2019.11
  - TaichuPix-2: 2020.02~2020.06
- **Chip size 5 mm×5 mm with standalone features**
  - In-pixel circuitry:
    - Continuously active front-end
    - Two digital schemes, with masking & testing config. logics
  - A full functional pixel array (64×192 pixels)
  - Periphery logics
    - Fully integrated logics for the data-driven readout
    - Fully digital control of the chip configuration
  - Auxiliary blocks for standalone operation
    - High speed data interface up to 4 Gbps
    - On-chip bias generation
    - Power management with LDOs
    - IO placement in the final ladder manner
      - Multiple chip interconnection features included

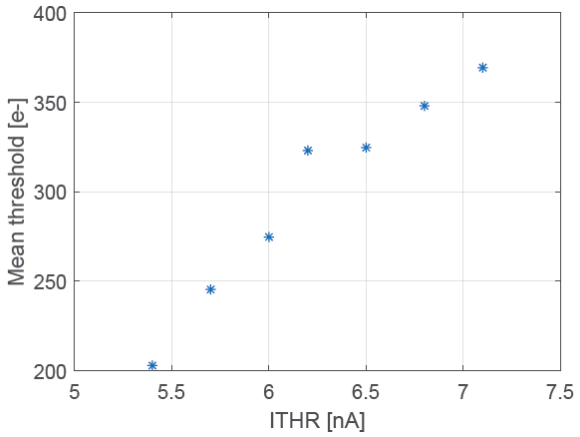
Performance of threshold and noise of TaichuPix2

- Pixel array includes 4 sectors with different transistor parameters/layout for analog front-end, S1 chosen for the full-scale design.
- Threshold can be tuned by changing ‘ITHR’ (a global current bias)





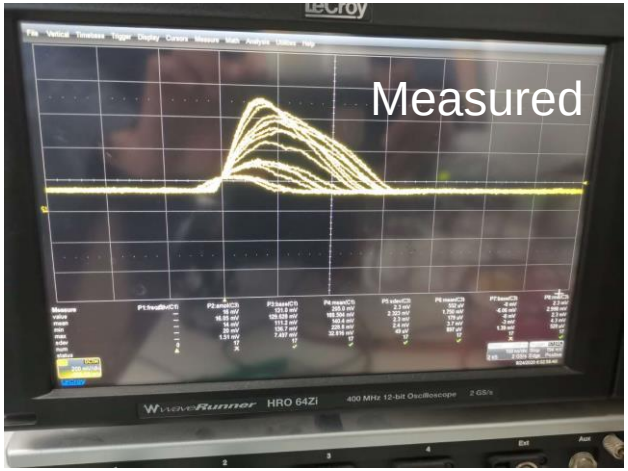
Mean threshold vs. Threshold current ITHR

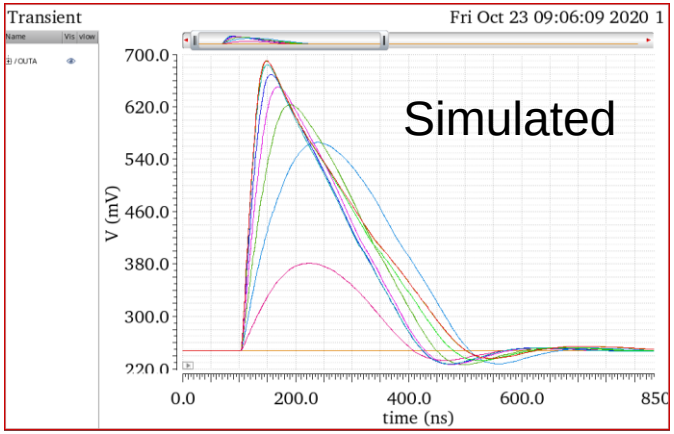


Chip4	Threshold Mean (e^-)	Threshold rms (e^-)	Temporal noise (e^-)	Total equivalent noise (e^-)
S1	267.0	49.8	29.3	57.8
S2	293.4	54.5	26.9	60.8
S3	384.9	58.4	24.4	63.3
S4	411.9	56.6	26.5	62.5

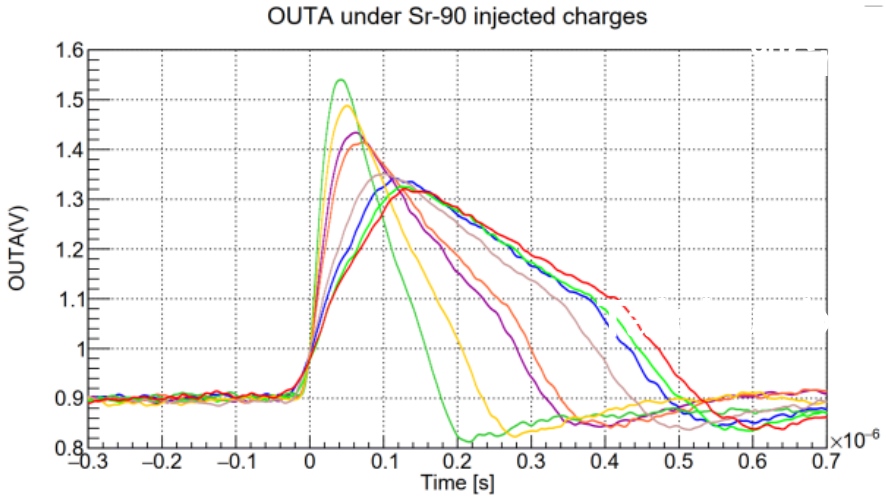
TaichuPix response to radioactive source

- **Functionality of TaichuPix1&2 proved**

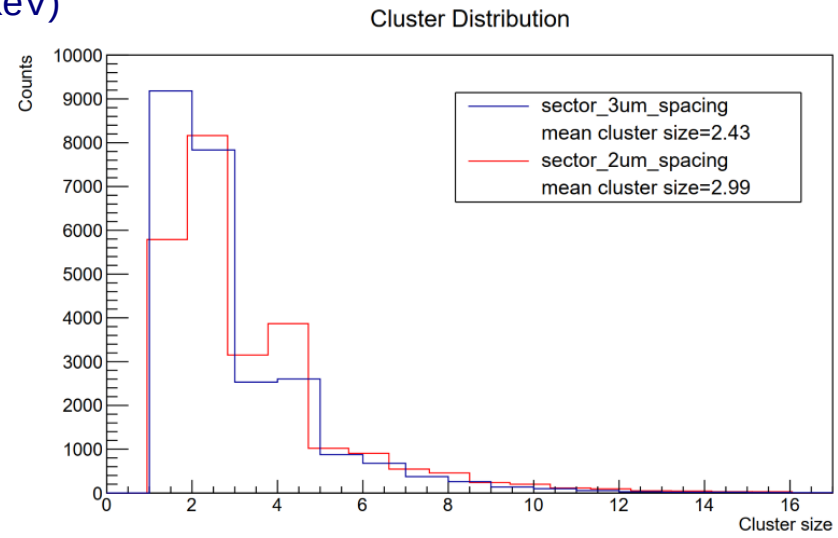




TaichuPix2 response to **X-ray** tube (cutting energy @ 6keV)

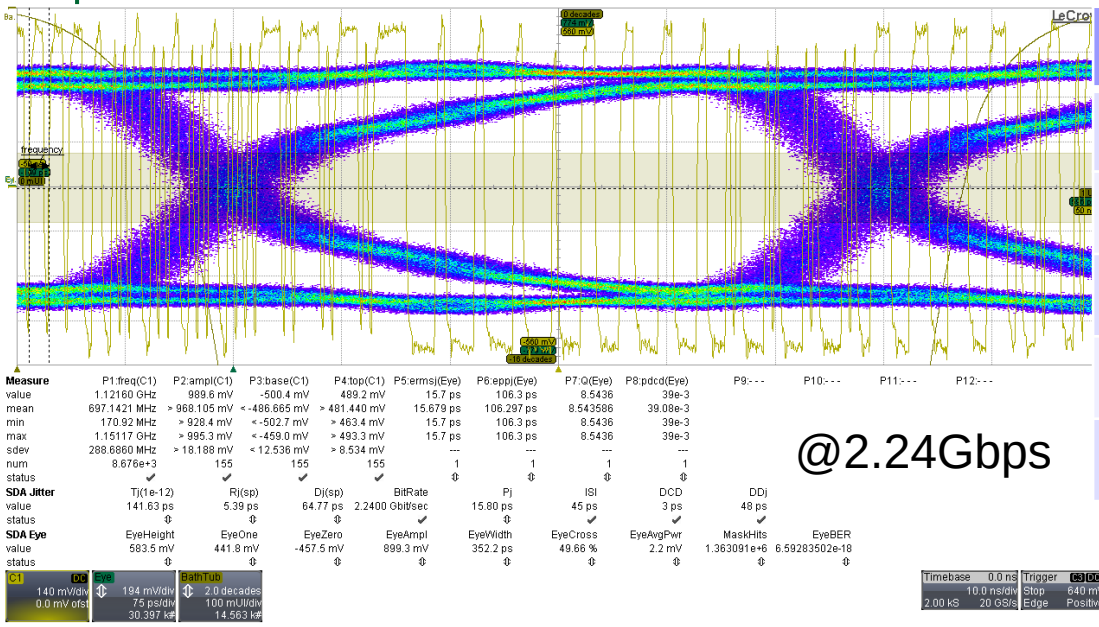


TaichuPix1 response to ^{90}**Sr** exposure

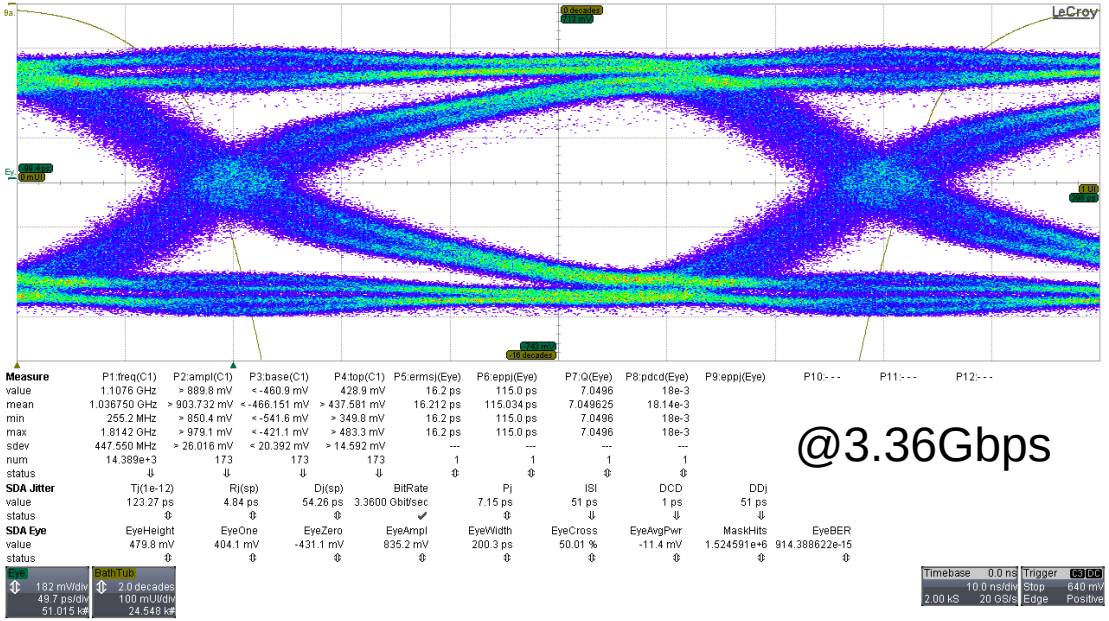


TaichuPix1 cluster size to ^{90}**Sr** exposure

Test of the data interface



@2.24Gbps



@3.36Gbps

Bit rate	2.24Gbps	3.36Gbps	4.48Gbps
Clk freq	1.12GHz	1.68GHz	2.24GHz
BER	6.59e-18	9.14e-13	3.23e-5
Tj@e-12	141.63ps	123.27ps	147.14ps
Rj	5.39ps	4.84ps	5.35ps
Dj	64.77ps	54.26ps	70.90ps

- **Data readout in DDR mode**
- **Data interface was tested by the on-chip PRBS source, a high speed oscilloscope (@16Gsps), and code stream verified in FPGA**
- **BER qualified till 3.36 Gbps, failed at 4.48 Gbps**
- **Concerning the highest data rate for triggerless at 4 Gbps, at least 2 SER interface ports needed**
- **Thus bit rate @2.24 Gbps is safe and power optimized**

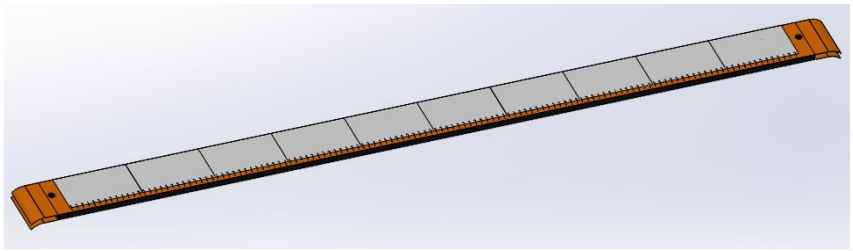
Overview of the full scale prototype

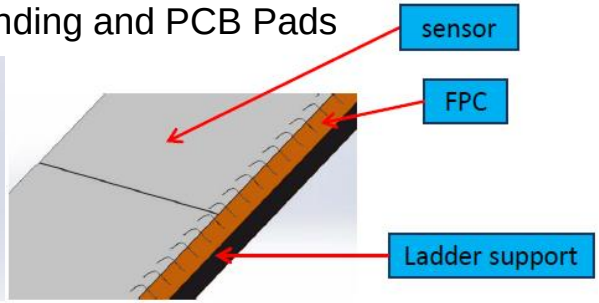
1. Pixel array 1024*512
2. Periphery
3. DAC & Bias generation
4. Data interface
5. LDO (test blocks)
6. Chip inter-connection features
7. Scribe-able top power connection features

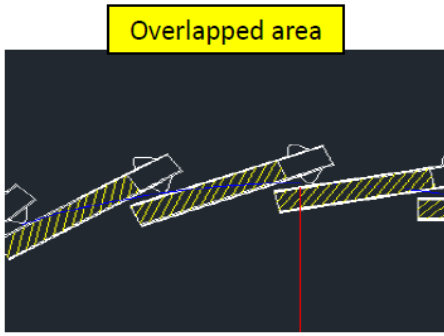
- Process: 180 nm CMOS Imaging Sensor process (7 metal layers)
- Pixel cell copied exactly from MPW + scaled logic with new layout Periphery + debugged/improved blocks + enhanced power network

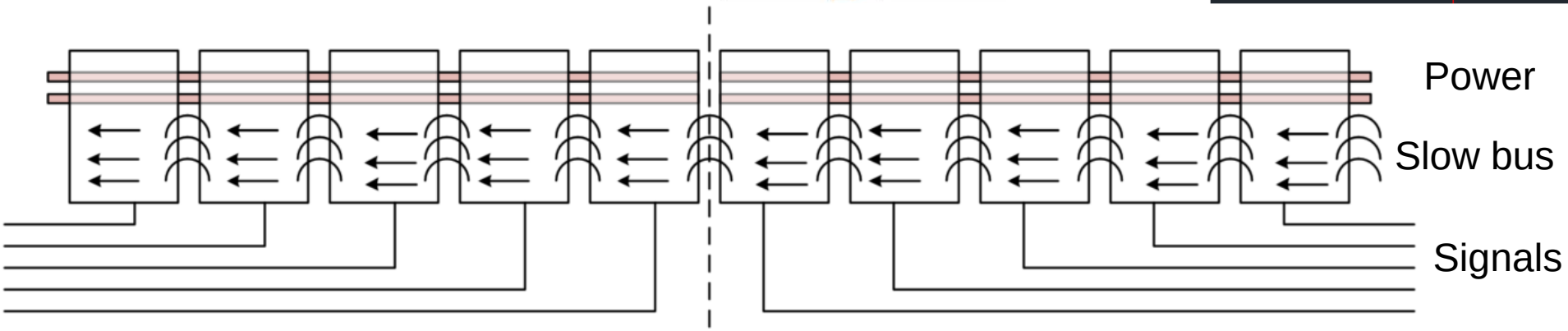
Flex cable design consideration

2mm margin for wire bonding and PCB Pads







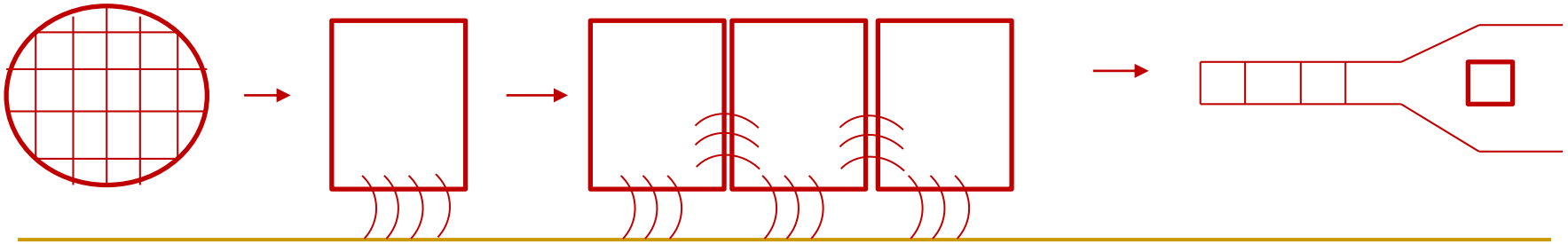


- **Design goals & considerations for the Flex PCB**
  - Minimum material budget
    - Minimum dead zone extension, limited height of PCB
      - Minimum set of signals on Flex
      - Inter-chip connection for slow controls through wire bonding → save some space & metal on PCB
    - Robust power supply
  - Manufacturability

Testability design & test plan consideration

- **All test features reserved, while the connection IOs will be reduced at different stages depending on chip test & study results**
  - Analog probe signals at the top part, accessible from the top pads
  - When mounted on ladder, only minimum self test possibilities can be reserved

1. **Probe Card design for the wafer test**
   - For all the pads at both sides
2. **Single chip test board design**
   - Designed with all the test features for the chip functional study
3. **Multiple chip test board for the ladder debugging**
   - Designed following the same manner as the ladder but on PCB
   - Signals and power supplies will be limited just with the ladder's dimension
   - Extra test signals can be connected to the extended area, to help debugging
4. **The real flex cable design for the ladder**
   - Core design and lessons will be exported from 3



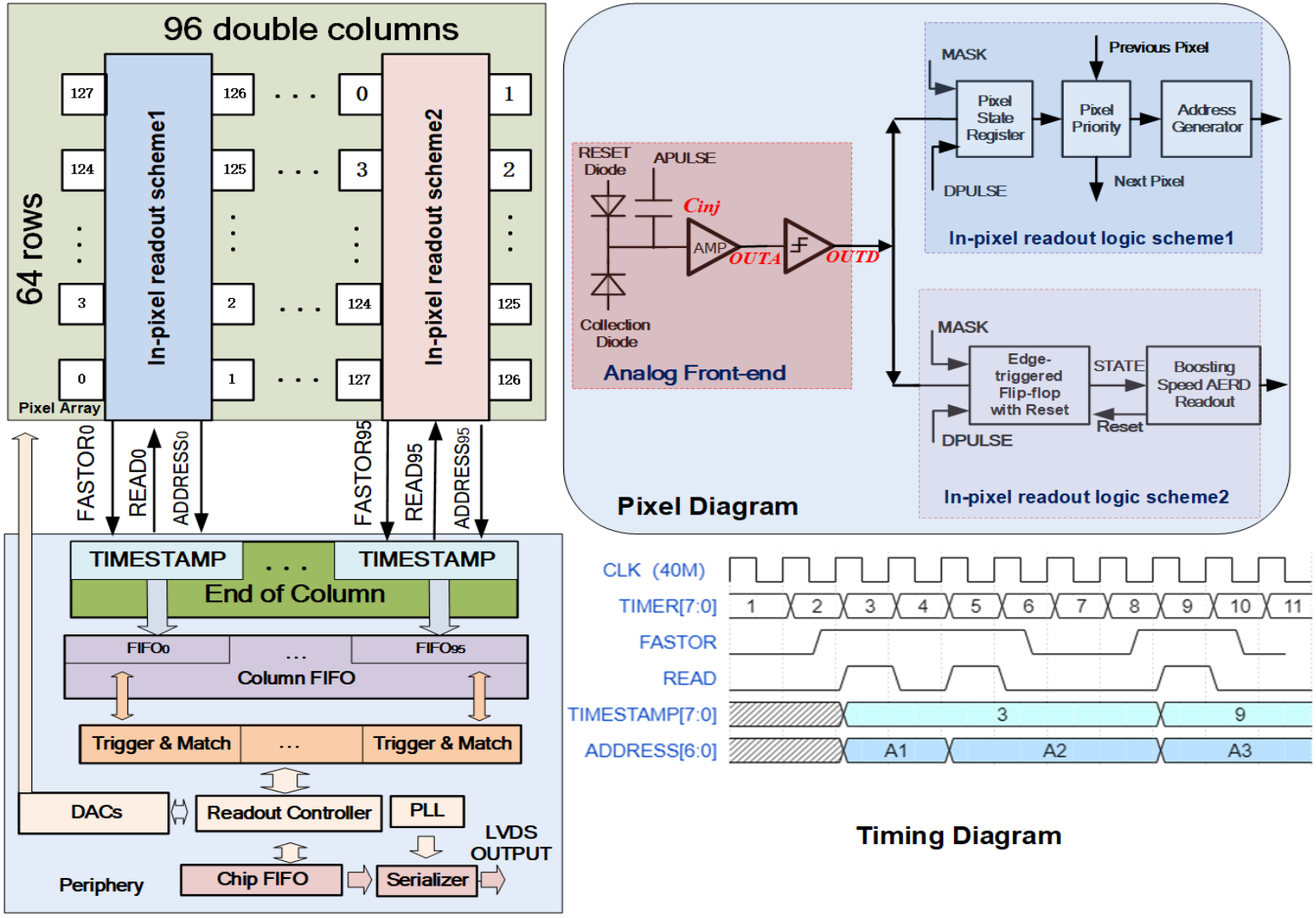
Summary

- **Small scale TaichuPix chips were developed to perform initial R&D**
  - Pixel pitch 25 μm, readout time 50 ns/pixel
  - Full signal chain & functionality verified with both electrical & radioactive test
- **The first full scale prototype have been designed**
  - Chip size is 25.7 mm × 15.9 mm, will be submitted for engineering run soon
- **Recent plan**
  - More tests on TaichuPix2 chip
  - Preparation for the full scale chip test (probe card, test PCB, flex cable …)

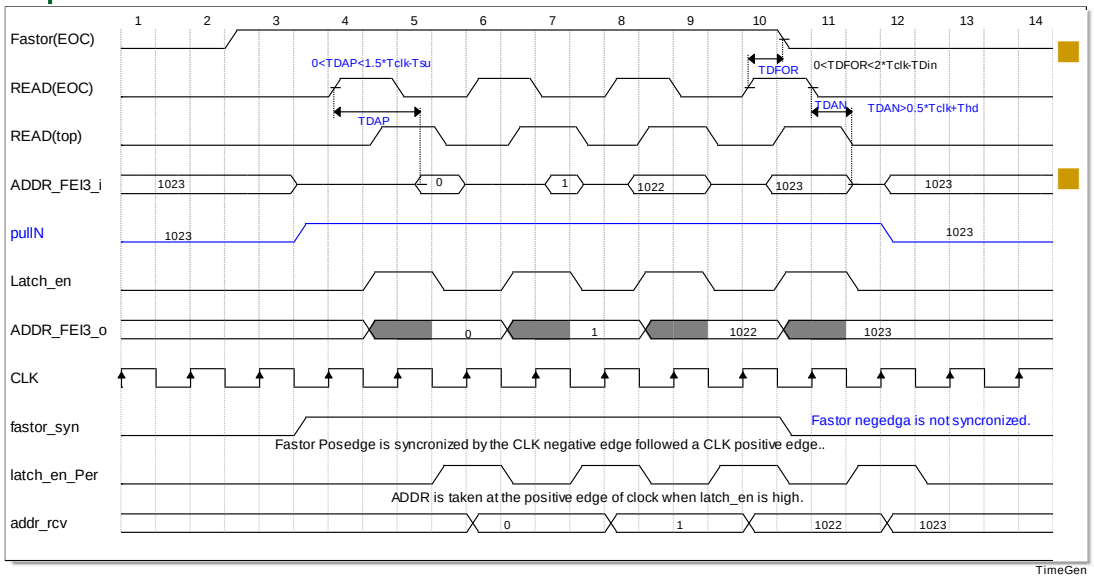
Thank you very much for your attention!

Backup

Chip diagram and timing



Readout & Periphery



Time stamp recorded when 'fastor' is valid

Each pixel readout by 2 clocks (50 ns)

- Worst delay ~ 25ns
  - Sim by 512 rows (full scale)
  - TDA: read sent –addr come
- Address latch @ 37.5ns
  - @1.5 clock
  - Enough headroom for all corners

- **Designed for low power**
  - Only the hit (fastor) info & address fannout from the pixel array
  - Only the read (acquisition) signal is fanned in to the pixel array
    - Clock & time stamp are localized only in the EOC, different from FE-I3
- **Optimized @ highest hit rate**
  - Common time stamp recorded for a full double column
    - For low power
    - Column is hit every 8.3us / pixel is readout in 2 clocks (50ns) / cluster size 3 pixels
    - Dead time 500ns – 98% trigger efficiency

Detection efficiency vs. Dead time