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A Novel Ultra-High-Speed Sensor Implementation with Variable Spatial and Temporal Resolution using Temporal Pixel Multiplexing

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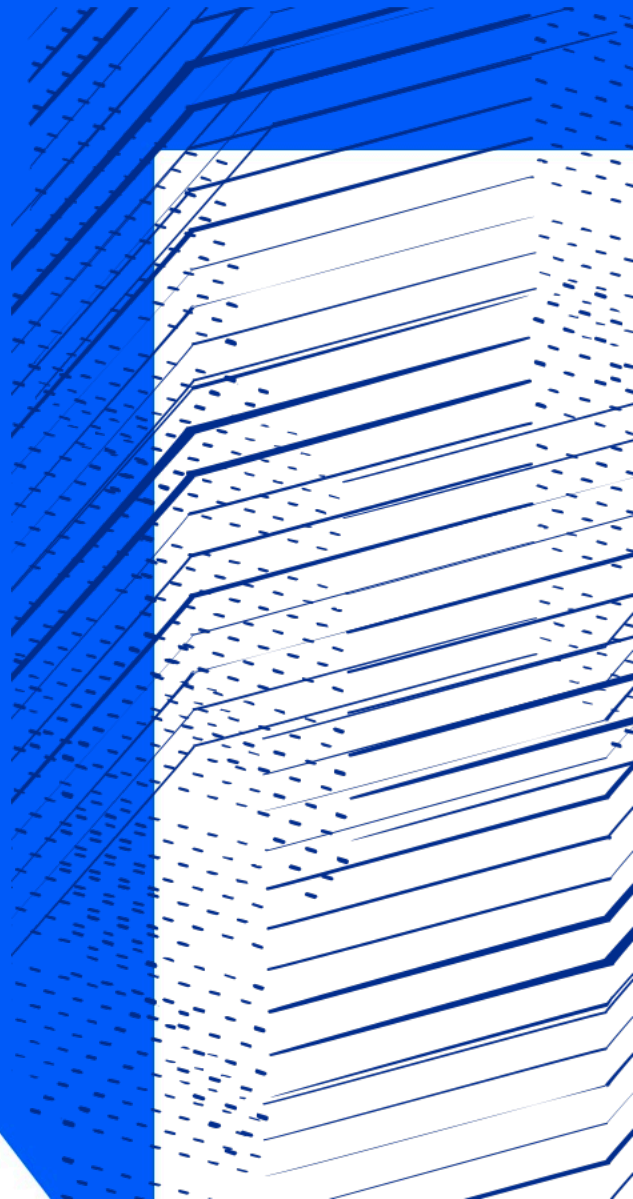
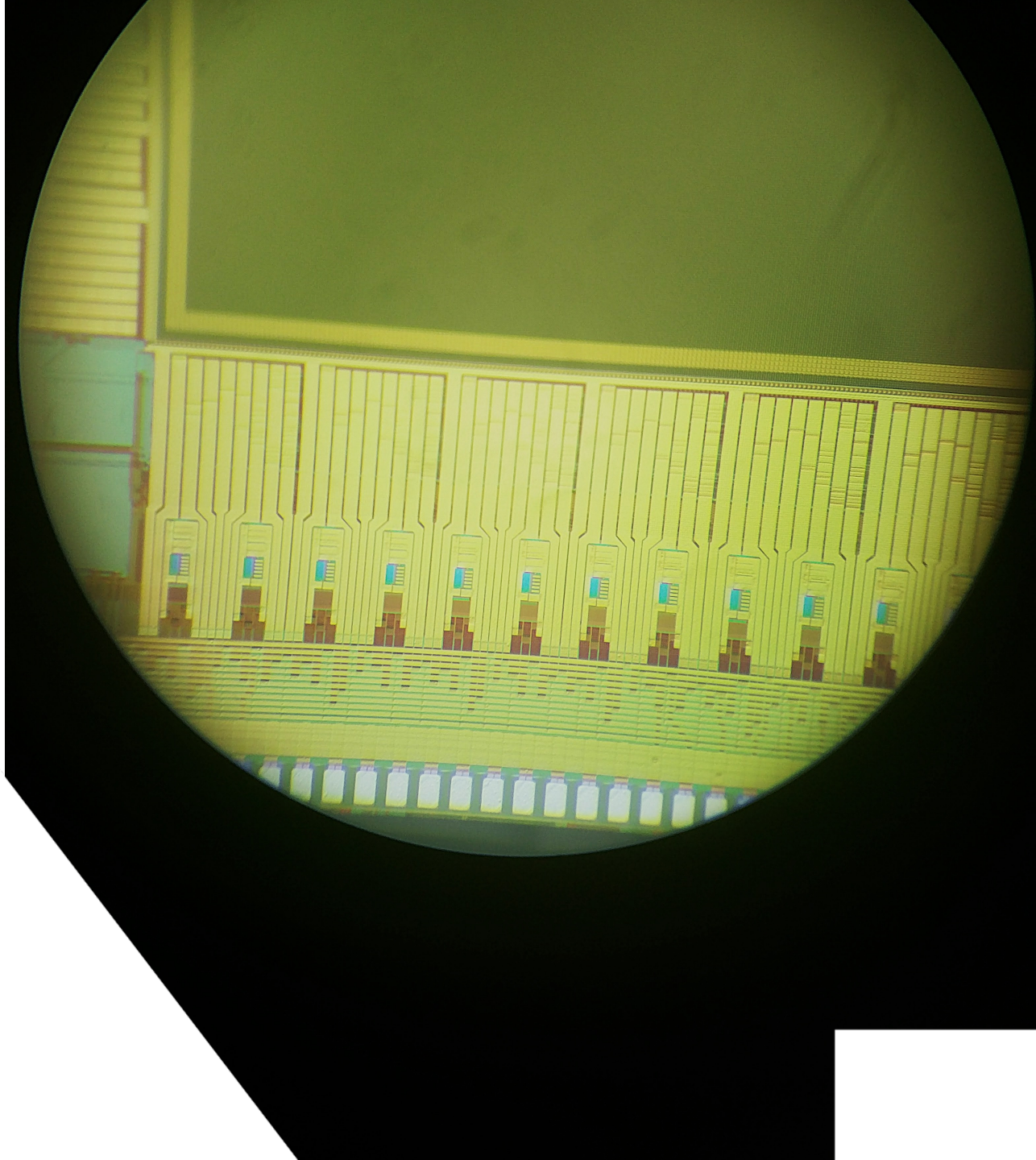


Overview



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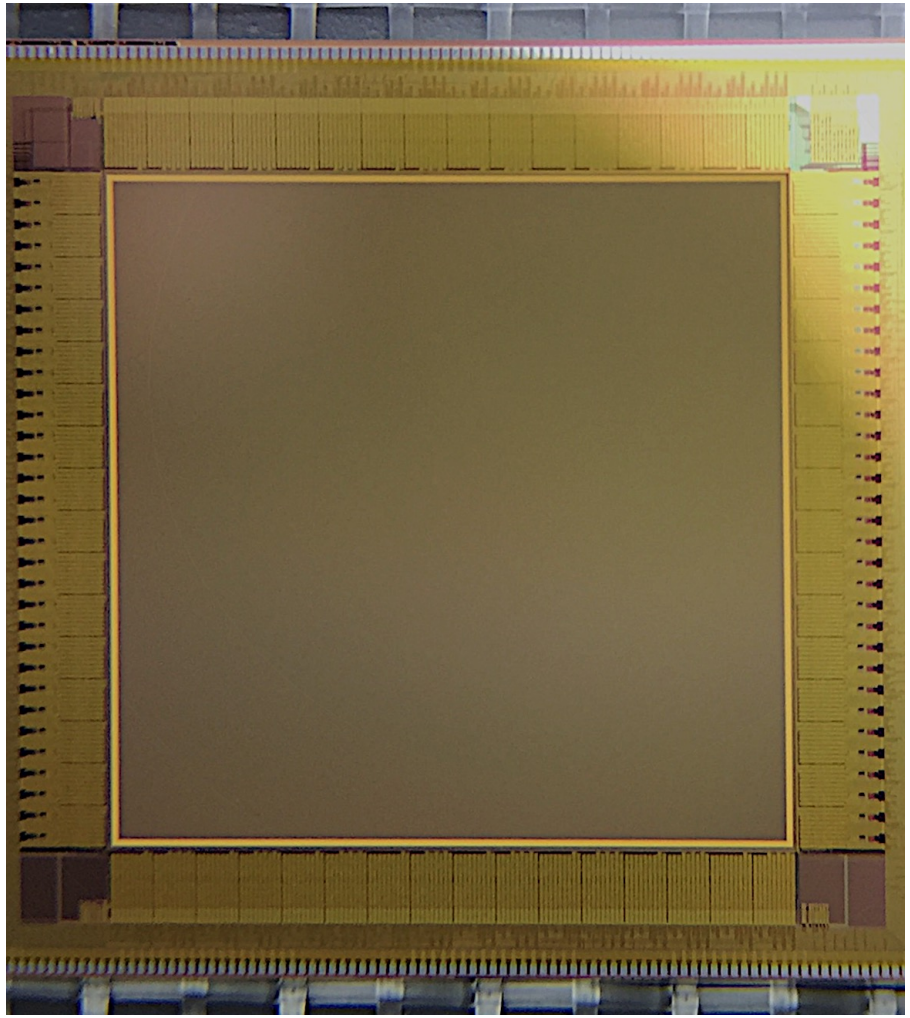
Primary application

High-Speed High-Resolution Optical Microscopy

The TPM CMOS sensor enables simultaneous high-speed imaging of cellular activity and high-spatial resolution imaging of anatomical structures.

- Pixel pitch: 10 µm × 10 µm
- Frame rate: up to 10 Mfps
- Pixel array format: 1024 × 1024
- Configurable number of frames
- Analogue readout



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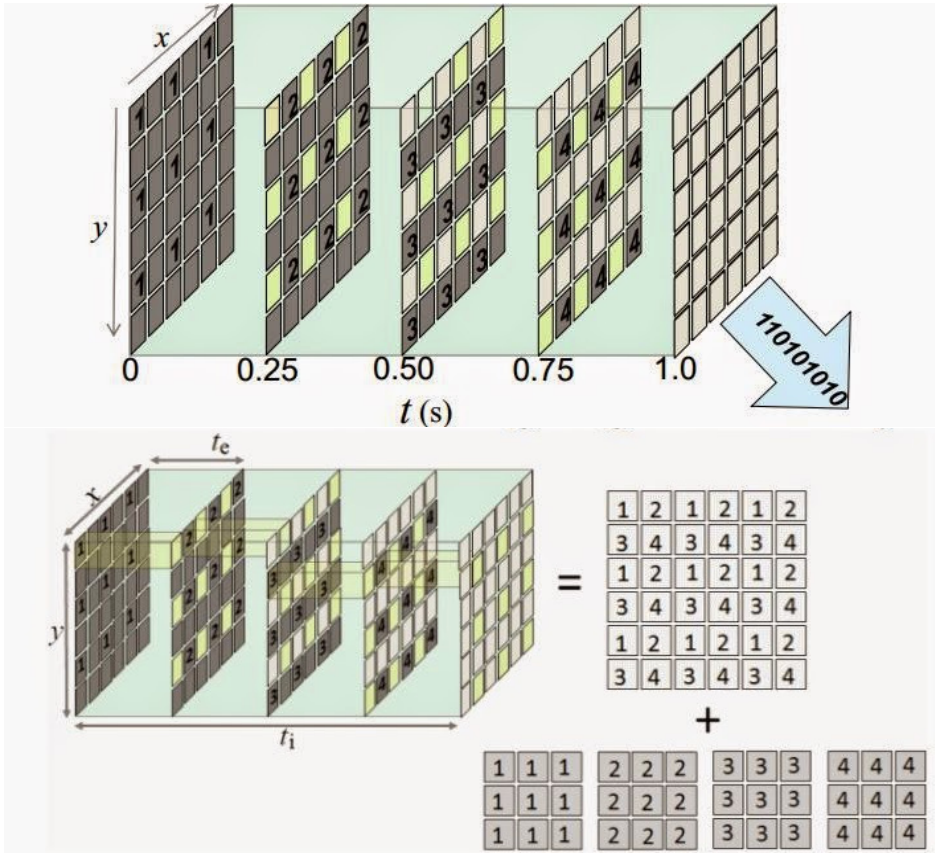
TPM concept

- Pixel array is arranged in a pre-specified grid pattern, e.g. a 2 × 2 grid pattern, as shown in figure on the right side of this slide.
- Each pixel with the same ID integrates light at the same time.
- Exposures of the resulting pixel groups are staggered throughout the detector's total exposure time.
- The full resolution frame is read out and digitized after all the pixel groups have finished integrating light.
- It can then be post-processed into a short movie, formed from lower resolution frames, consisting of pixels which have been exposed at the same time and collected together.
- In the example shown in this slide, 4 sequential 9-pixel subframes can be extracted from a single 36-pixel frame as follows:
  - The 1st subframe consisting of all pixels with ID #1;
  - The 2nd subframe consisting of all pixels with ID #2;
  - The 3rd subframe consisting of all pixels with ID #3;
  - The 4th subframe consisting of all pixels with ID #4.



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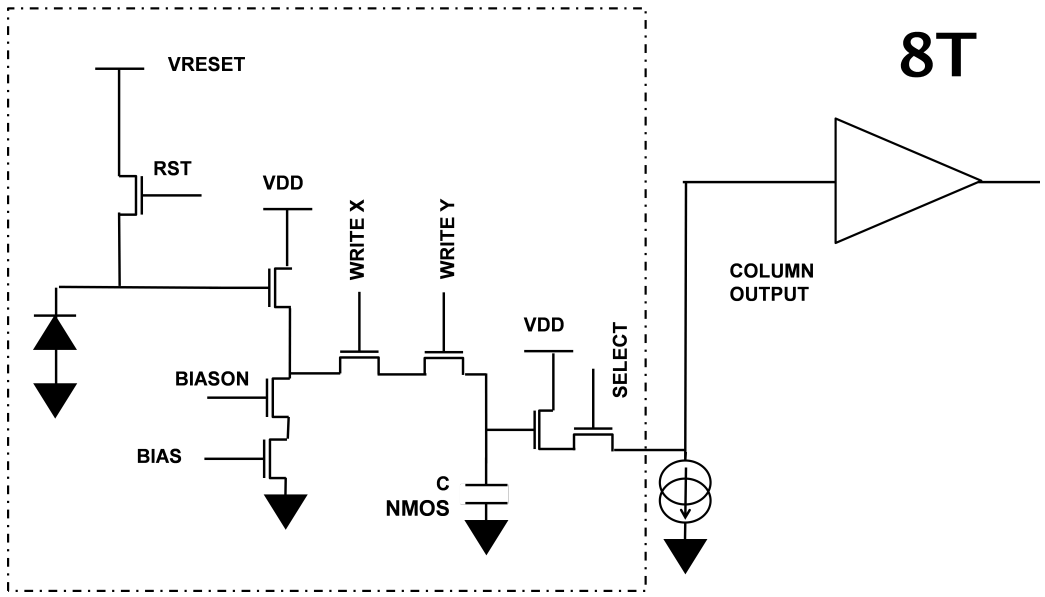
TPM pixel

- The TPM pixel is based on a 3T-APS architecture with a partially pinned photodiode (PPPD).
- The pixel contains 8 transistors and a storage capacitor.
- It has 2 internal source-followers (SFs):
  - The 1st SF is used to drive the in-pixel storage node;
  - The 2nd SF is used to drive the column readout node.
- In addition to that, it has 5 NMOS switches:
  - The RST switch is used to reset the photodiode node;
  - The BIASON switch is used to control the 1st SF;
  - The SELECT switch is used to control the 2nd SF;
  - The WRITEX and WRITEY switches are used to implement a pre-defined grid pattern for TPM exposures.



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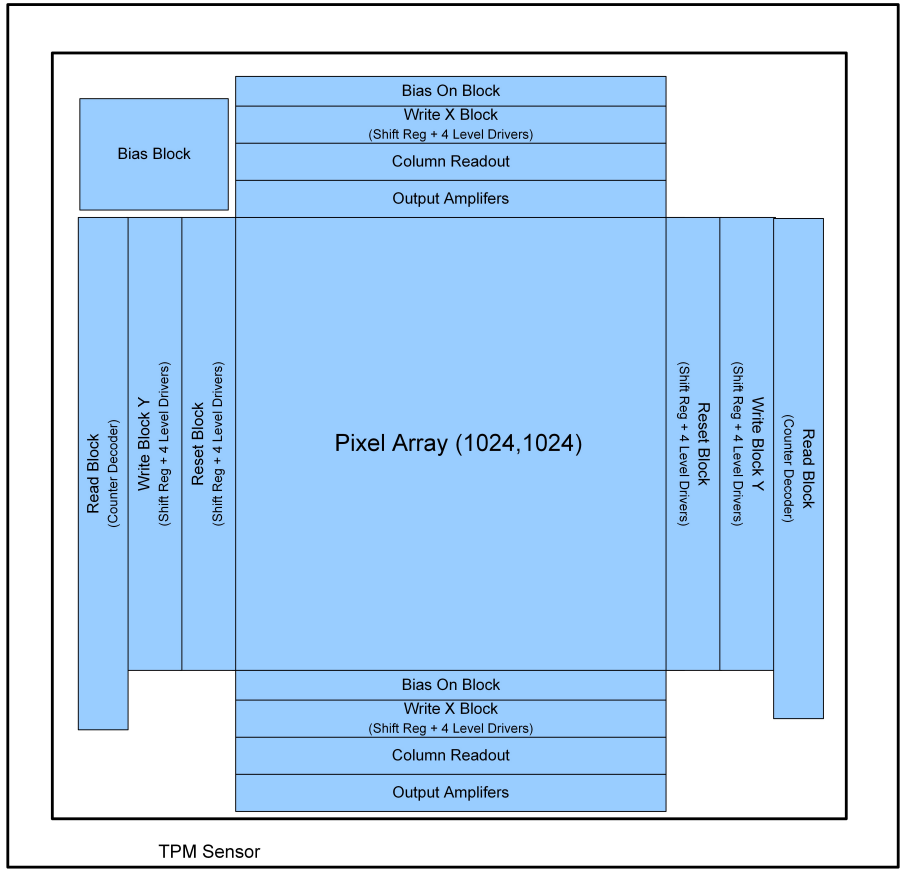
TPM sensor

- The TPM pixel is controlled by RST, BIASON, WRITEX, WRITEY and SELECT signals.
- To reduce the load of the line, the control signals are split in the middle of the pixel array and driven from both sides:
  - The SELECT signal is controlled by a 10-bit counter placed on the left and right side of the chip;
  - The RST and WRITEY signals are controlled by two separate 1024-bit shift registers placed on the left and right side of the chip;
  - The BIASON and WRITEX signals are controlled by two separate 1024-bit shift registers placed on top and bottom side of the chip.

- In case of a 4 × 4 TPM mask example, the pattern clocked through the BIASON, WRITEX and WRITEY shift registers should be 1000, whereas the pattern for the RST shift register should be 0111.
- The clock for WRITEX/BIASON shift registers should be 4 times slower than that for WRITEY/RST shift registers.



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TPM sensor operation (4 × 4 TPM mask)

Operating registers (col 1)

RST				
1	1	1	0	1
1	1	0	1	1
1	0	1	1	1
0	1	1	1	0

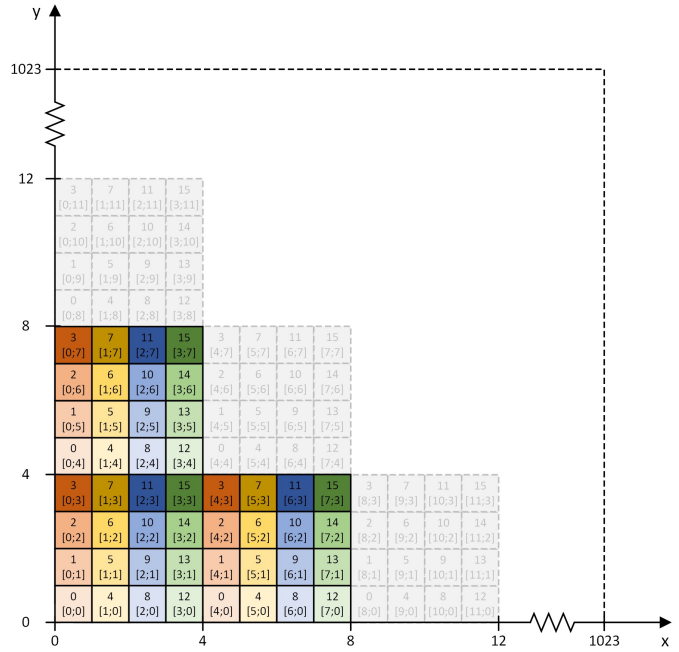
WRTY				
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
1	0	0	0	1

WRTX				
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
1	0	0	0	1

R – reset; I – integrate; IW – integrate/write

Each colour shows the state of registers and operation phase of pixels in 4x4 mask corresponding to it. New data bit is clocked in and cur
shifted on the negative edge of the clock. Note that, due to the size of 4x4 TPM mask, WRTX_*_CLK is 4 times slower than WRTY/RST_

4x4 TPM mask				
RST<3> → / WRTY<3> →	3	7	11	15
RST<2> → / WRTY<2> →	2	6	10	14
RST<1> → / WRTY<1> →	1	5	9	13
RST<0> → / WRTY<0> →	0	4	8	12
WRTX<0> →	BIASON<0> →	WRTX<1> →	BIASON<1> →	WRTX<2> →	BIASON<2> →	WRTX<3> →	BIASON<3> →



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TPM sensor operation (4 × 4 TPM mask)

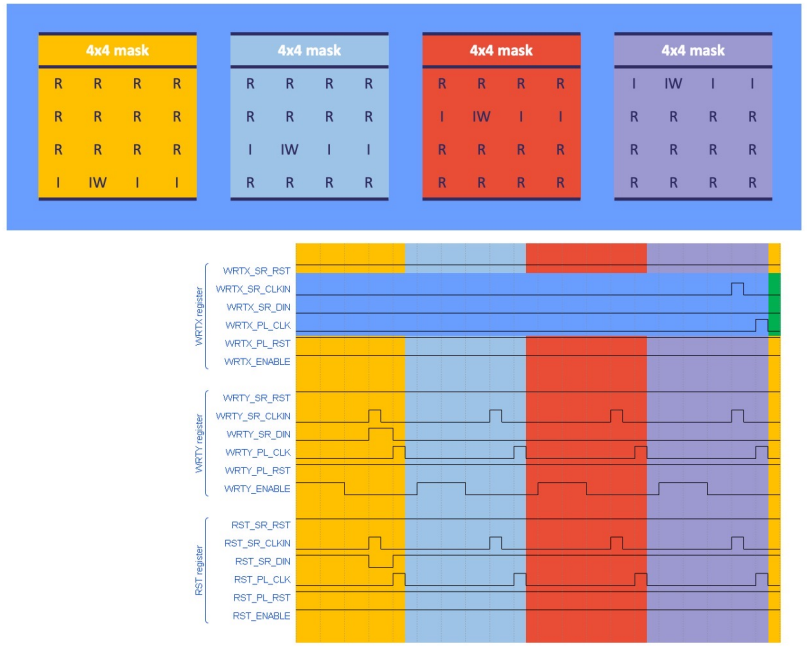
Operating registers (col 2)

RST				
1	1	1	0	1
1	1	0	1	1
1	0	1	1	1
0	1	1	1	0

WRTY				
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
1	0	0	0	1

WRTX				
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
1	0	0	0	1

R – reset; I – integrate; IW – integrate/write



Each colour shows the state of registers and operation phase of pixels in 4x4 mask corresponding to it. New data bit is clocked in and cur
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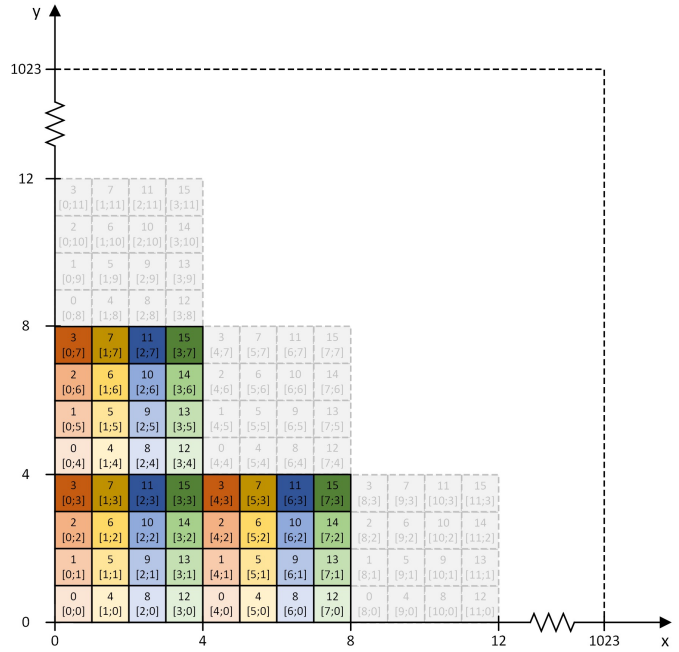
4x4 TPM mask				
RST<3> → WRTY<3> →	3	7	11	15
RST<2> → WRTY<2> →	2	6	10	14
RST<1> → WRTY<1> →	1	5	9	13
RST<0> → WRTY<0> →	0	4	8	12
	WRTX<0> → BIASON<0> →	WRTX<1> → BIASON<1> →	WRTX<2> → BIASON<2> →	WRTX<3> → BIASON<3> →



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TPM sensor operation (4 × 4 TPM mask)

Operating registers (col 3)

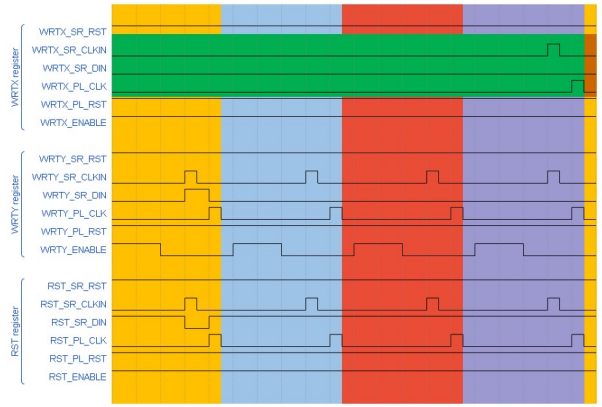
R – reset; I – integrate; IW – integrate/write

RST				
1	1	1	0	1
1	1	0	1	1
1	0	1	1	1
0	1	1	1	0

WRTY				
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
1	0	0	0	1

WRTX				
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
1	0	0	0	1

4x4 mask				4x4 mask				4x4 mask				4x4 mask			
R	R	R	R	R	R	R	R	R	R	R	R	I	I	IW	I
R	R	R	R	R	R	R	R	I	I	IW	I	R	R	R	R
R	R	R	R	I	I	IW	I	R	R	R	R	R	R	R	R
I	I	IW	I	R	R	R	R	R	R	R	R	R	R	R	R



Each colour shows the state of registers and operation phase of pixels in 4x4 mask corresponding to it. New data bit is clocked in and cur
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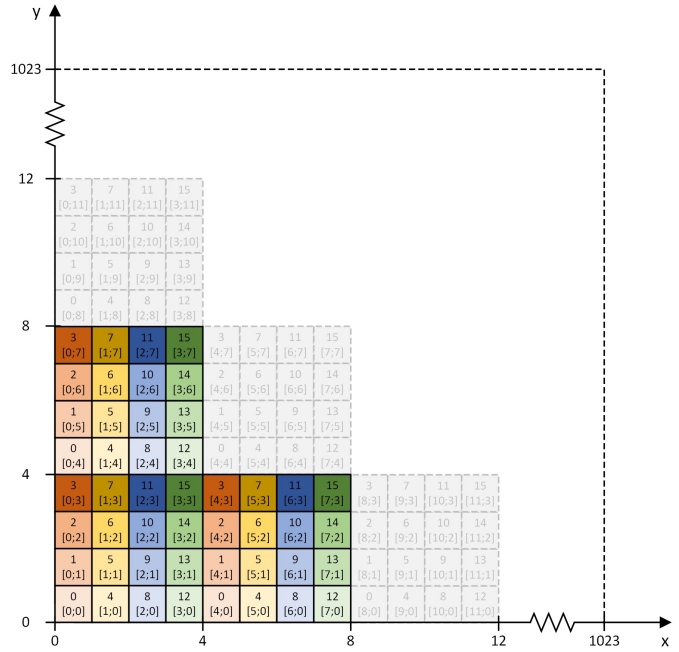
4x4 TPM mask				
RST<3> → WRTY<3> →	3	7	11	15
RST<2> → WRTY<2> →	2	6	10	14
RST<1> → WRTY<1> →	1	5	9	13
RST<0> → WRTY<0> →	0	4	8	12
	WRTX<0> → BIASON<0> →	WRTX<1> → BIASON<1> →	WRTX<2> → BIASON<2> →	WRTX<3> → BIASON<3> →



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TPM sensor operation (4 × 4 TPM mask)

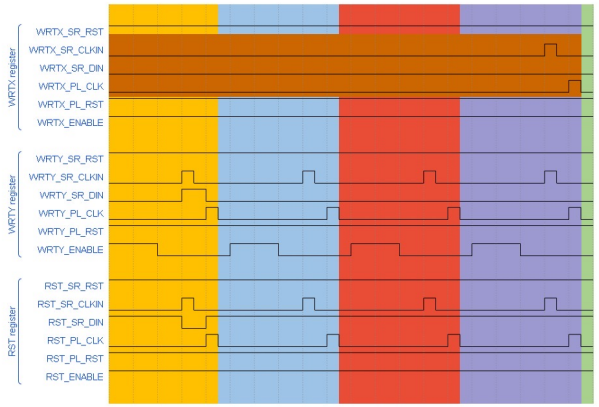
Operating registers (col 4)

RST				
1	1	1	0	1
1	1	0	1	1
1	0	1	1	1
0	1	1	1	0

WRTY				
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
1	0	0	0	1

WRTX				
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
1	0	0	0	1

R – reset; I – integrate; IW – integrate/write



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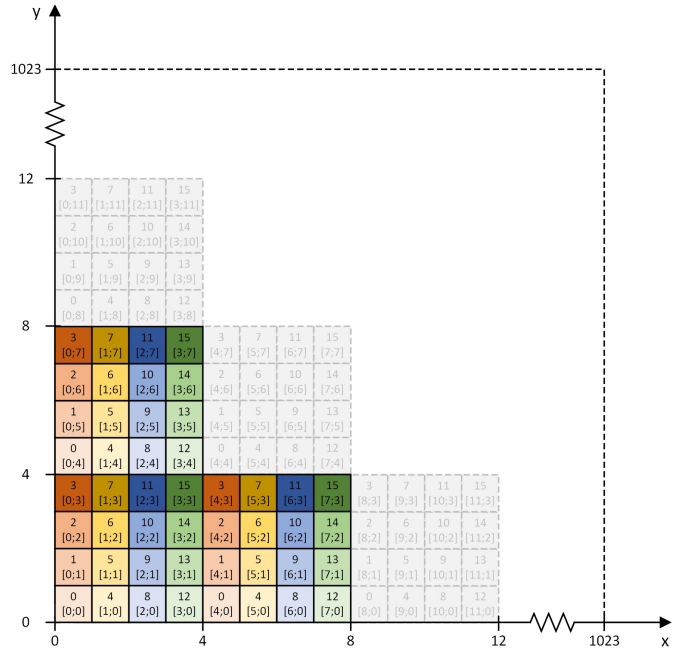
4x4 TPM mask				
RST<3> → WRTY<3> →	3	7	11	15
RST<2> → WRTY<2> →	2	6	10	14
RST<1> → WRTY<1> →	1	5	9	13
RST<0> → WRTY<0> →	0	4	8	12
	WRTX<0> → BIASON<0> →	WRTX<1> → BIASON<1> →	WRTX<2> → BIASON<2> →	WRTX<3> → BIASON<3> →



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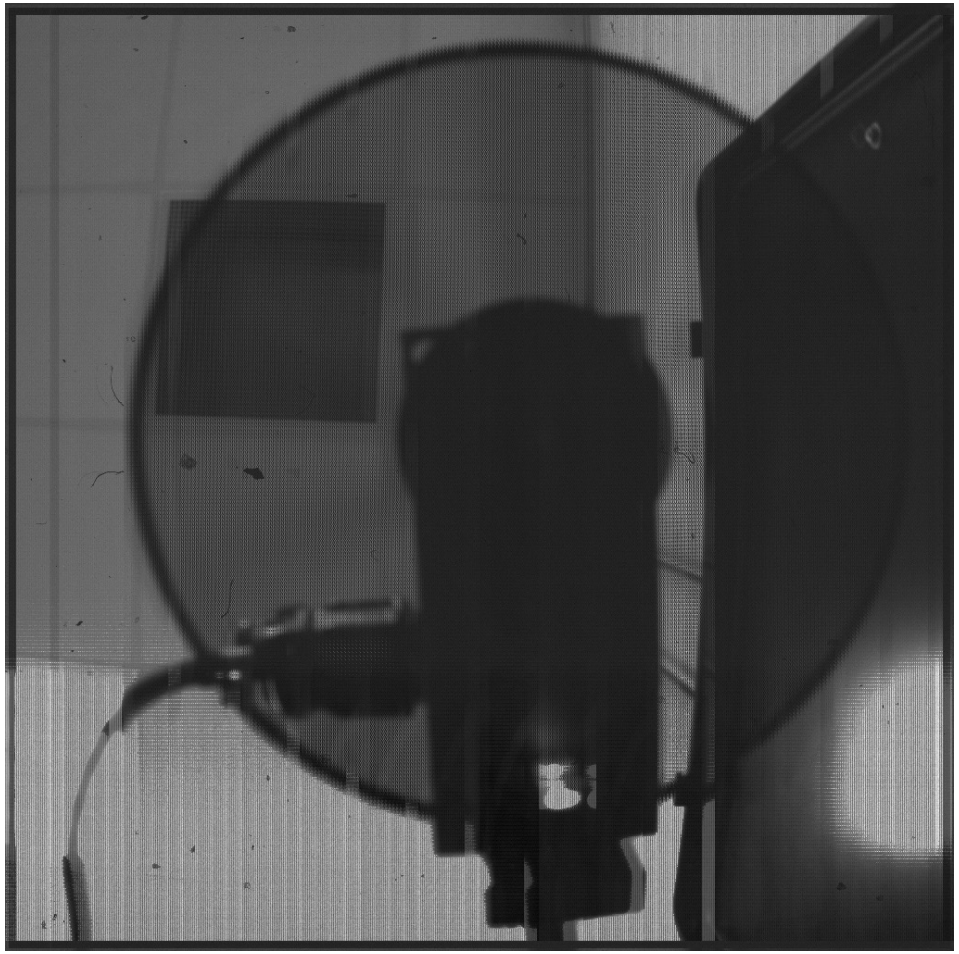
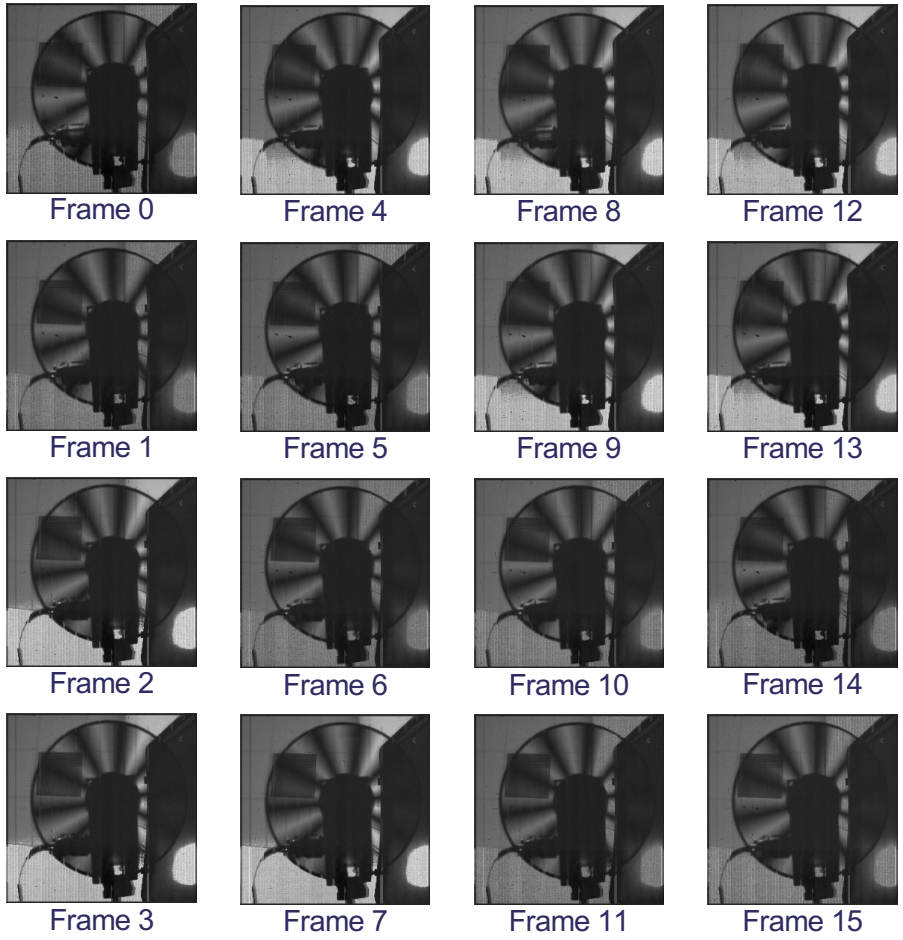
TPM example with a 4 × 4 grid pattern





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Summary

- **Tower Semiconductor 180 nm 1.8/3.3 V CIS process technology**
- **High resolution:** up to 1K × 1K
- **Very high framing rate:** up to 10 Mfps
- **Configurable number of frames**
- **Analogue readout**

Parameter	Specifications
Pixel type	8T with PPPD
Floating diffusion capacitance	5.6 fF
Conversion gain	17 μV/e^-
Maximum full-well capacity	~52.5 ke^-
Fill factor	~53%
Pixel unit size	10 μm × 10 μm
Pixel array format	1024 × 1024
Effective pixel array format	1000 × 1000
Sensitive area	10 mm × 10 mm
Minimum integration time	100 ns @ 10 MHz (TPM)
Maximum output voltage swing	1 V
Maximum readout speed	10 MS/s
Readout frame rate	300 fps

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Questions?

www.technologysi.stfc.ac.uk/Pages/CMOS-Sensors-Design.aspx

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Thank you

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