# Status of the Upgrade Project of the CMS Tracker for the High-Luminosity LHC

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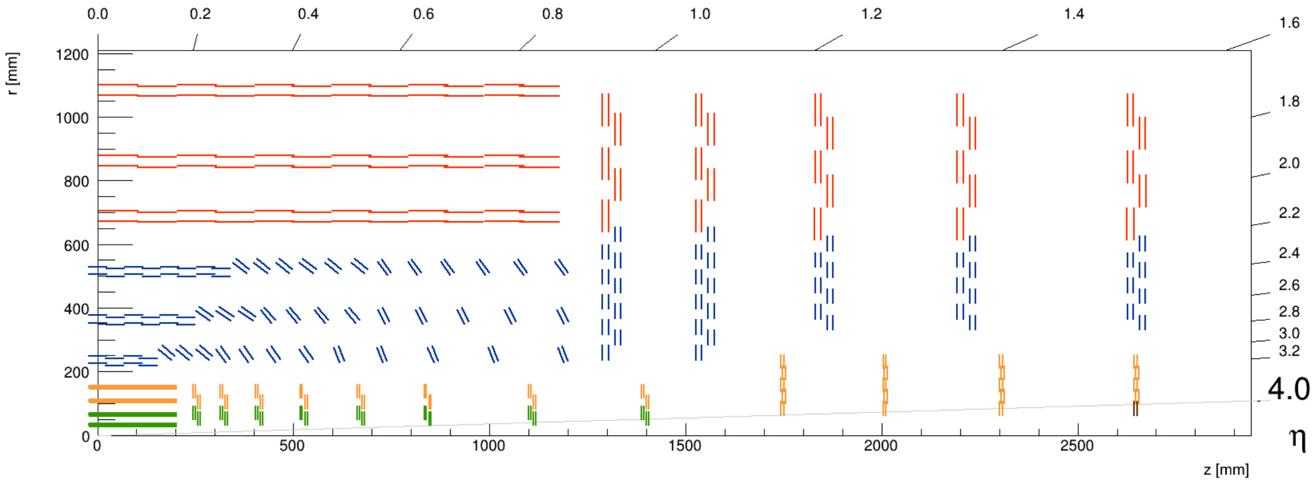
on behalf of the CMS Collaboration

# The Tracker upgrade for HL-LHC

- High-Luminosity LHC scenario
  - Instantaneous luminosity up to $5 \times 10^{34}$ $cm^{-2}s^{-1}$ ($7.5 \times 10^{34}$ $cm^{-2}s^{-1}$ )
    - Increase (6x) granularity in the innermost detector
    - More selective Level1 trigger including tracking
  - Integrated luminosity up to 3000 $fb^{-1}$ (ultimate HL-LHC scenario: 4000 $fb^{-1}$)
    - Improve (10x) radiation tolerance of the detectors
    - Easy maintenance and replacement of the innermost region




*Outer Tracker TB2S*
*7608 strip-strip pT-modules*
***31M** channels*

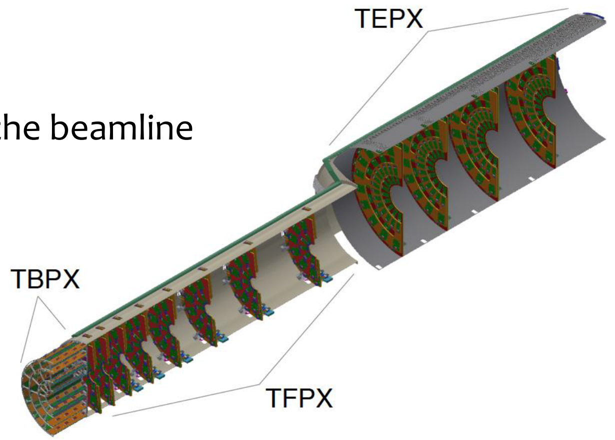
*Outer Tracker TBPS*
*5592 pixel-strip pT-modules*
***170M + 11M** channels*

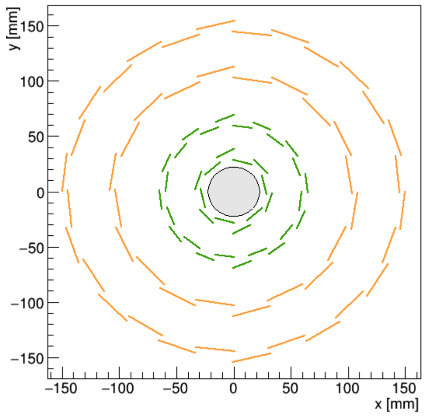
*L1 Trigger*

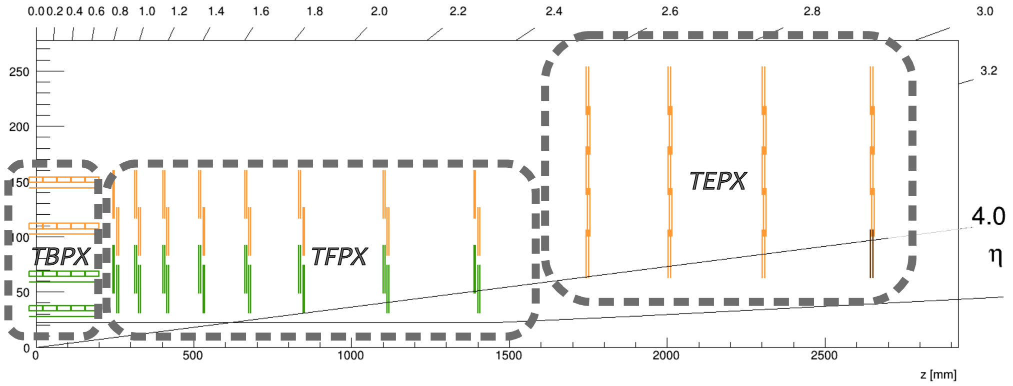
*Inner Tracker*
*3892 hybrid pixel 1x2 or 2x2 chip modules*
***2G** channels*

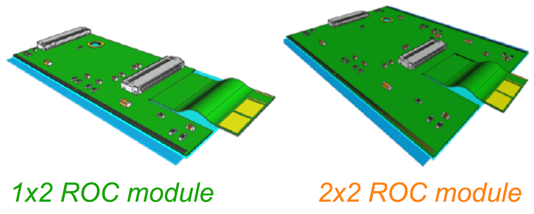
# Inner Tracker

- Detector layout
  - Extended coverage up to |η|=4, innermost modules located at r=2.75 cm from the beamline
  - 4 barrel layers (TBPX) + 2x8 small discs (TFPX) + 2x4 large discs (TEPX)
    - TBPX: no crack at z=0, two ladders per layer skewed in rφ for the insertion in CMS
    - TFPX and TEPX: each disc made of 4 identical dees
  - Hybrid pixel modules
    - Two module types: 1x2 and 2x2 readout chip per module

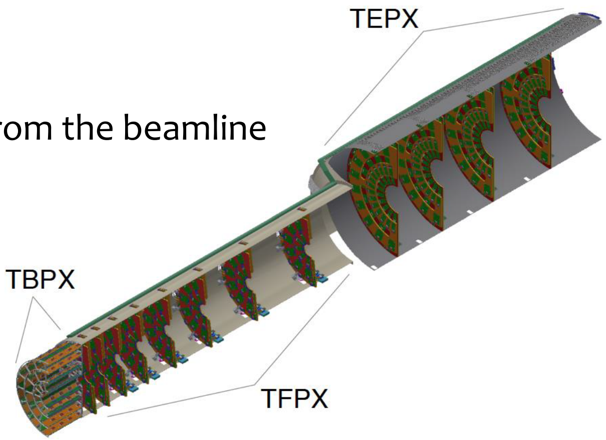


# Inner Tracker




- Detector layout
  - Extended coverage up to $|\eta|=4$, with innermost modules located at r=2.75 cm from the beamline
  - 4 barrel layers (TBPX) + 2x8 small discs (TFPX) + 2x4 large discs (TEPX)
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    - Two module types: 1x2 and 2x2 readout chip per module
  - 2020/Q4: revision of the expected radiation levels in CMS using updated FLUKA maps

Ultimate luminosity scenario for HL-LHC (4000 $fb^{-1}$)

| | LHC run 4+5 | | LHC run 4+5+6 | |
|---|---|---|---|---|
| | 1e16 $n_{eq}/cm^2$ | Grad | 1e16 $n_{eq}/cm^2$ | Grad |
| TBPX L1 | 1.88 | 1.03 | 3.51 | 1.91 |
| TFPX R1 | 1.25 | 0.81 | 2.34 | 1.50 |

Out of reach scenario independently from the choice of the sensor technology

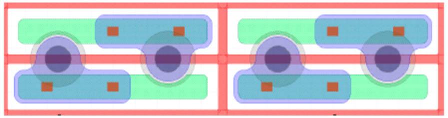
Adopt as baseline:

- A replacement of the innermost layer/ring after LHC long-shutdown 5
- Benchmark for the detector design : 1.9e16 $n_{eq}/cm^2$ fluence and 1.0 Grad Total Ionizing Dose

# Inner Tracker Sensors

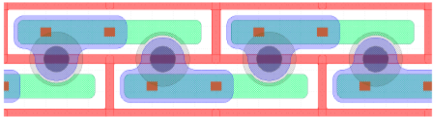
(more details in M.Hajheidari's talk)

- Decision to be taken by 2021/Q4 (intense R&D program in the shadow of the final ROC)
  - Baseline option:
    - n-on-p planar, 150 um active thickness, 25x100 um$^2$ cell size everywhere
    - bitten implant, no punch-through bias dot
    - hit efficiency >99% after ~2.0e16 $n_{eq}$/cm$^2$, parylene-N coating for spark protection up to max operation voltage 800V

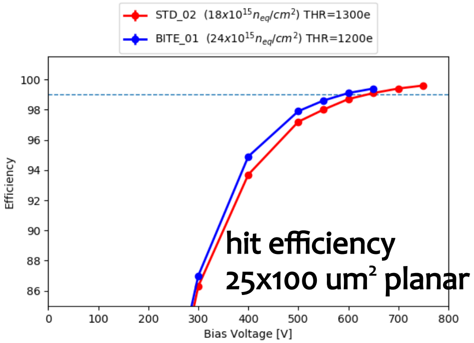


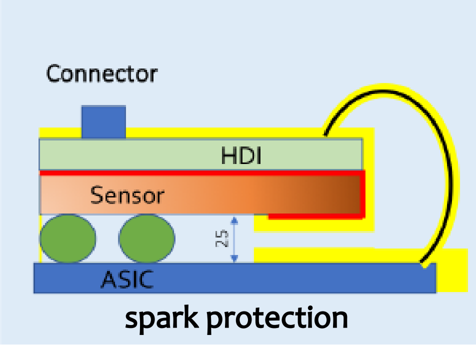
*standard bitten implant design*

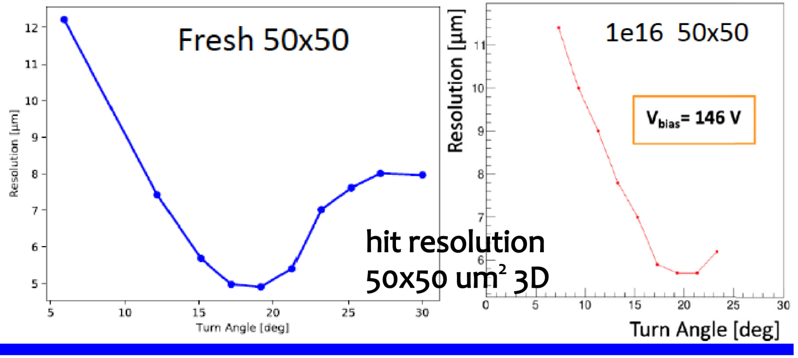
  - Alternatives under investigation:
    - Technology
      - 3D for TBPX L1 and TFPX R1: better power consumption, almost no degradation of hit resolution after 1.0e16 $n_{eq}$/cm$^2$
    - Cell aspect ratio
      - 50x50 um$^2$ still considered for the discs
      - Planar sensors with bricked layout in the central η region



*bricked design*

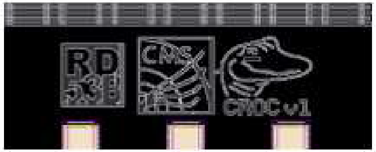


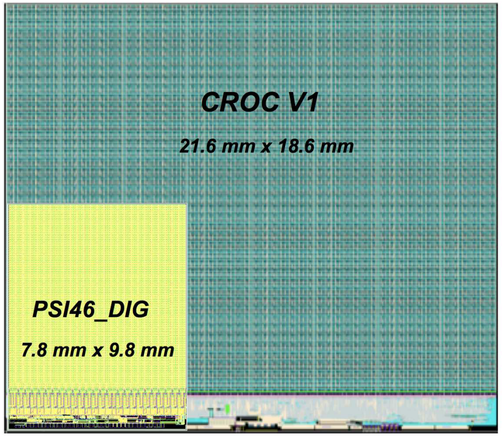



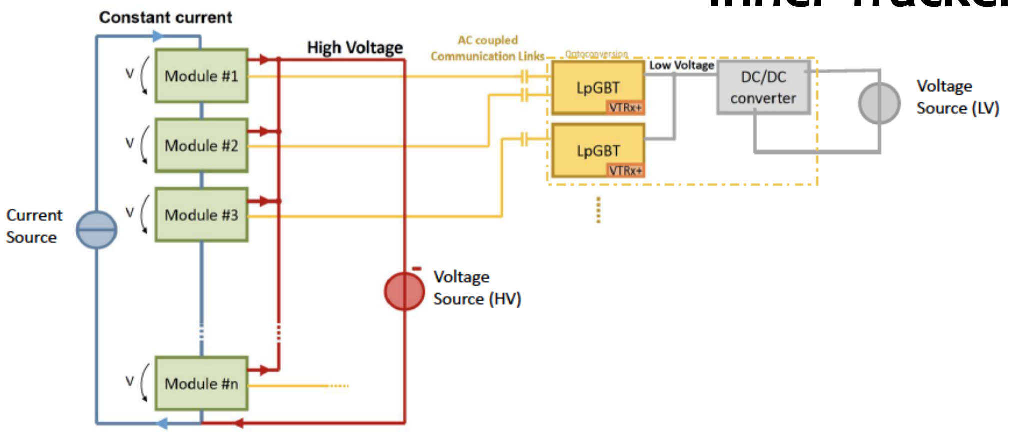
# Inner Tracker ASIC

- Readout chip: C-ROC
  - Developed in CMOS 65nm technology within the CERN RD53 project
    - Radiation tolerant up to 1 Grad (verified at high dose rate) and robust against SEU effects
    - Bonding pad reticles fitting both 50x50um$^2$ and 25x100 um$^2$ pixel cells
    - Low power consumption < 1 W/cm$^2$ at max trigger rate (CMS Level1: 750 kHz)
    - Serial powering via on-chip shunt-LDO regulators (1 for analog + 1 for digital sections) to supply IT the needed 50 kW with a limited mass of the power cables
- CMS version of the ASIC submitted in June 2021, first wafers already at CERN
  - Full size ASIC: 432x336 channels
  - Analog FE linear architecture featuring an in-time threshold O(1000e)
  - 4 bit digital readout with selectable 6-to-4 bit dual slope ToT mapping for charge compression (elongated clusters, heavy ionizing particles)



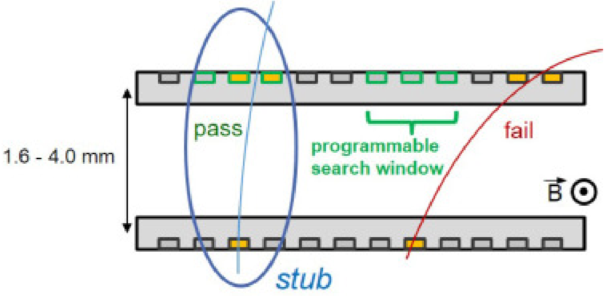
# Inner Tracker System Architecture

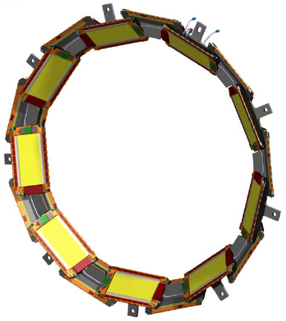



- Powering: serial power
  - Modules grouped in 500 serial power chains, up to 12 modules in a chain
  - Chips in a module connected in parallel (4A for 1x2 ROC modules and 8A for 2x2 ROC modules)
  - Sensor bias following the serial power chains with a single return line
    NB: for 3D sensors, IV acceptance criteria adapted to account the extra module-to-module change of the HV reference
  - Single power supply module: current source (SP), HV for the sensor (0-800V), LV for *portcards* and for *pre-heaters* required by $CO_2$ cooling
  - Only Cu cladded Al wires in the detector volume
- Readout
  - C-ROC readout serially via e-links (1.6 m max length) to portcards hosting VTRX+ and lpGBT (electro-opto conversion) + DC-DC converters located at larger radii (less radiation harsh environment)
- Cooling based on evaporative $CO_2$ ($T_{set}$=-35 °C) distributed in 1.8 mm outer diameter stainless steel pipes (168 cooling loops)

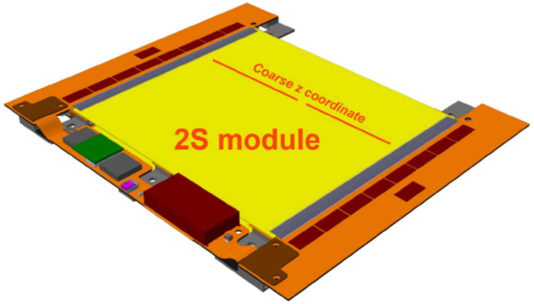
# Outer Tracker

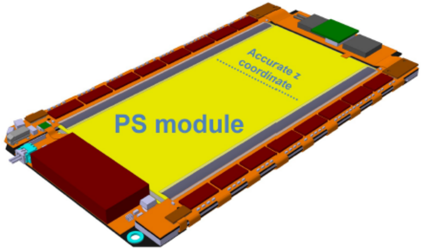
- Detector layout
  - Design driven by Level1 trigger capability: 40 MHz reconstruction of all pT>2 GeV tracks (~3% of the tracks) within a time budget of 4 us
  - *pT module* concept: pT discrimination provided in front-end electronics through hit correlations (*stubs*) between two closely spaced sensors
  - Coverage up to |η|=2.4
  - Tilted section in the barrel for full efficiency on stubs from inclined tracks
- Outer Tracker modules
  - self-contained unit connected with only 2 optical fibers and 3 wires to the back-end



10x10 $cm^2$




10x5 $cm^2$

## 2S (strip-strip) modules

- sensor (strips): 2x5 cm, 90 um pitch, planar, AC coupled

## PS (pixel-strip) modules

- top sensor (strips): 2x2.5 cm, 100 um pitch, planar, AC coupled
- bottom sensor (pixels): 1.5 mm x 100 um, planar, DC coupled

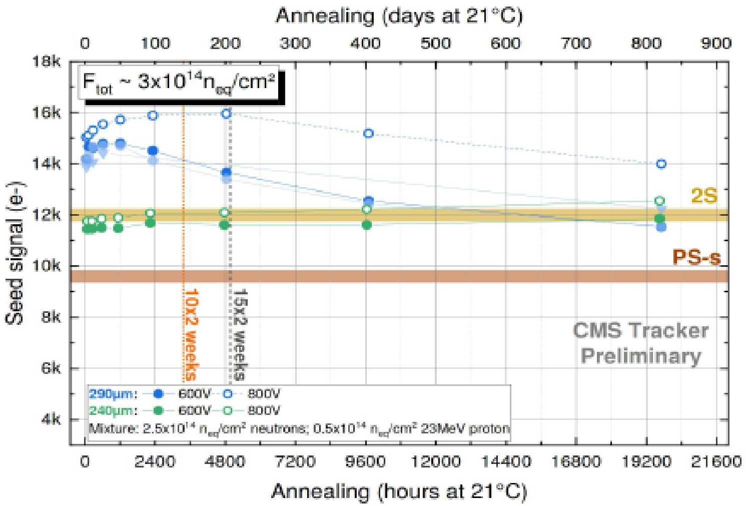
# Outer Tracker Sensors

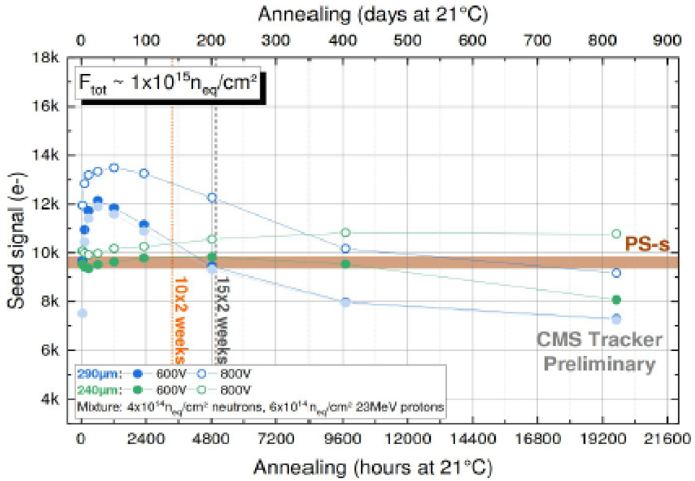
- Final design
  - n-on-p silicon, 290 um active thickness
    - ddFZ option already revoked by the company

      FZ thinned sensors (240 um) option discarded by CMS in 2019 because of mechanical robustness and cost
    - Figure of merit: >98% efficiency on seed signal after 4000 $fb^{-1}$ at an affordable bias voltage, where efficient detection of seed signal is defined as:

      MPV/3 > threshold and threshold = 4 * electronic noise

      Practically: 12ke (2S sensor) 9.6ke (PS-s sensor)
    - Expected fluence after 4000 $fb^{-1}$
      - 95% of 2S sensors: $\Phi$<3e14 $n_{eq}/cm^2$ → HV=600 V (●)
      - 95% of PS sensors: $\Phi$<7e14 $n_{eq}/cm^2$ → HV=800 V (○)
  - single supplier: HPK
- Status: pre-production (5% of the sensors) completed for 2S, PS-strip and PS-pixel
  - excellent matching of specs (<1% bad strips, $I_{2S@600V}$<7.5 uA)



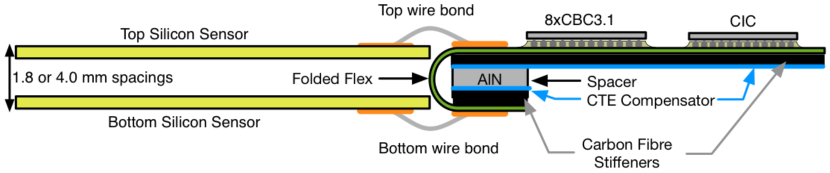
# Outer Tracker ASICs

- ASICs
  - Three sensor-specific readout ASICs
    - CBC (2S), SSA (PS-strip), MPA (PS-pixel): binary readout and correlation of hits from top/bottom sensors
  - One common “concentrator” chip (CIC) forwarding hits & stubs to lpGBT
  - Status:
    - CBC3.1 production started at GlobalFoundry (delivery for 2021 not affected by shortage of Si wafers)
    - Second version(s) of SSA, MPA, CIC: prototypes ready for proto-hybrids and proto-MaPSA 2021/Q4-2022/Q1

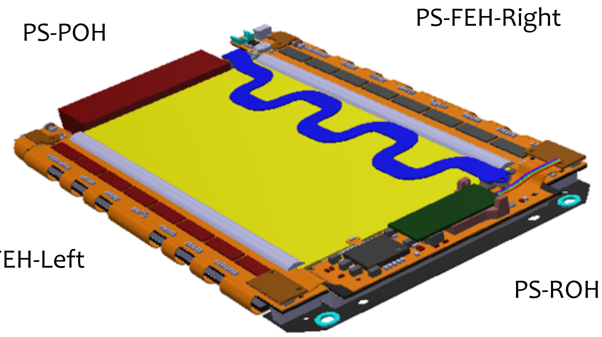
# Outer Tracker Hybrids

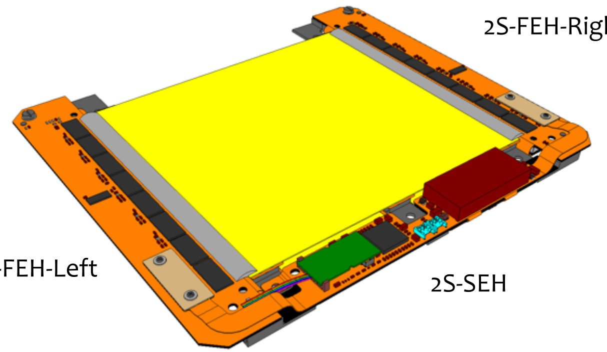
(more details in F.Zhang 's poster)

- Hybrids
  - Total of 15 different hybrid types
  - Front-end hybrids (FEH)
    - routing signals from top and bottom sensors to readout ASICs
    - made of polymide flex circuits, CF stiffners, AlN spacers
  - Service hybrids (SEH, ROH, POH)
    - DC-DC converter
    - Optical readout + lpGBT



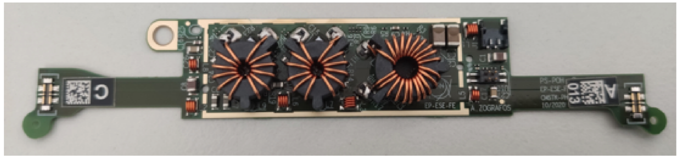

2S-FEH



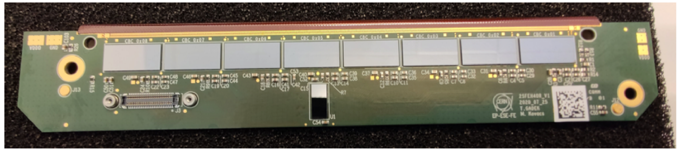




10 hybrid types for PS (1.6, 2.6, 4.0 mm spacers) + 5 hybrid types for 2S (1.8, 4.0 mm spacers)

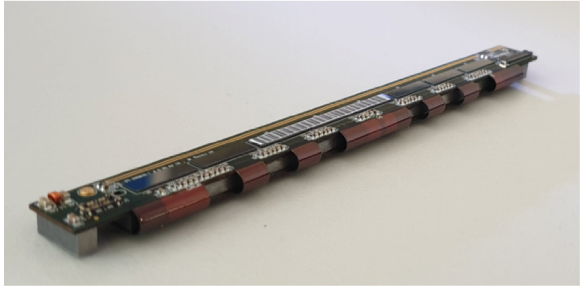
# Outer Tracker Hybrids

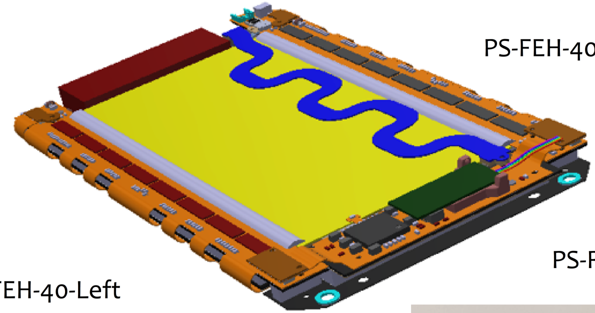


PS-POH



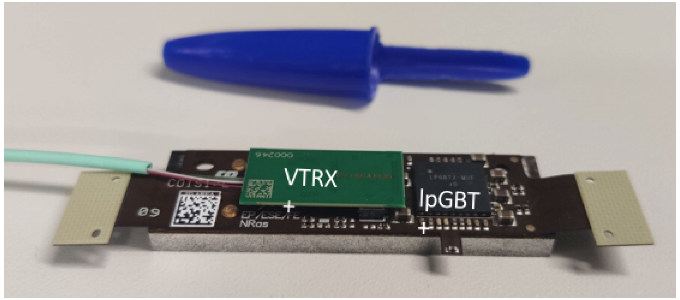
PS-FEH-40-Right





PS-FEH-40-Left

PS-ROH-40



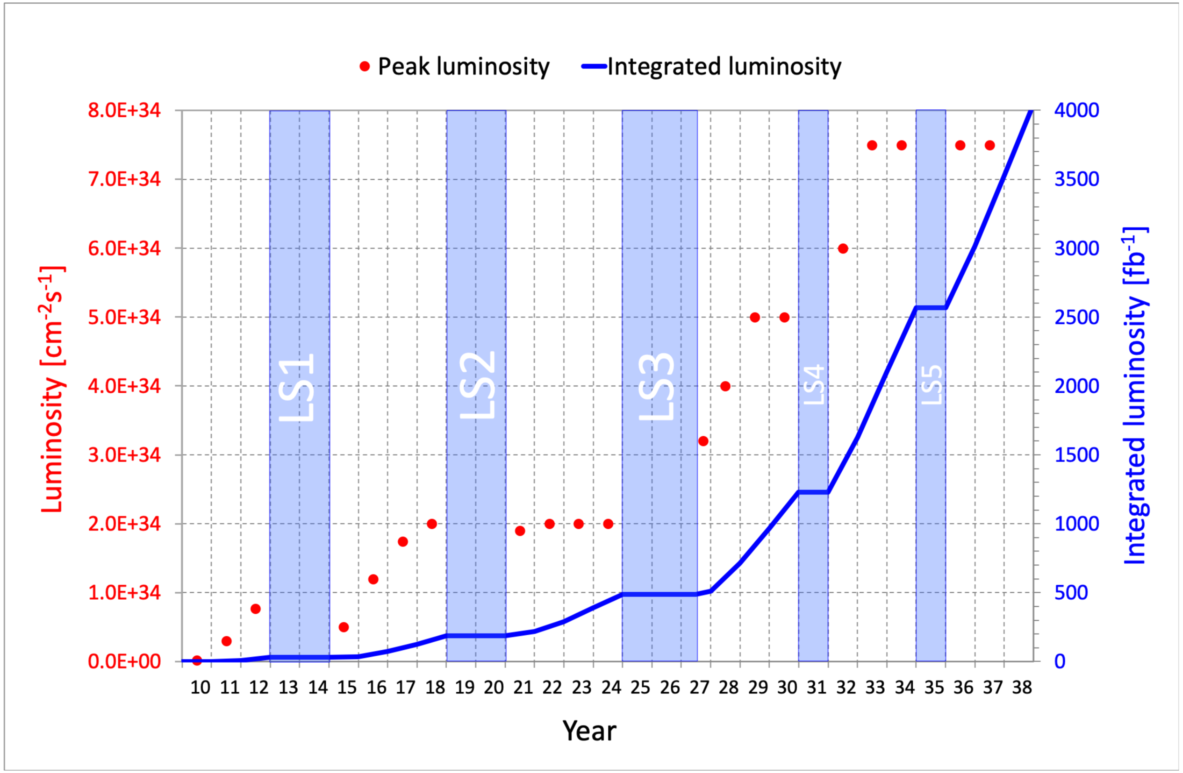

- Prototypes for all the 15 hybrid flavors now available for test
- Invitation to tender done; order to be placed in 2021/Q4

# Summary

- Full exploitation of HL-LHC instantaneous and integrated luminosity requires an extremely challenging design of the tracking detector
- Outer Tracker: prototypes existing for almost all the components, few already in the (pre-)production stage
- Inner Tracker: prototype phase still on-going, major decision on the technology for the sensors to be taken by the end of 2021
- Construction will not mark the end of the R&D effort as part of the Inner Tracker will be replaced at about half of the HL-LHC lifetime

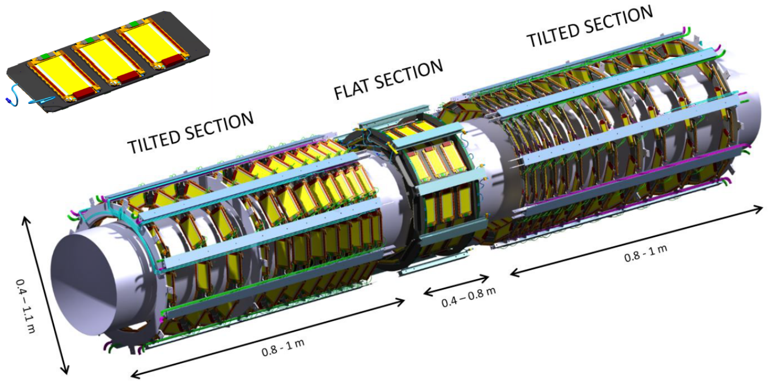
# EXTRA SLIDES

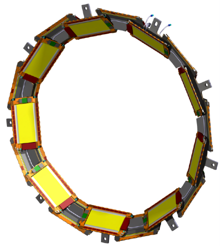
# High-Luminosity LHC timeline

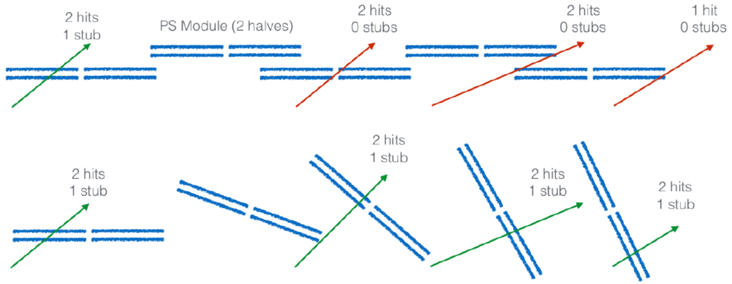


# Outer Tracker layout

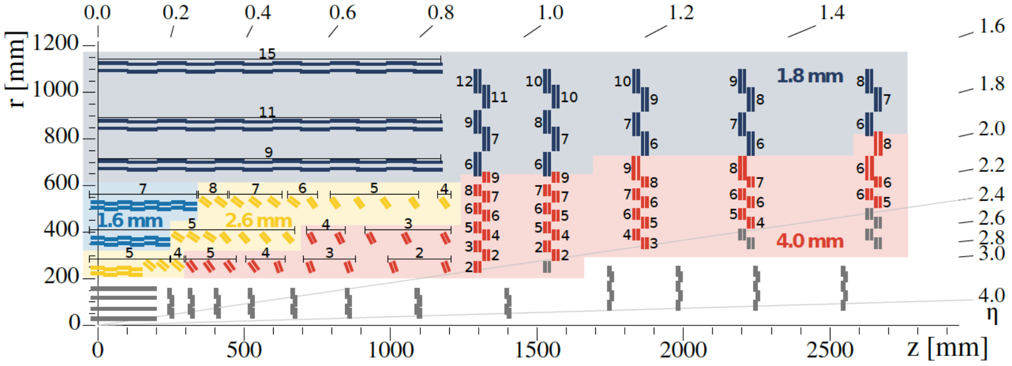
- Tilted barrel geometry fully efficient for inclined track stubs otherwise crossing top/bottom sensors in different modules






- Sensor spacing optimized in the different regions to guarantee efficient turn-on curves for stubs from pT=2 GeV tracks




*TDR layout*

- Track Finder Processor
  - end-to-end system based on Xilinx Virtex FPGA hosted on a custom ATCA board
- Track reconstruction using a *hybrid algorithm*
  - Tracklet seeds from pairs of stubs in pairs of layers + beamspot
  - Road search for matching stubs in the next layers and merge of duplicate tracks
  - Track parameter fit of candidates based on a Kalman filter
  - Optionally used for reconstruction of displaced tracks using triplets of stubs