Science and Technology Facilities Council

HEXITEC$_{MHz}$

Spectroscopic X-ray Imaging at MHz Frame Rates – The HEXITEC$_{MHz}$ ASIC

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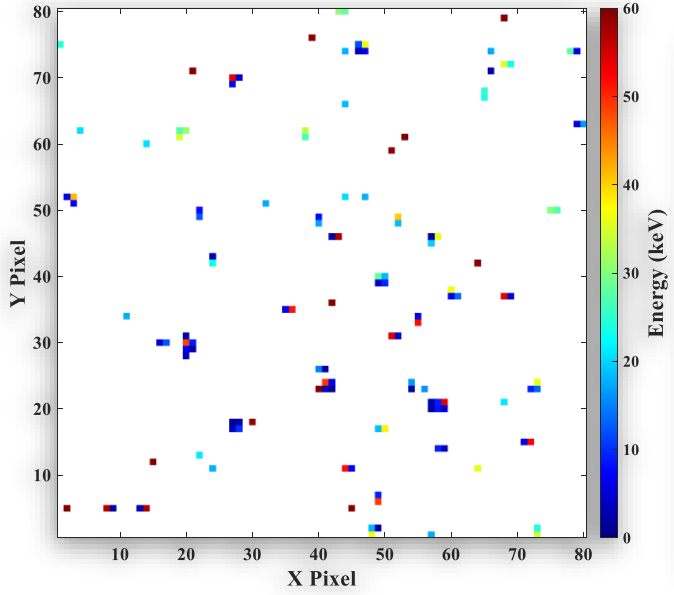
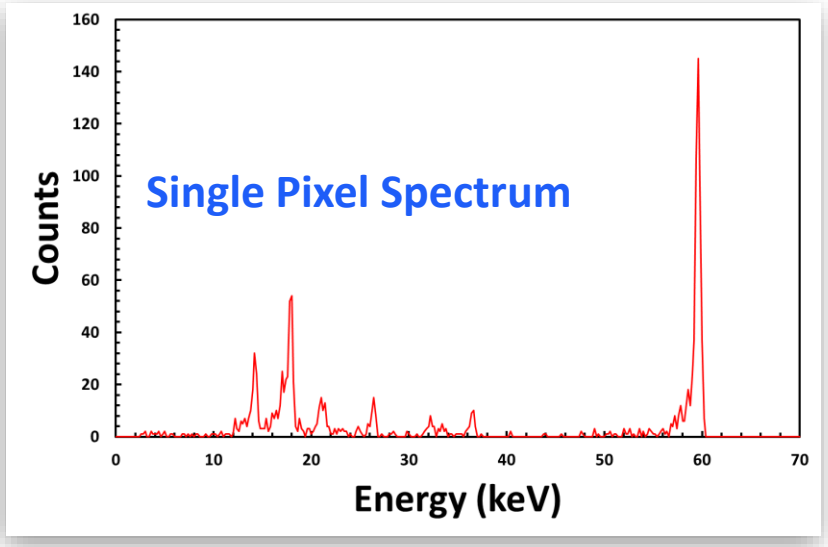
HEXITEX ASIC

HEXITEC ASIC

- 80 x 80 pixelated ASIC capable of Spectroscopic X-ray imaging with CdZnTe or CdTe detectors
- Energy values histogrammed for each pixel across many frames
- Rolling Shutter
- Analogue Readout
- Digitisation in DAQ
- Delivered in 2014 on a 0.35µm process

Parameter	Value
Pixel Pitch (µm)	250
Array Size	80 × 80
Max Frame Rate (kHz)	9.3
High Gain (keV)	2 – 200
Low Gain (keV)	6 – 600
$FWHM_{@100keV}$ (keV)	< 1

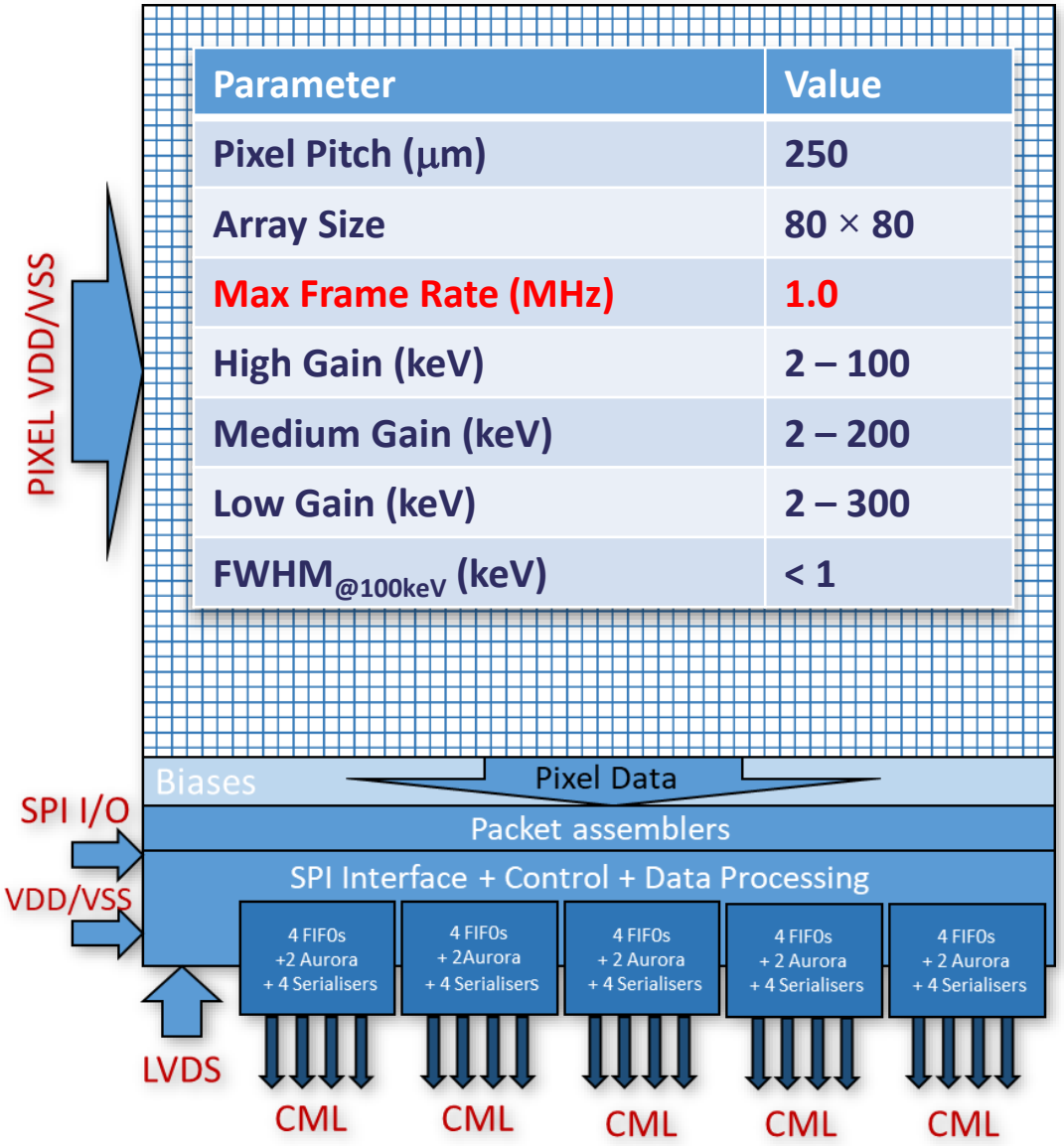




Uses in: X-ray fluorescence, Transmission Imaging, Compton Imaging

HEXITEC$_{MHz}$ ASIC

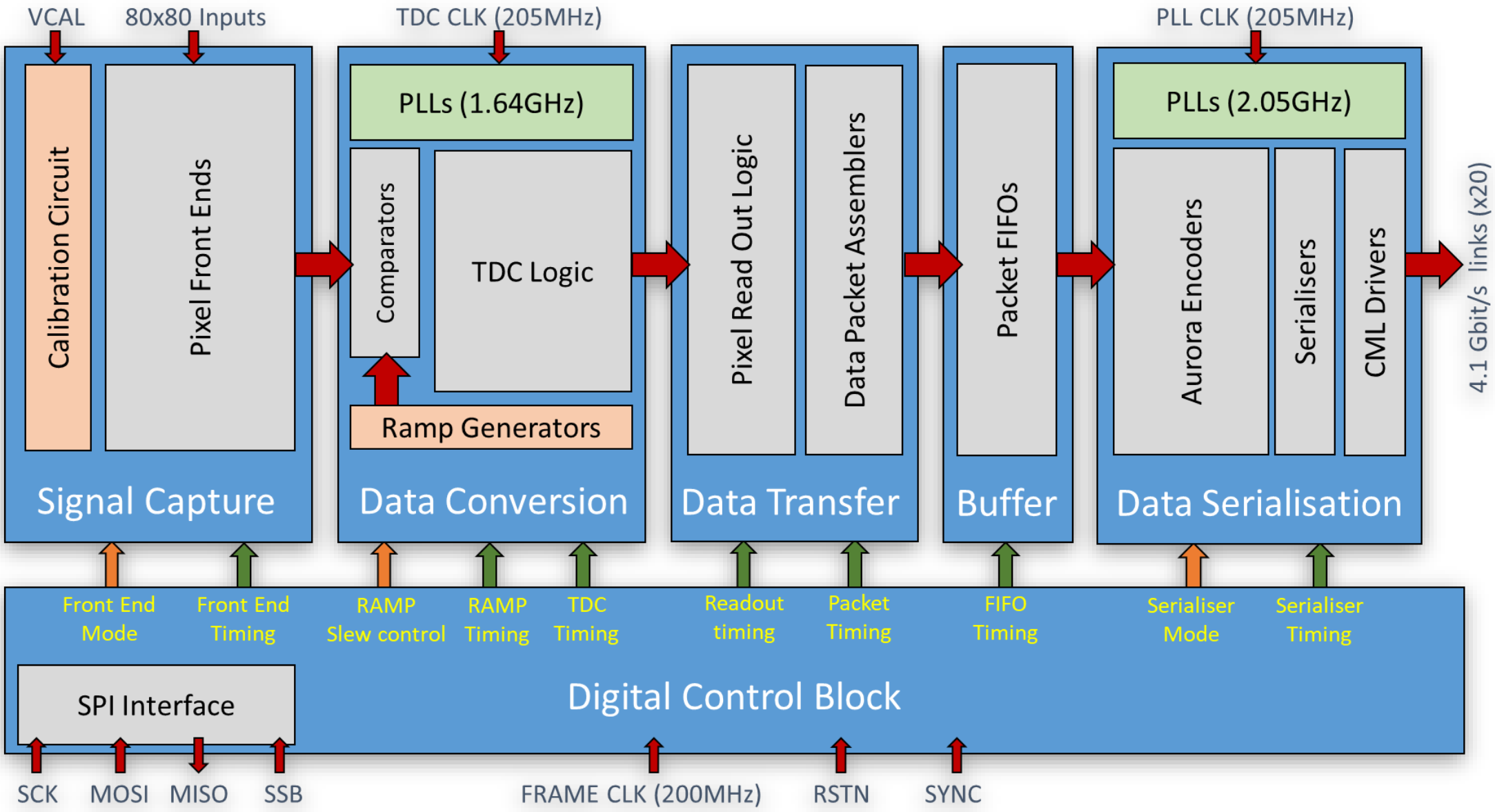
Parameter	Value
Pixel Pitch (μm)	250
Array Size	80 × 80
Max Frame Rate (MHz)	1.0
High Gain (keV)	2 – 100
Medium Gain (keV)	2 – 200
Low Gain (keV)	2 – 300
FWHM$_{@100keV}$ (keV)	< 1



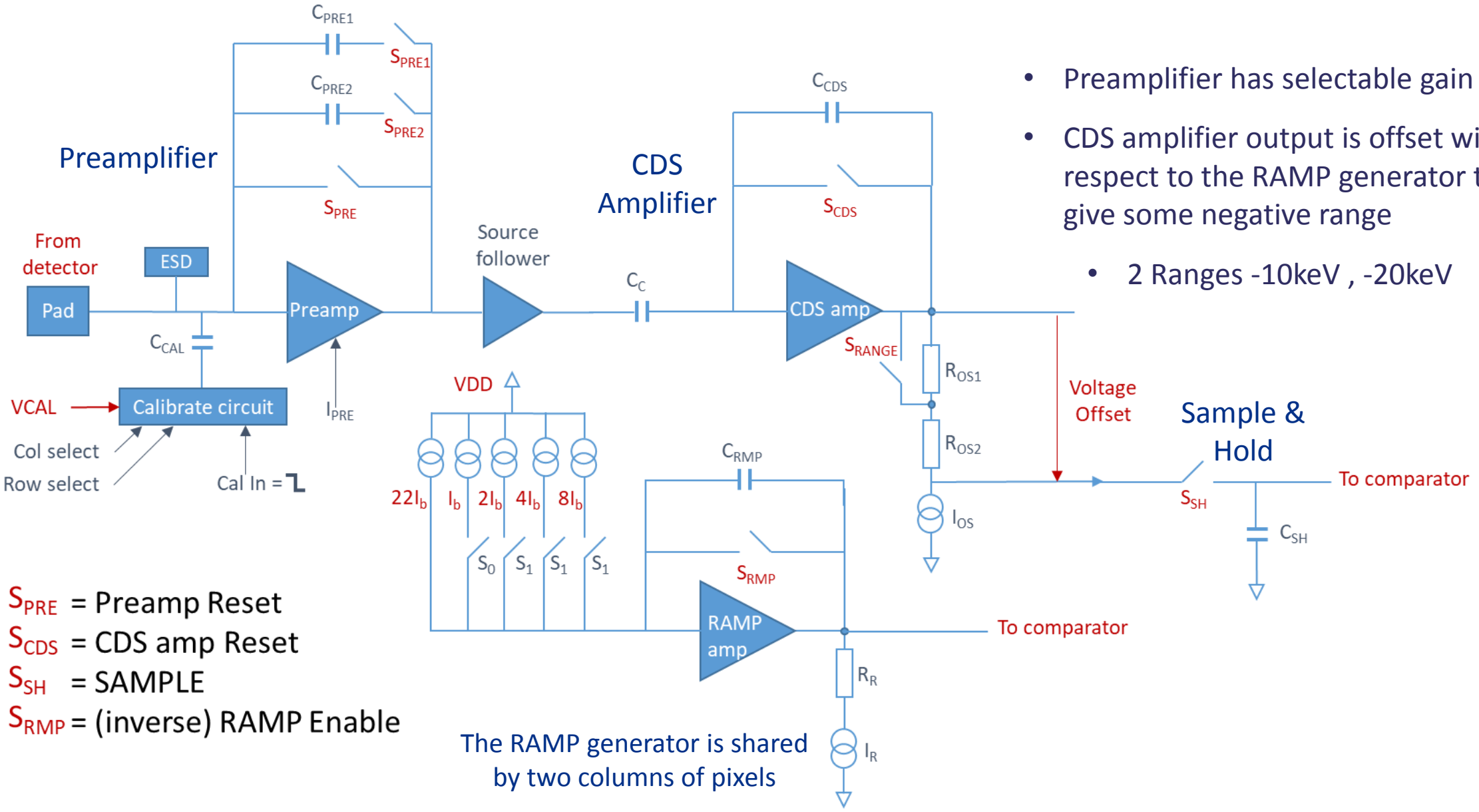
- The HEXITEC ASIC has been used in many applications such as synchrotron based X-ray fluorescence imaging and laboratory based spectroscopic imaging
- X-ray light sources are upgrading to have higher luminosity and consequently higher data rates
- HEXITEC$_{MHz}$ can meet this demand with a 1MHz frame rate increasing the count rate by two orders of magnitude
- This will enable new applications in spectral transmission imaging and high speed hard X-ray spectroscopy

- On-chip digitisation
- 20 x 4.1Gbit/s serialisers for 12-bit data per pixel
- Up to 1MHz continuous frame rate
- <1keV FWHM @ 2-200 keV gain range
- 2-side buttable
- Operate synchronously or asynchronously to a beam
- Presently under manufacture on a 180nm process

Block Diagram



Front End

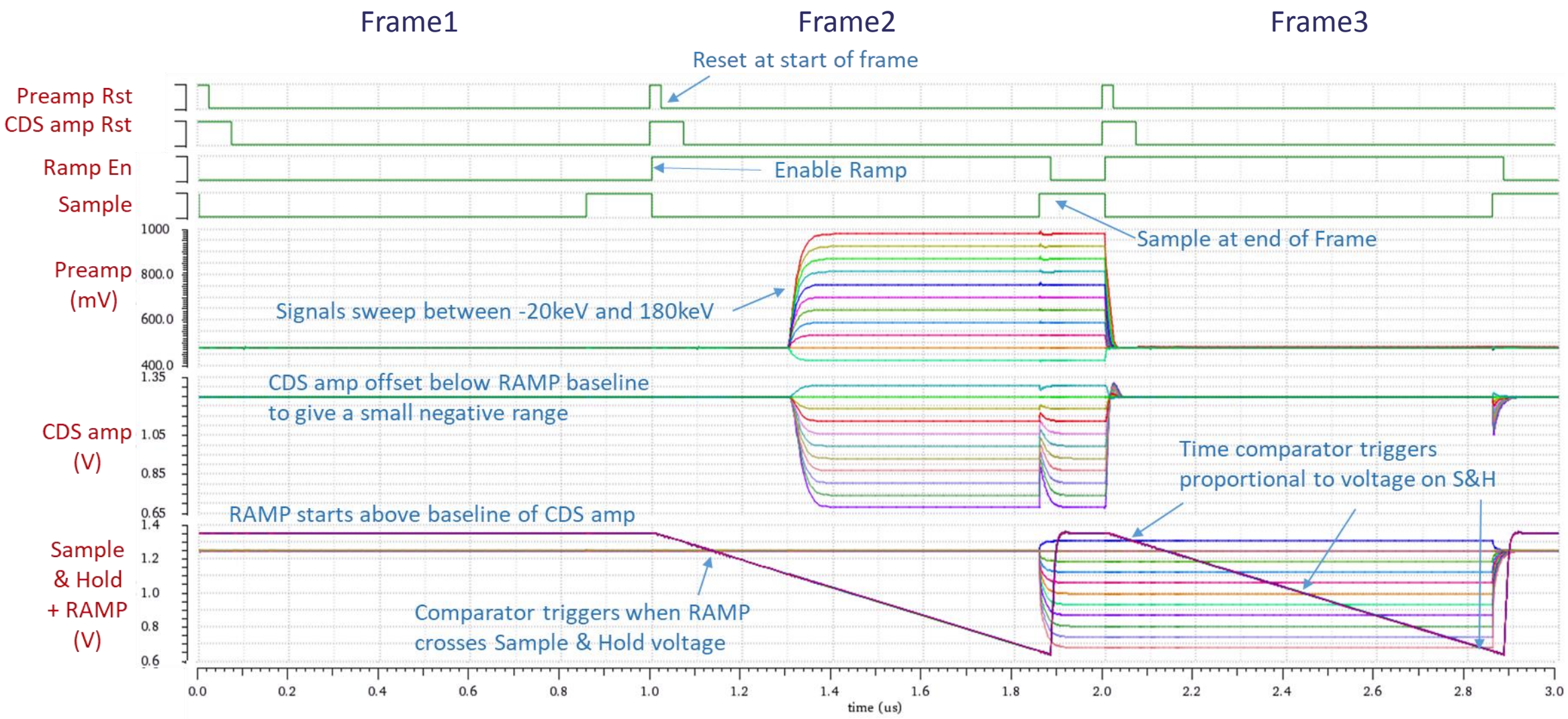


- Preamplifier has selectable gain
- CDS amplifier output is offset with respect to the RAMP generator to give some negative range
  - 2 Ranges -10keV , -20keV

S_{PRE} = Preamp Reset
S_{CDS} = CDS amp Reset
S_{SH} = SAMPLE
S_{RMP} = (inverse) RAMP Enable

The RAMP generator is shared by two columns of pixels

Front End Timing

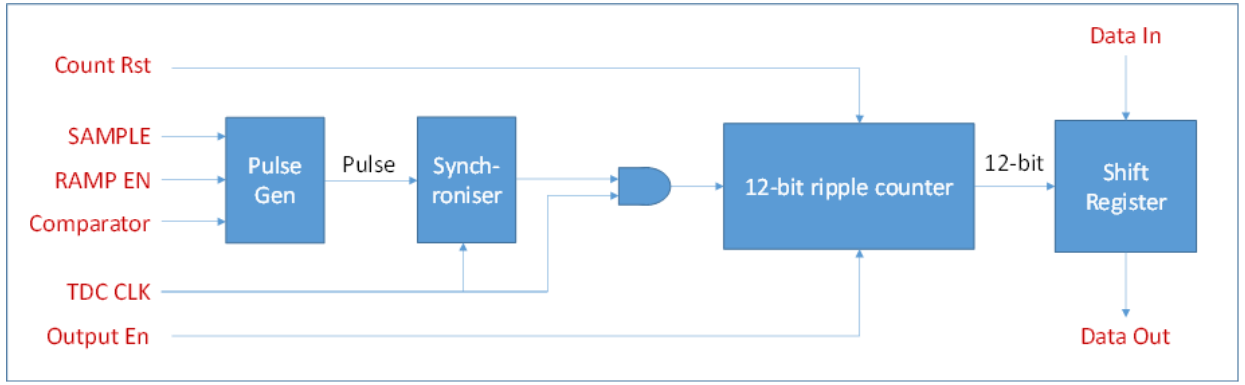


Can sense small negative signals which can induced by charge in neighbouring pixels
This can be used to increase the spatial and spectroscopic resolution

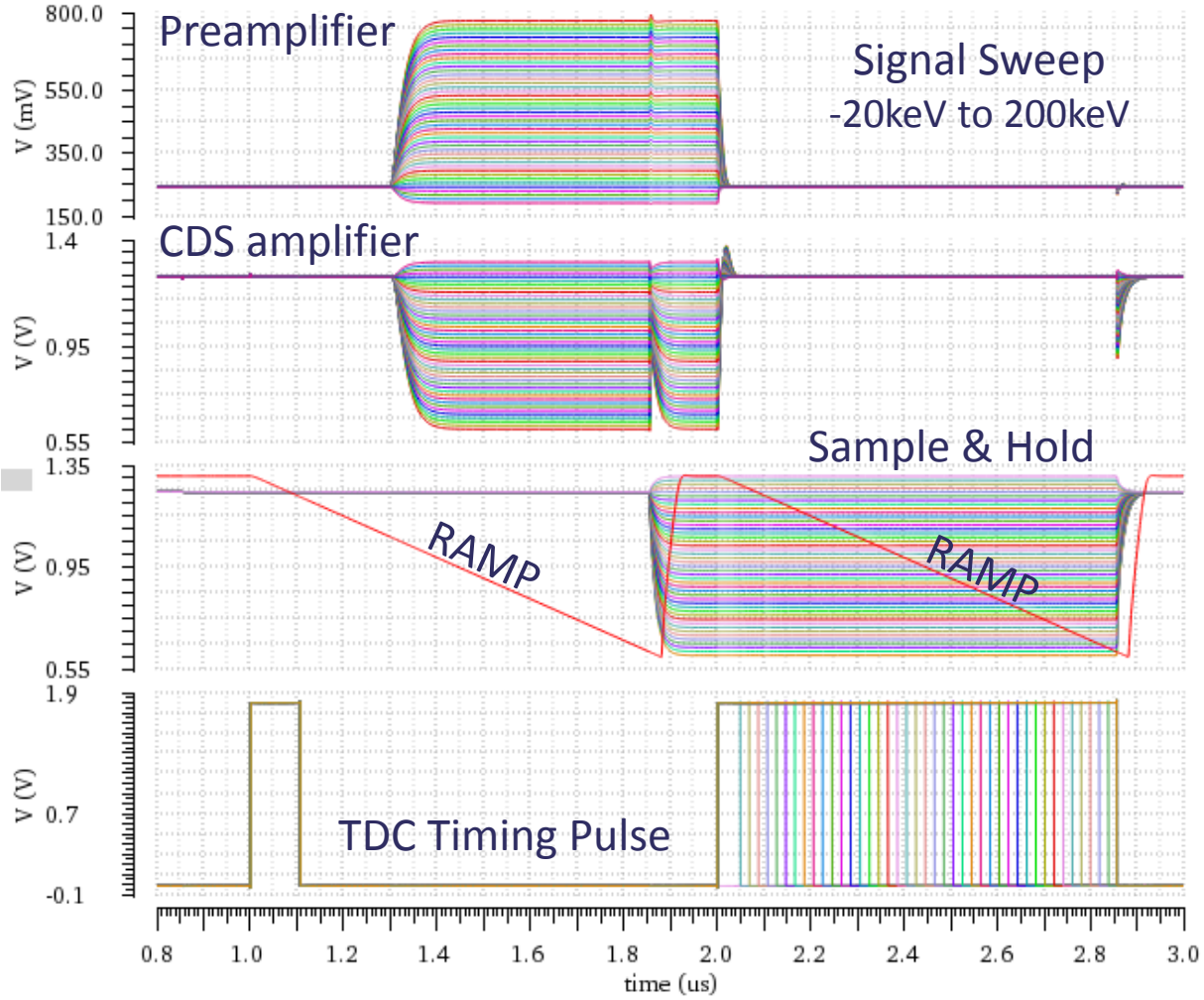
TDC Conversion

- TDC (Time to Digital Convertor) converts the Sample & Hold voltage into a 12-bit digital value
- Sample & Hold and RAMP outputs form the inputs to a comparator
- Comparator triggers when these voltages are equal
- Generate a pulse that goes high at start of the RAMP and goes low when comparator triggers
- Pulse length is proportional to the voltage on the sample & hold
- Pulse is used to generate a clock train which clocks a 12-bit ripple counter
- Data is latched into a shift register which moves it to the bottom of the pixel array

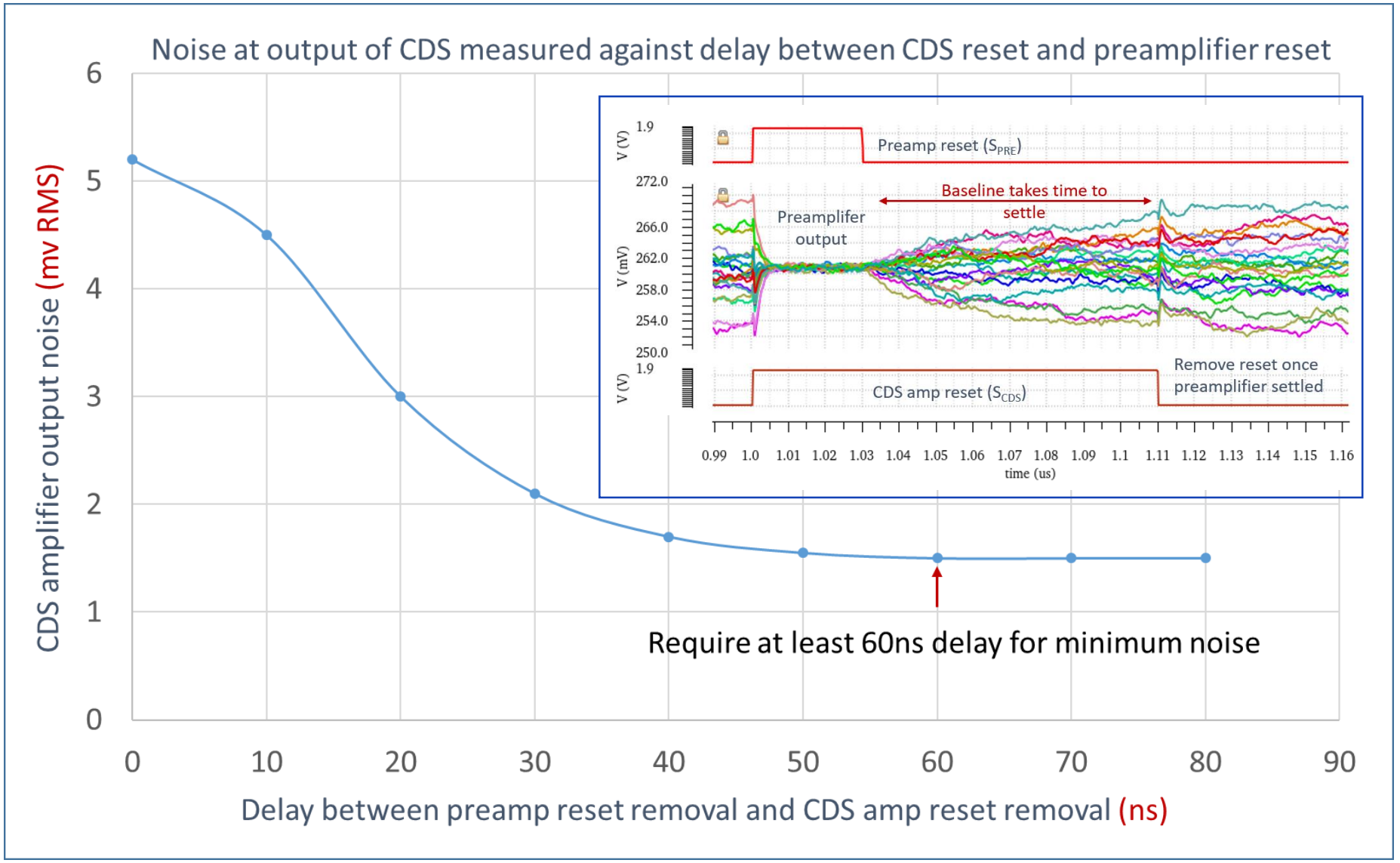
TDC logic block diagram



TDC Simulation



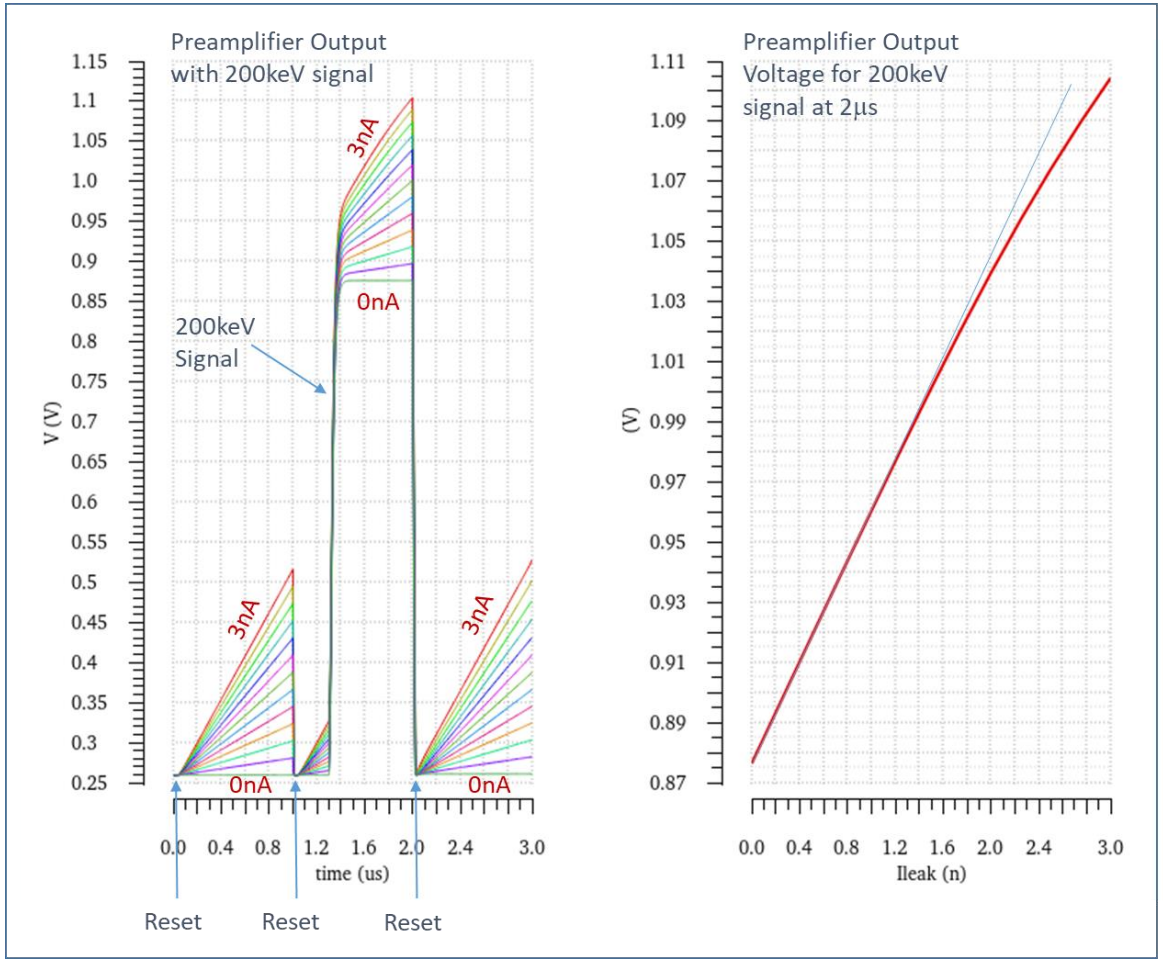
Noise due to reset timing



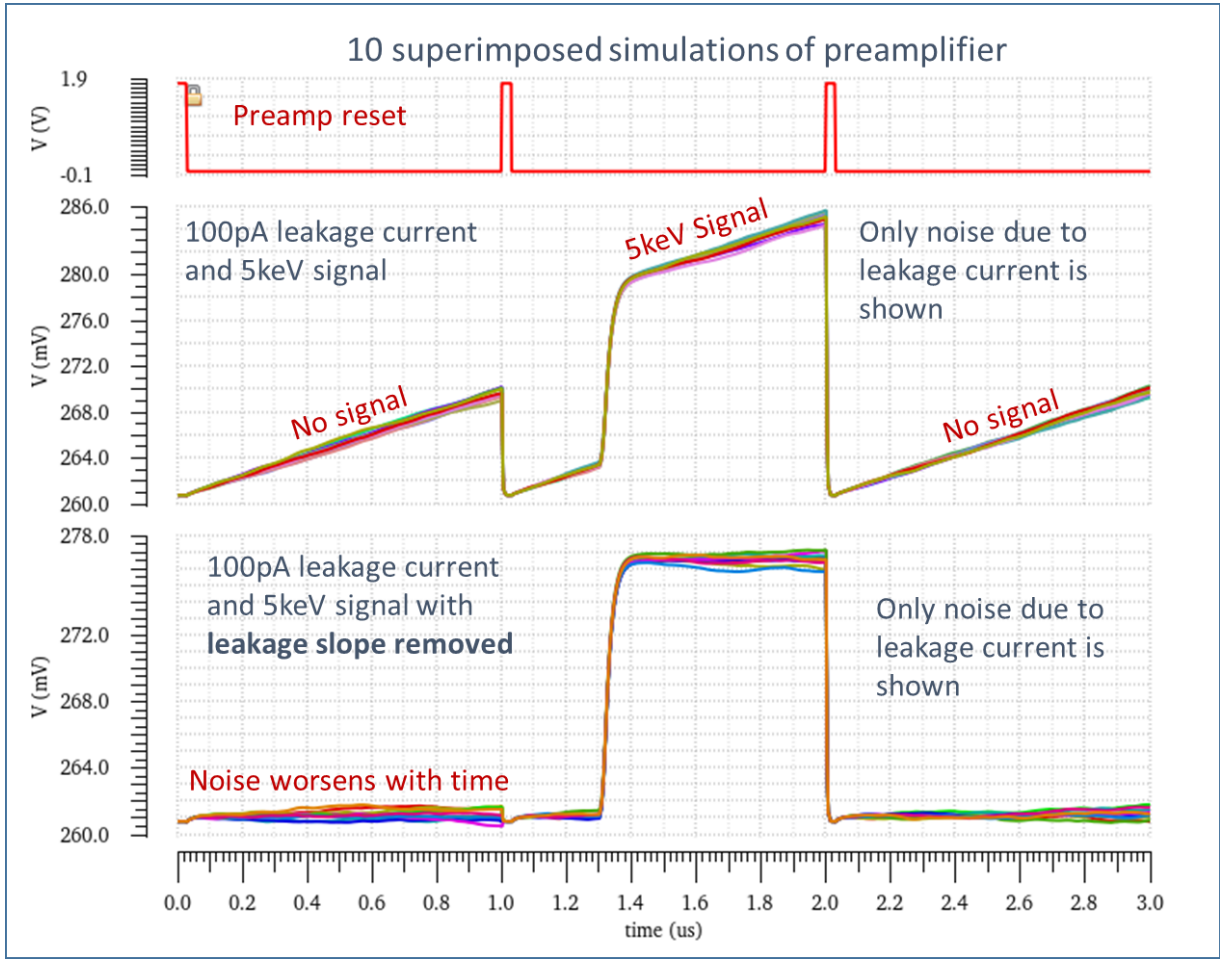
All timing signals are programmable within the frame to 5ns resolution

Effect of Leakage Current

Leakage current will have an effect on linearity above 1.5nA



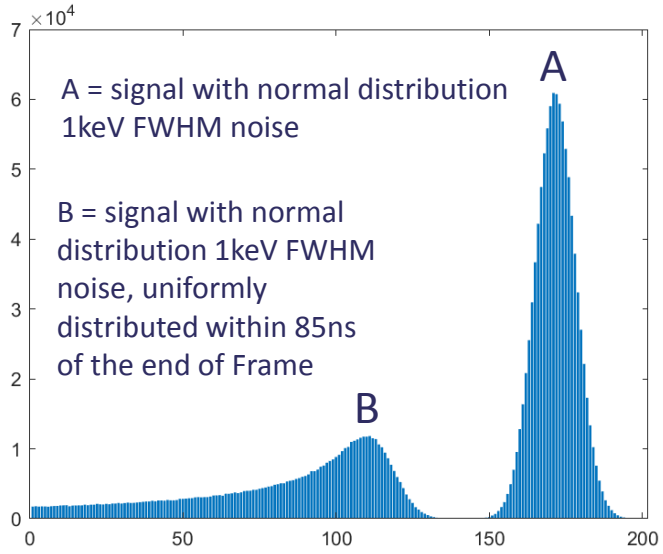
Noise increases with time with leakage current

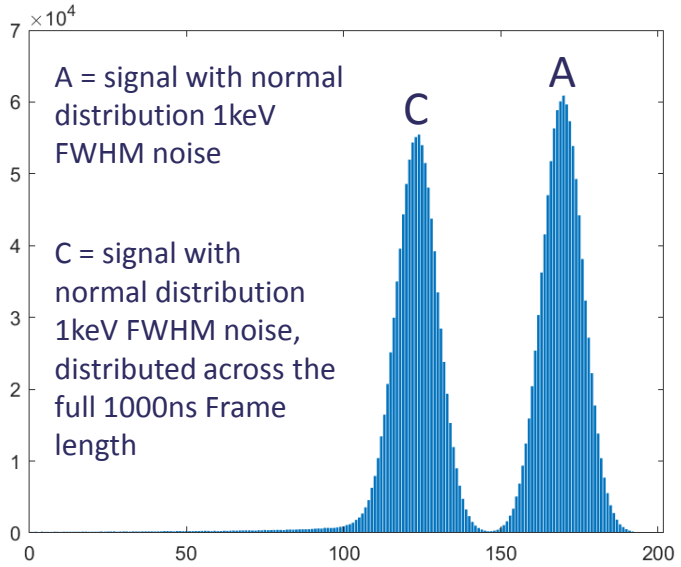


Asynchronous Mode

What happens if the signal forms near the end of the Frame?

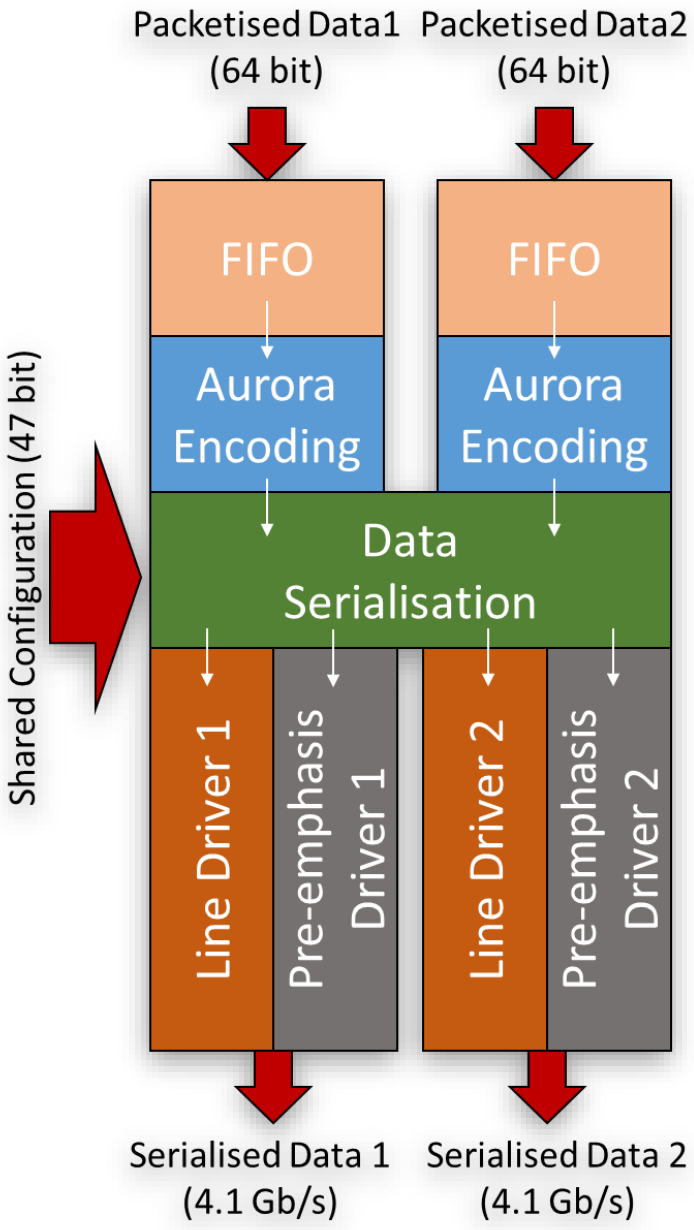
~5% of events that could be partially formed at 1MHz
MATLAB Simulations (B &C) shifted down in energy on plot):



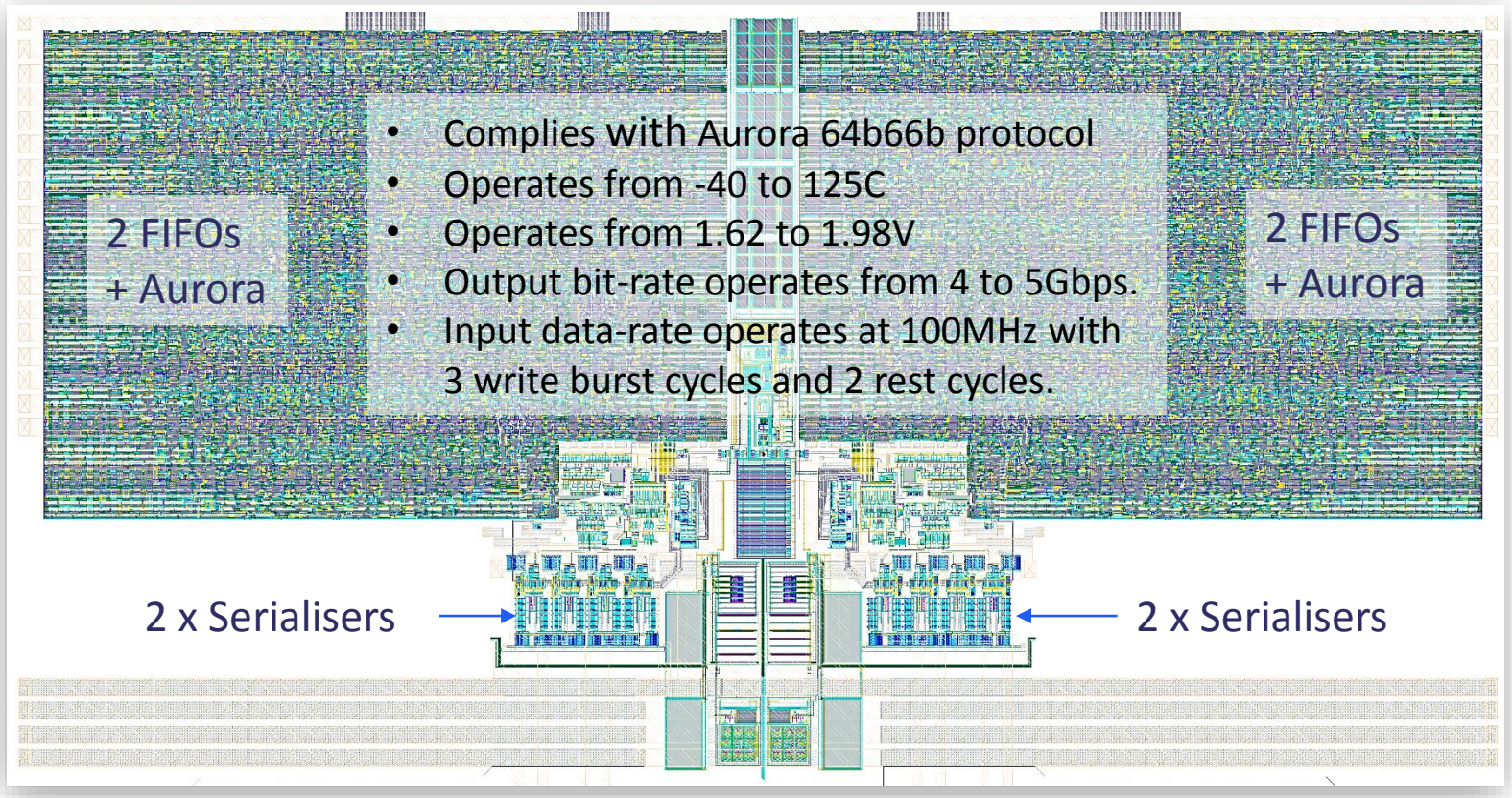


- Minimal effect when signal occurrence is distributed across the whole 1000ns frame.
- Slightly extended on the lower energy side but no significant affect on the noise measured
- No mitigating circuitry or mode of operation required
- If this effect turns out to be more significant, can use ‘long integration’ mode

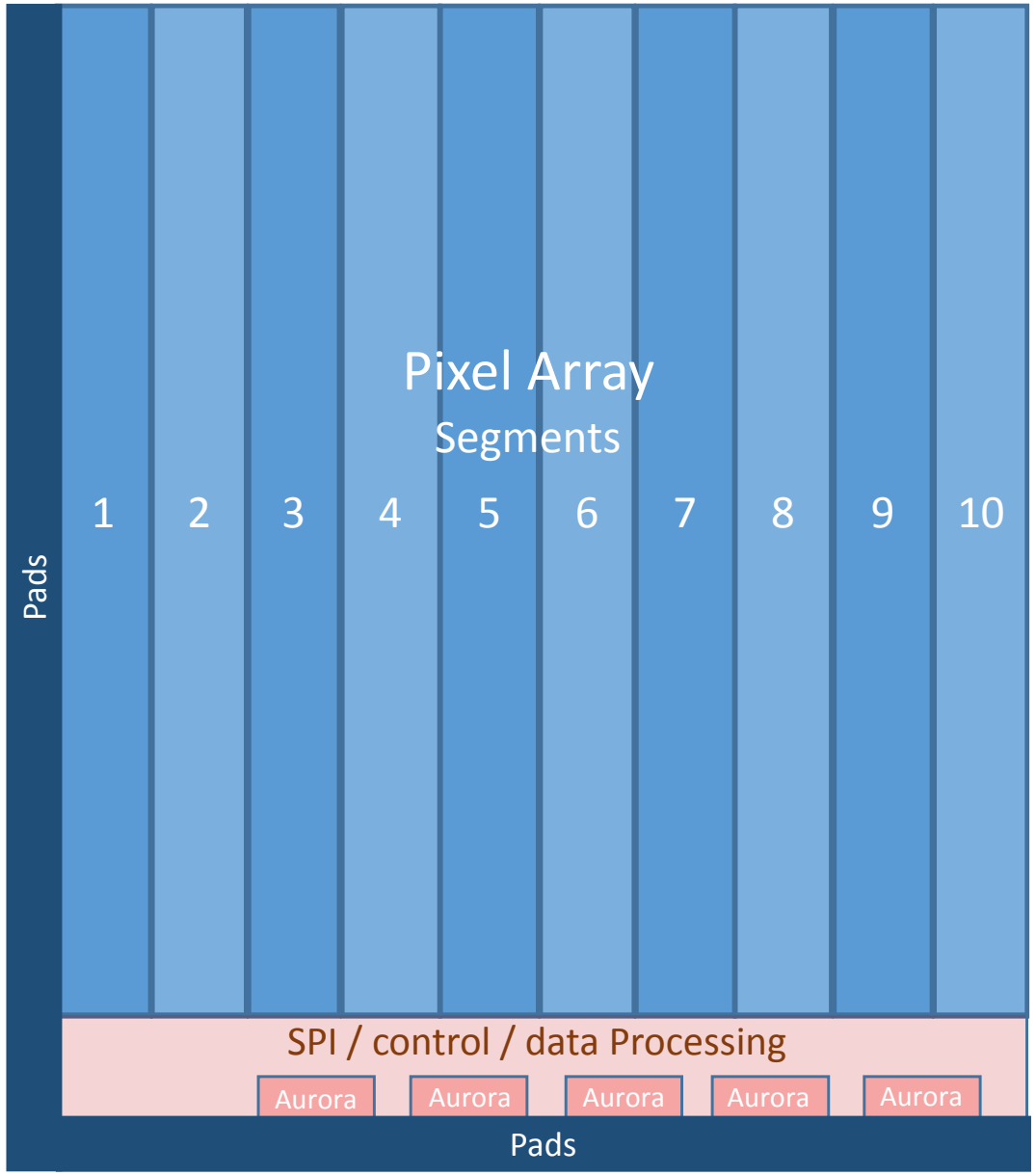
Serialiser



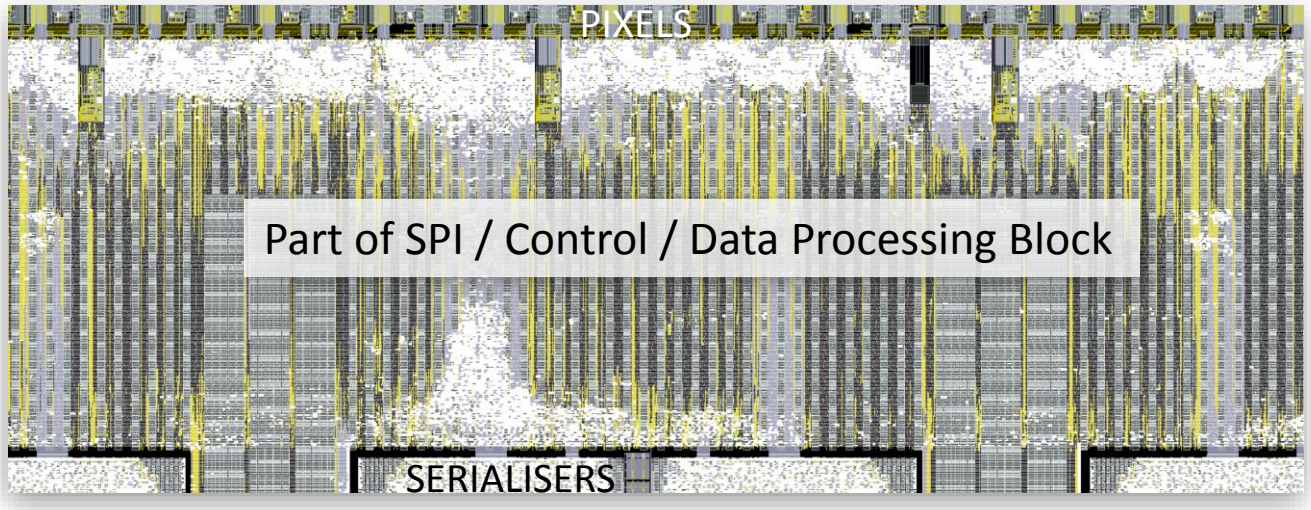
- 20 Serialisers at 4.1 Gb/s
- Aurora encoded 64b66b format
- Data serialised using CML circuitry
- Primary and pre-emphasis line drivers transmit data off-chip
- Configurable using 47-bit register



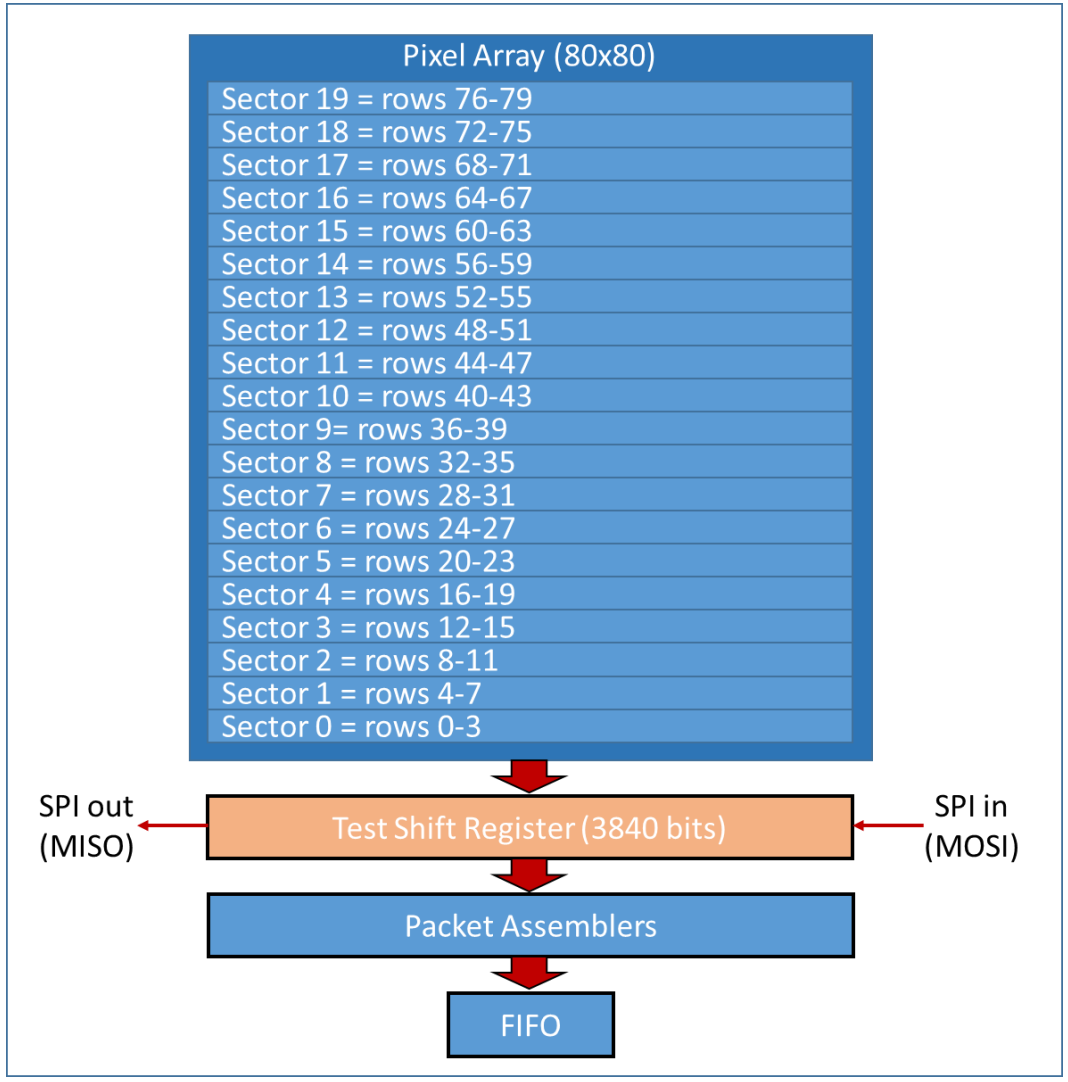
Segmentation



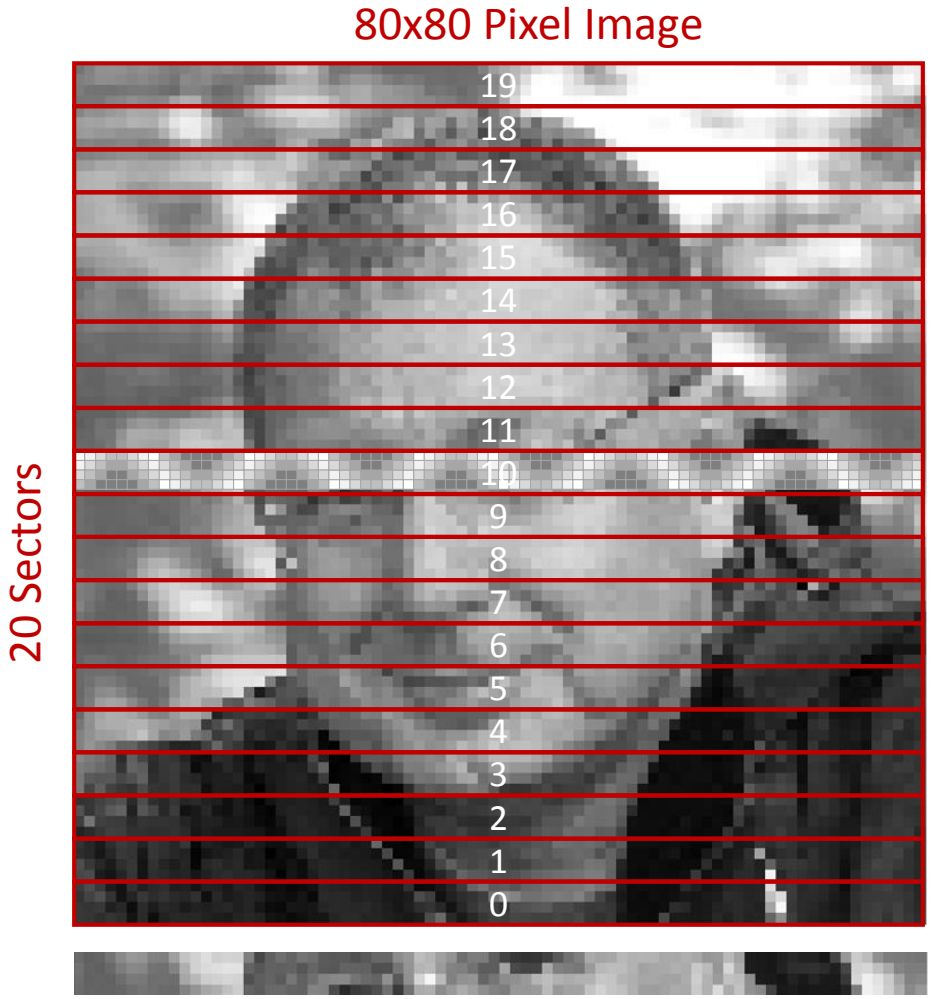
- Global or local control of the ASIC
- 10 ASIC Segments
  - Each segment can be individually controlled
  - 2 serialiser outputs per segment
- Control done through the SPI interface
- Programmable Control Signal Timing
  - Control signal timing can be programmed to 5ns resolution through the SPI interface



Test Feature

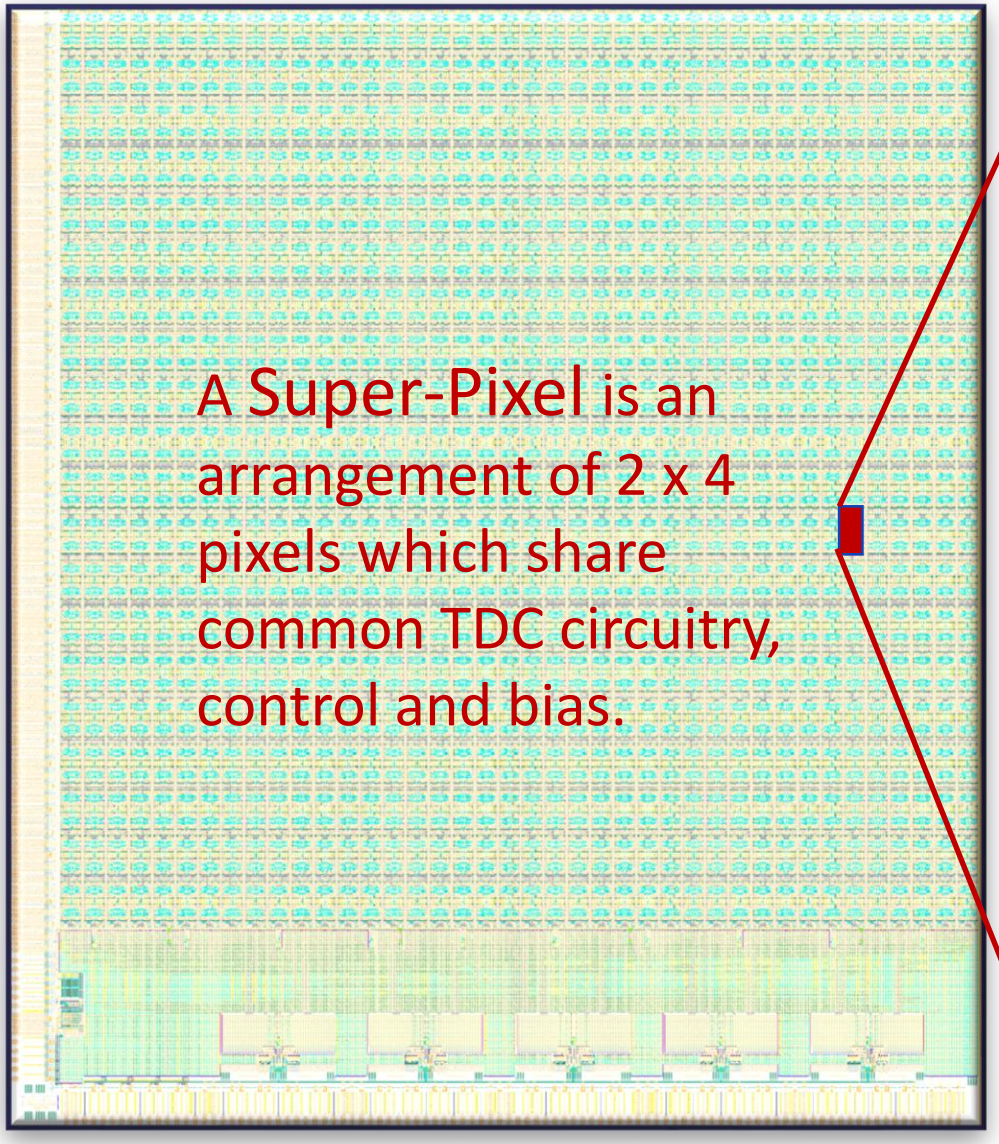


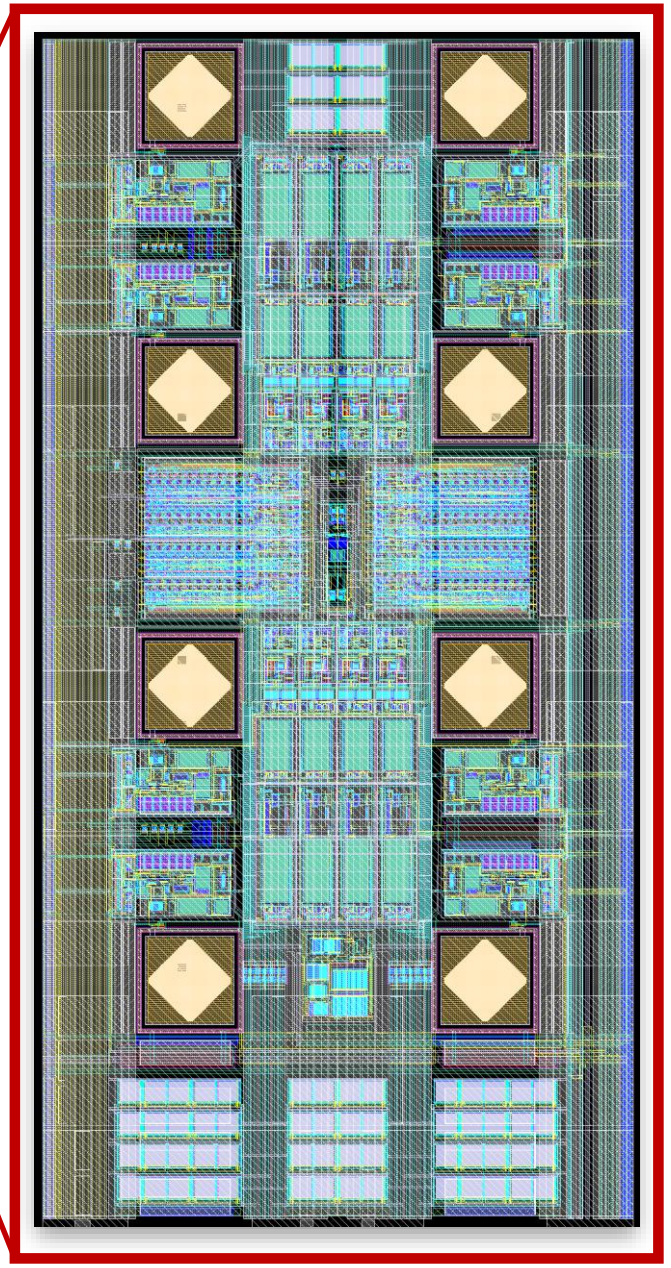
Overwrite part of an image with data in the shift register
Capture part of an image and read out through the shift register

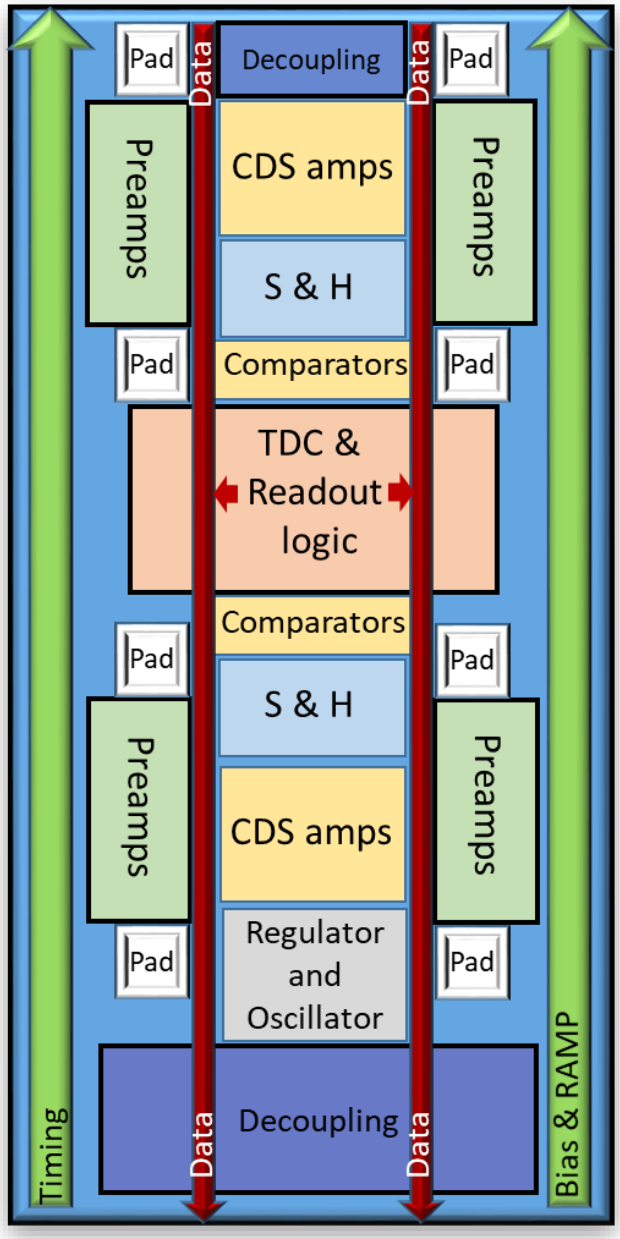


In addition the front end can be bypassed and a DC voltage can be applied directly to the TDC

Super-Pixel


24.3mm
21.1mm
A Super-Pixel is an arrangement of 2 x 4 pixels which share common TDC circuitry, control and bias.




Pad
Data
Decoupling
Data
Pad
Preamps
CDS amps
Preamps
S & H
Pad
Comparators
Pad
TDC &
Readout
logic
Comparators
Pad
S & H
Pad
Preamps
CDS amps
Preamps
Regulator
and
Oscillator
Pad
Pad
Timing
Data
Decoupling
Data
Bias & RAMP

Full Chip Simulation

Original Image
Black = 0keV
White ~ 200keV
Signal = Current pulse

Decoded Serial Data
Black = Decimal code 0
White = Decimal code 4095

Full chip simulation

System Verilog
VerilogA
VerilogAMS
Synthesised digital circuitry with full SDF back-annotated delays.

Apply current pulse stimuli to all pixels

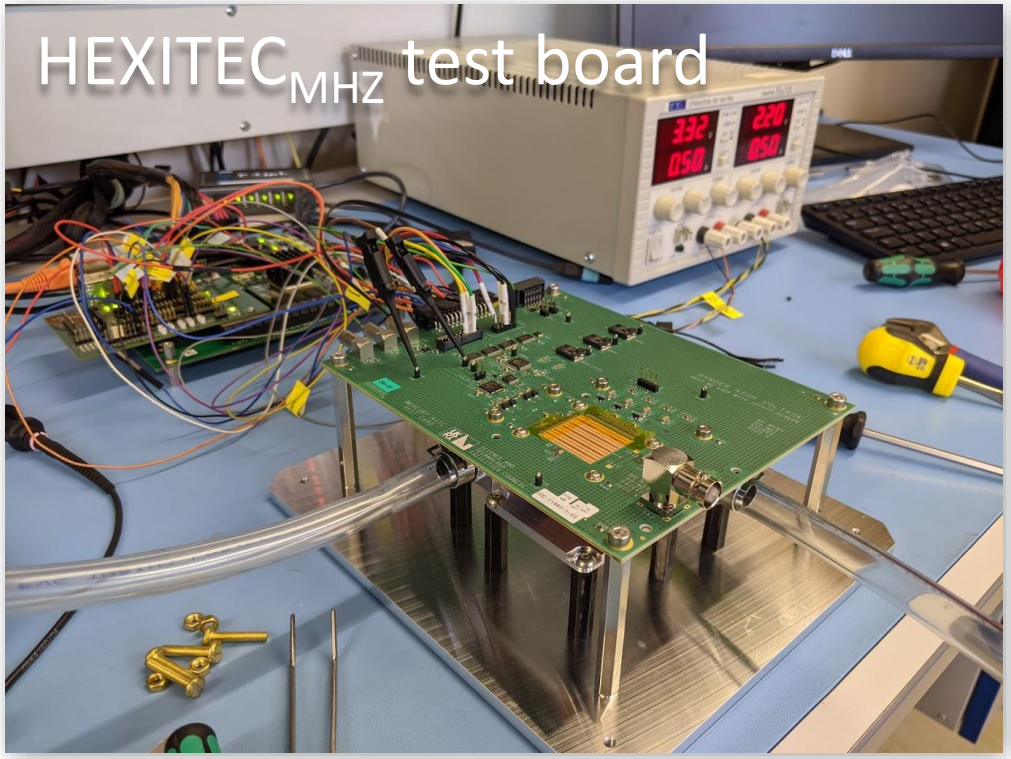
Decode data from all 20 serialisers

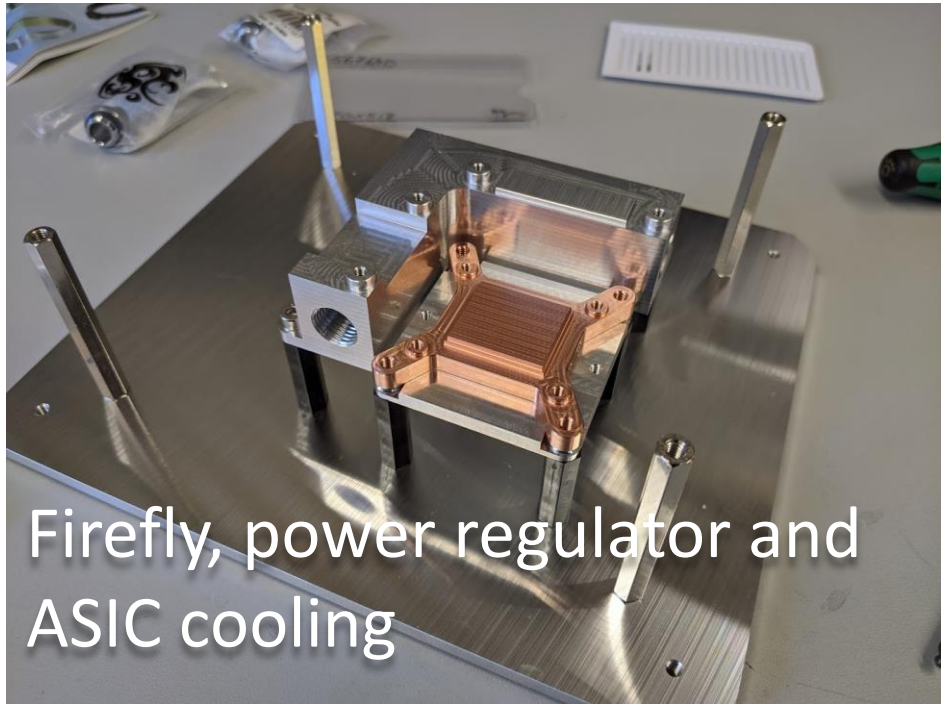
Reassemble image

The frontend output dynamic range does not fully cover the input dynamic range of the TDC hence there is less contrast

Status

- There were delays getting the ASIC into FAB
- Now being manufactured and is expected October 2021
- DAQ firmware / software developments are almost done
- Mechanics delivered and tested
- Ready to begin testing when the ASICs return





Thank you

email: lawrence.jones@stfc.ac.uk

HEXITEC$_{MHz}$ Features	Value
Pixel Pitch (μm)	250
Array Size	80 × 80
Buttability (sides)	2
Max Frame Rate (MHz)	1.0
High Gain (keV)	2 – 100
Medium Gain (keV)	2 – 200
Low Gain (keV)	2 – 300
FWHM$_{@100keV}$ (keV)	< 1
Data rate / serialiser (Mbits/s)	4.1

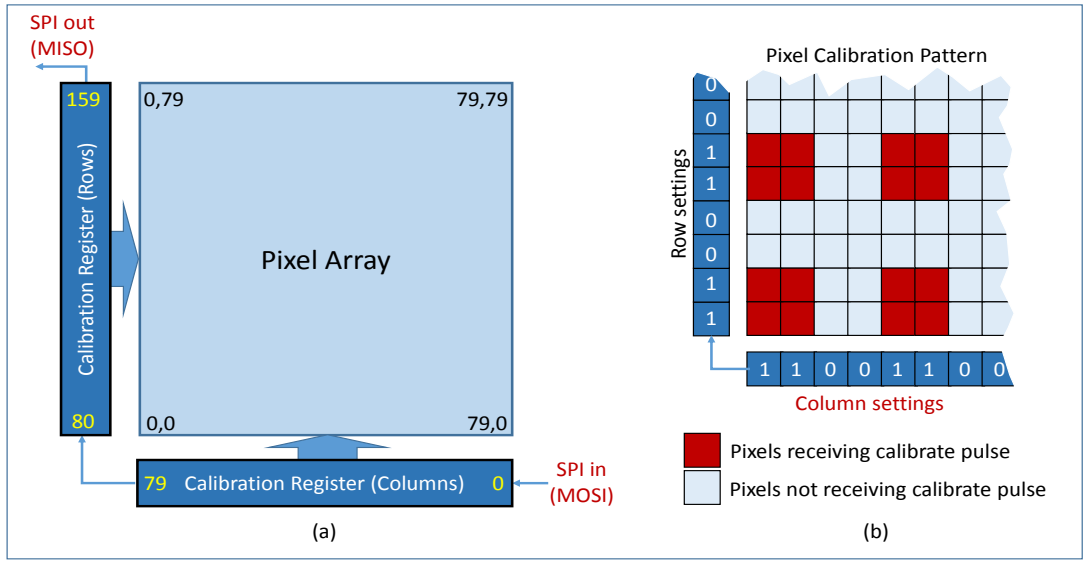
HEXITEC$_{MHz}$ Features	Value
Total data rate (Mbits/s)	82
TDC resolution (bits)	12
ASIC Segmentation (regions)	10
Integration Time (frames)	1 – 255
Frame Length (μs)	1.0 – 1.275
Control Timing Resolution (ns)	5
Power Supply (V)	1.8
Power Consumption (W)	12 – 15
Power Density (mW / mm^2)	23-29

Extra Slides

Why 250μm pitch?

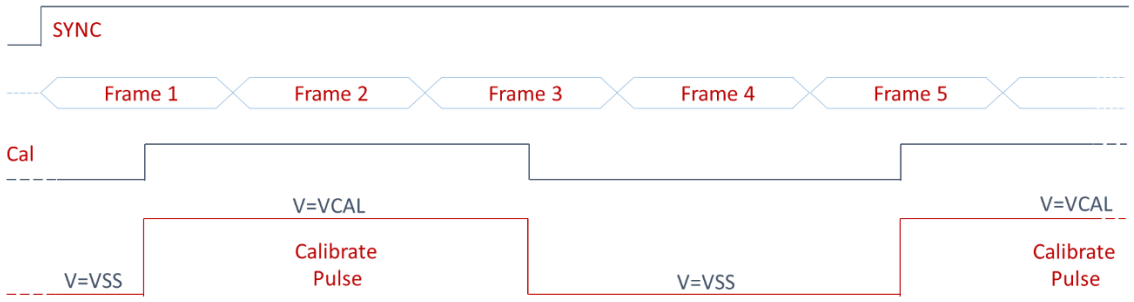
- The amount of charge sharing gets worse with small pixels
- With 250μm pixels we get ~40-50% of events sharing charge (depending on energy and detector thickness)
- HEXITEC can handle this and get good spectra
- We also have a bonding process for it and CdTe and CdZnTe
- We will use 1mm CdTe and 2mm CdZnTe, some 0.5mm GaAs and try out p-type Si on HEXITEC$_{MHz}$

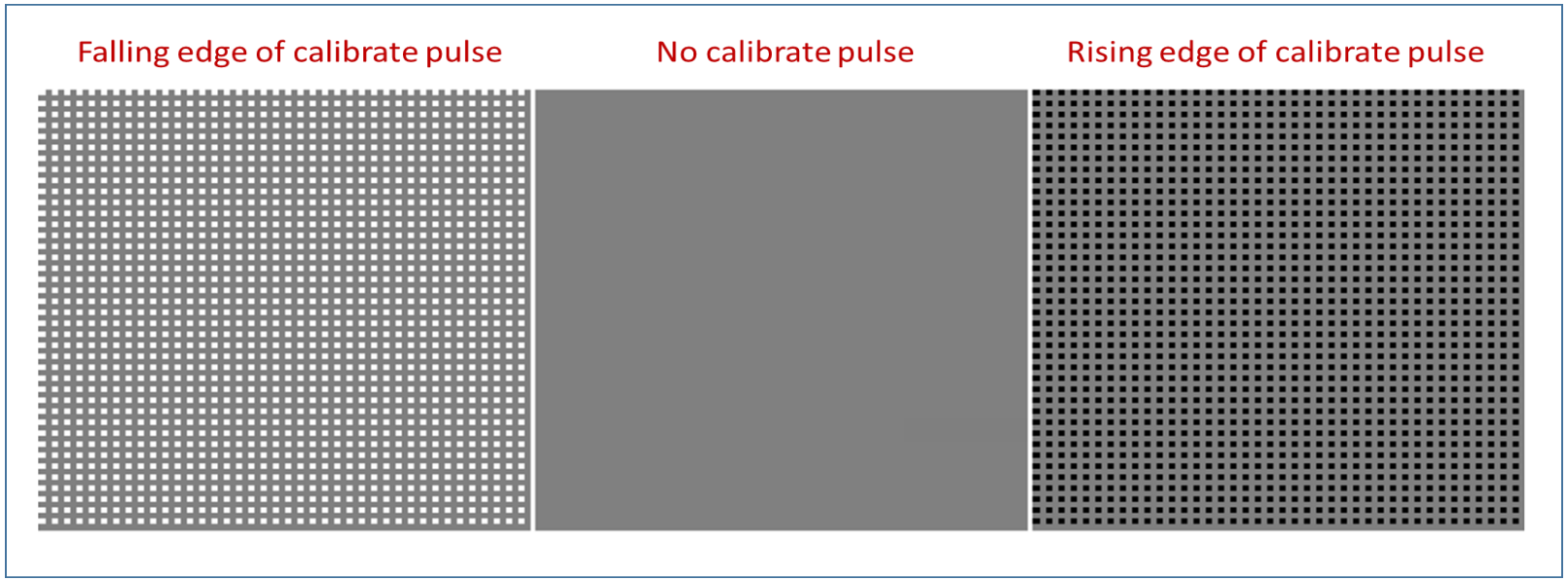
Test Pulse Circuit



80x80 Pixel Image

Calibration Timing



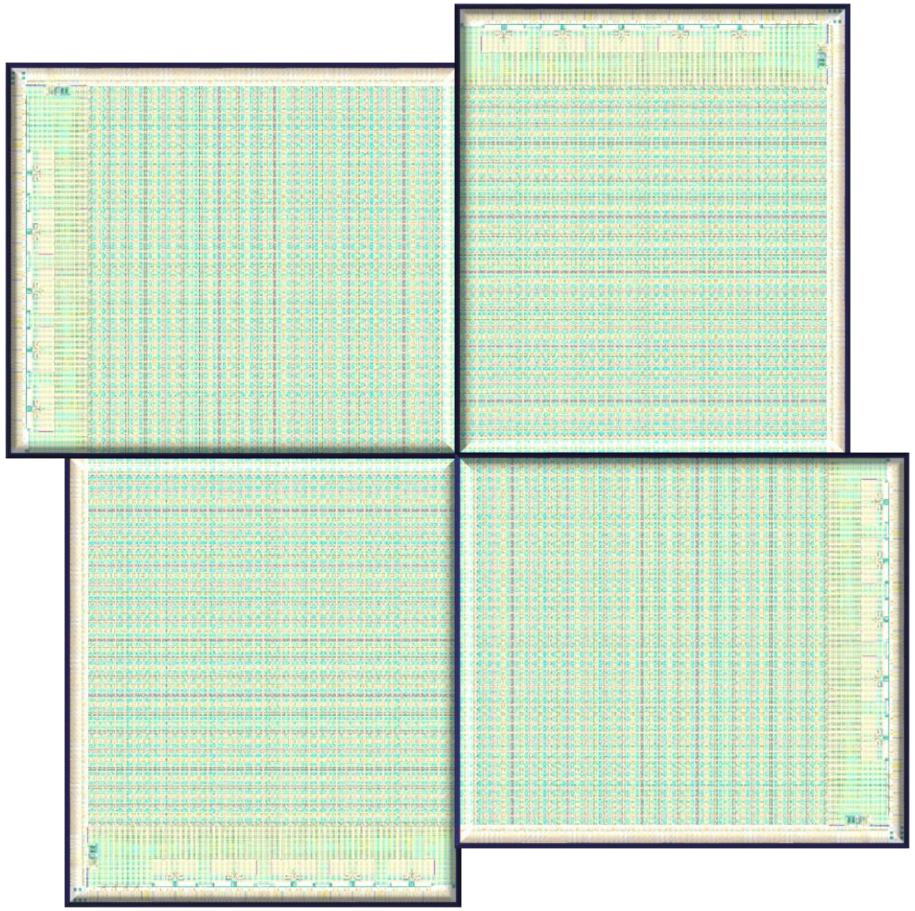


Positive image

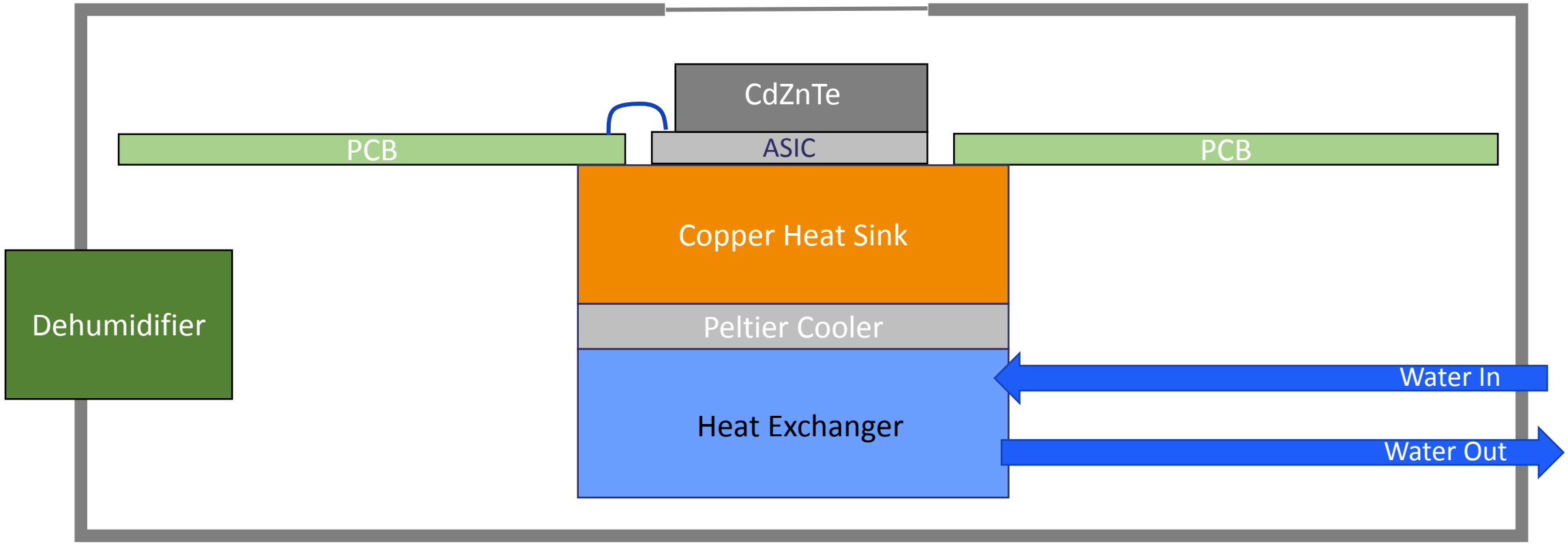
Baseline image

Negative Image

2-side buttable

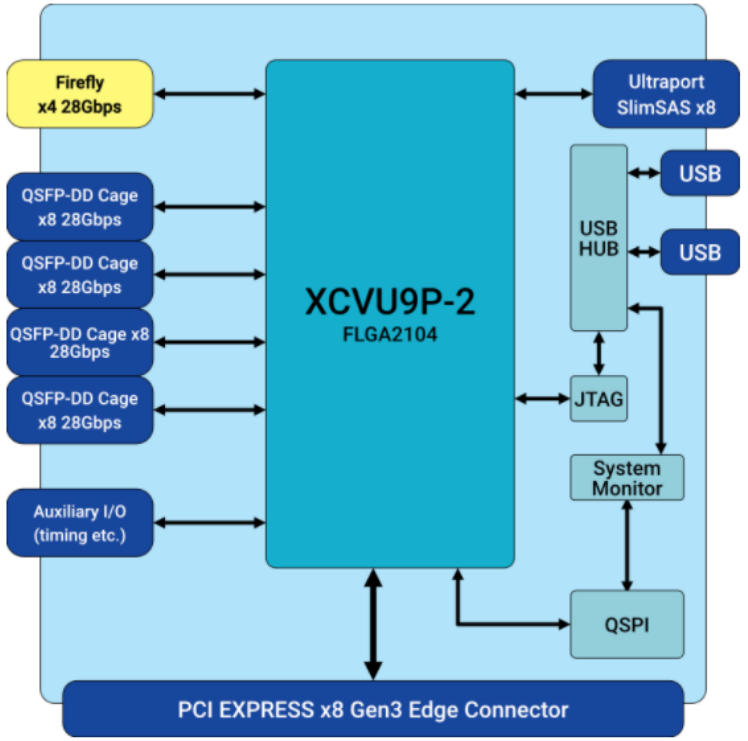


Cooling System



DAQ hardware

ADM-PCIE-9V5



Main Functions:

Decode Aurora 64/66b

Assemble frames

Gear up data rate and output on 100 GbE

SAMTEC Firefly modules on board

Alpha Data: ADM-PCIE-9V5:

Host Interface

PCI Express Gen3 x8 or OpenCAPI

Communications Interfaces

4x QSFP-DD 8x28Gbps - User Configurable, includes 10/25/40/100G Ethernet

1x Ultraport SlimSAS 8x25Gbps - OpenCAPI

1x Firefly 4x28Gbps - User Configurable

Input/Output Interfaces

Other Interfaces

USB (front and rear sockets) board management (built-in JTAG)

Isolated PPS Timing Input