Timepix4 timestamping detector for synchrotron applications

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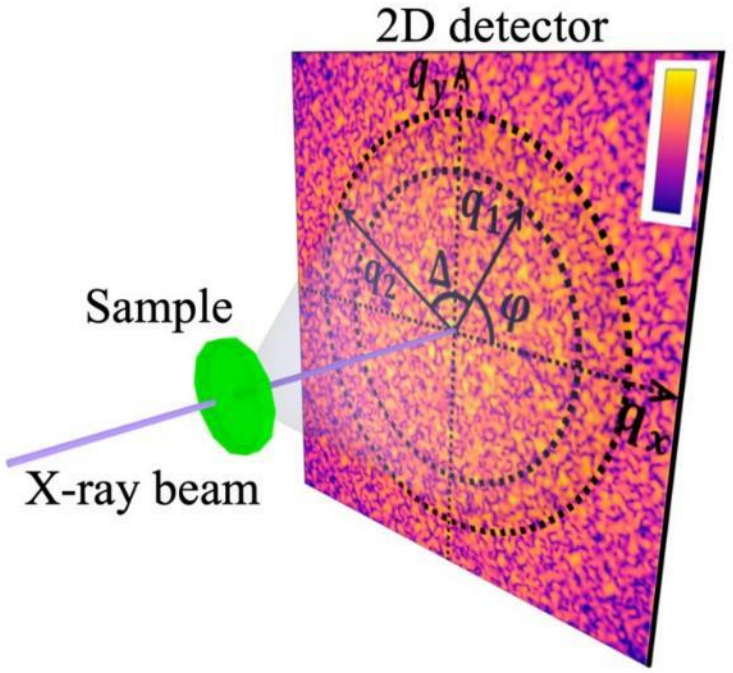
Position Sensitive Detectors 12, Birmingham, Sept 2021



HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

DESY.

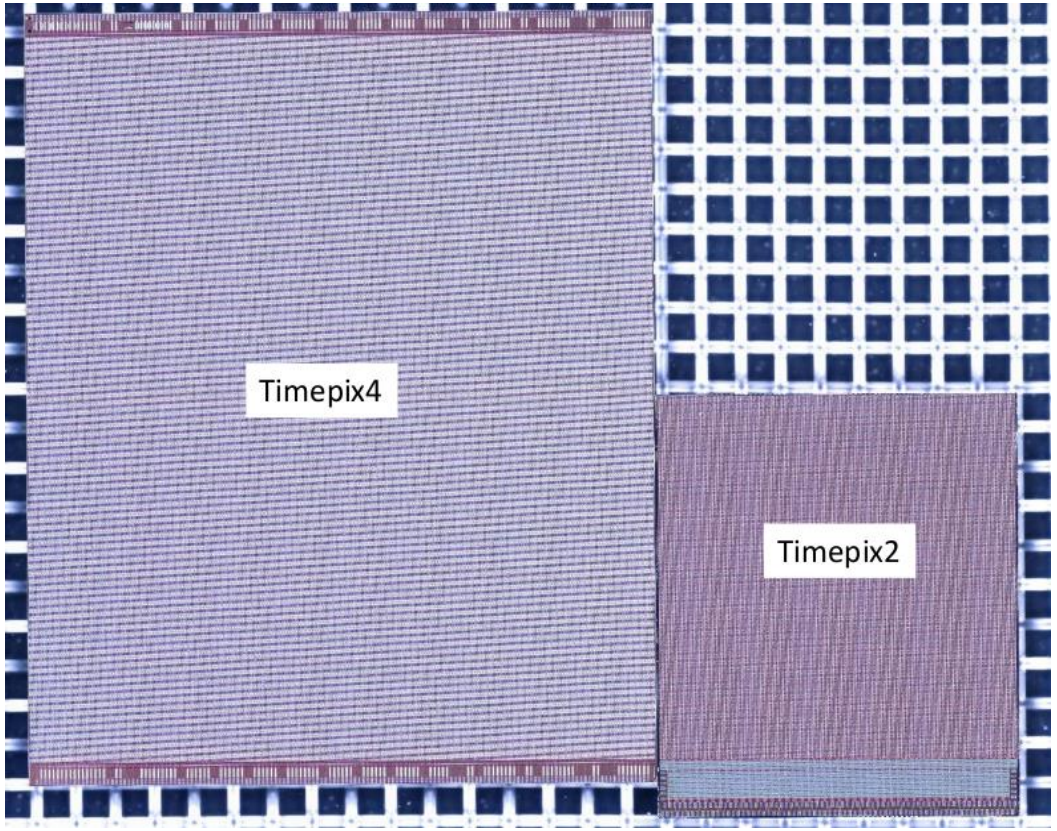
Introduction

- Timepix4 for synchrotron X-ray experiments
- Chip design and testing at CERN
- System development at DESY

Timepix4

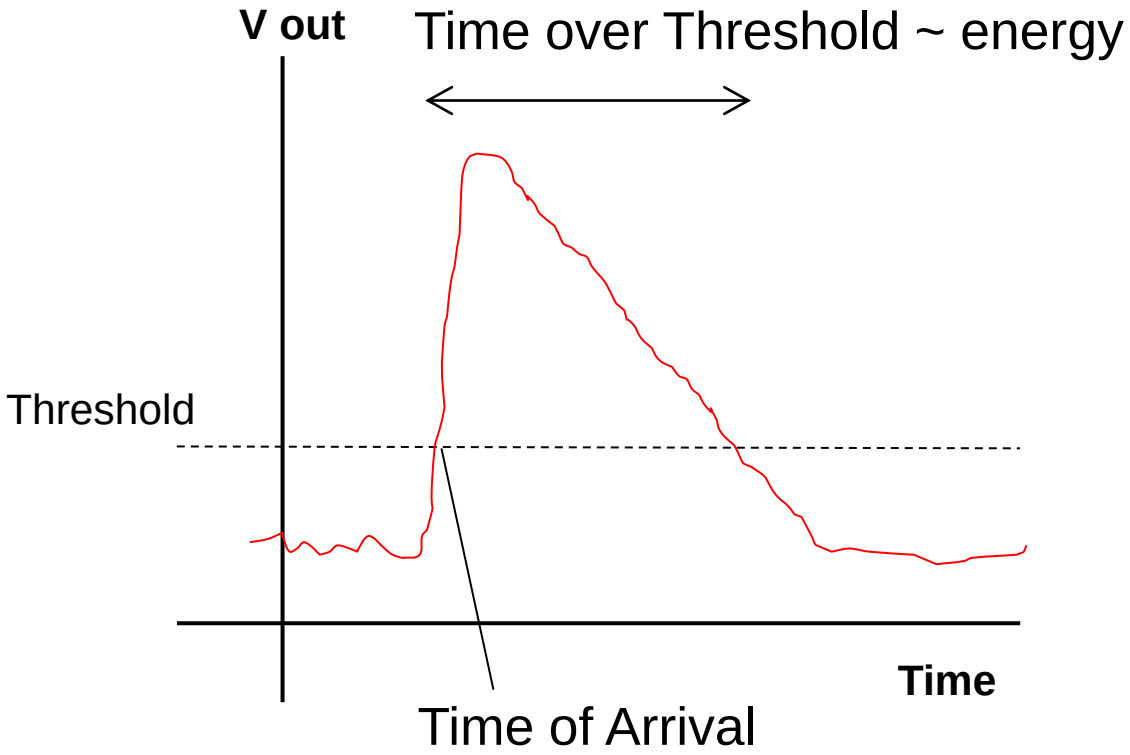
- Developed by CERN, Nikhef and IFAE for Medipix4 collaboration
  - 15 member institutes
- 65 nm TSMC process (previously 130 nm GF)
- First chips received April 2020
- Timestamping and hit counting modes of operation

55 µm pixel size
512 x 448 pixels

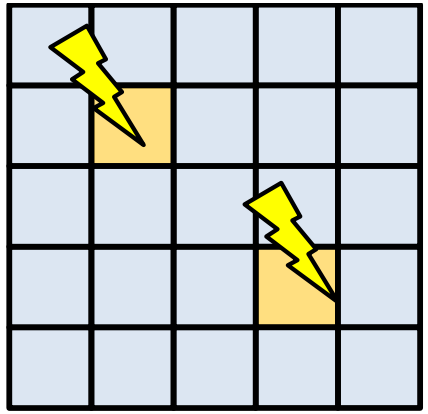


Timestamping mode with event-by-event readout

- Time of arrival with **200 ps** time binning (1.6 ns in Timepix3)
- Time over threshold with **~ 1 keV** resolution
- Hit rate bandwidth **350 million hits/s/cm²** (8 times higher than Timepix3)



Detector



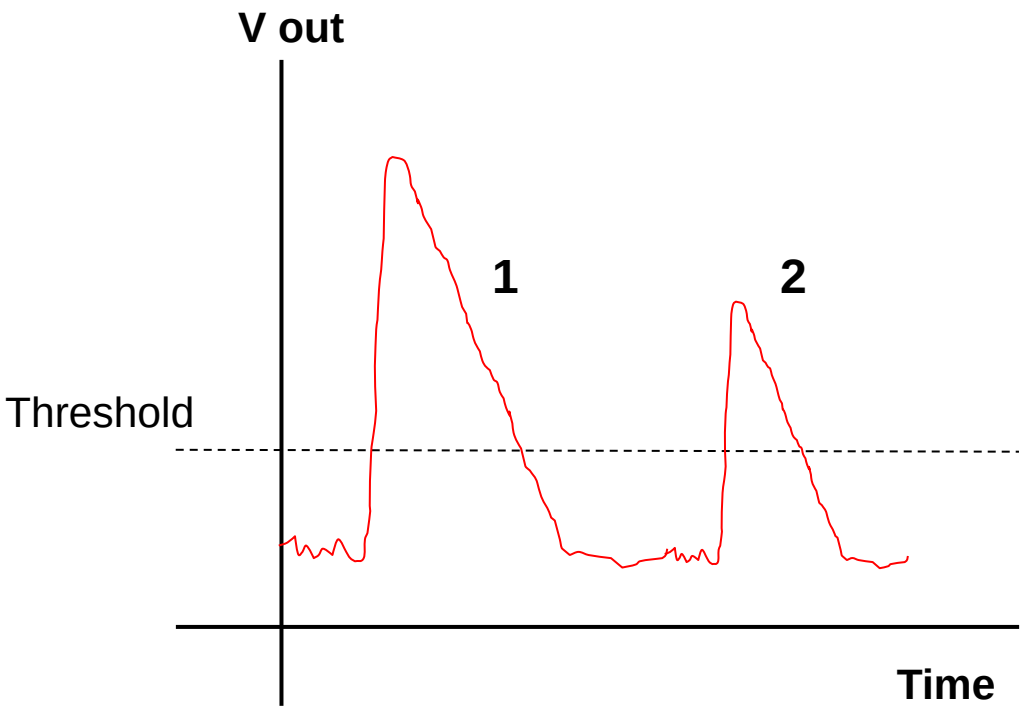
Data packets

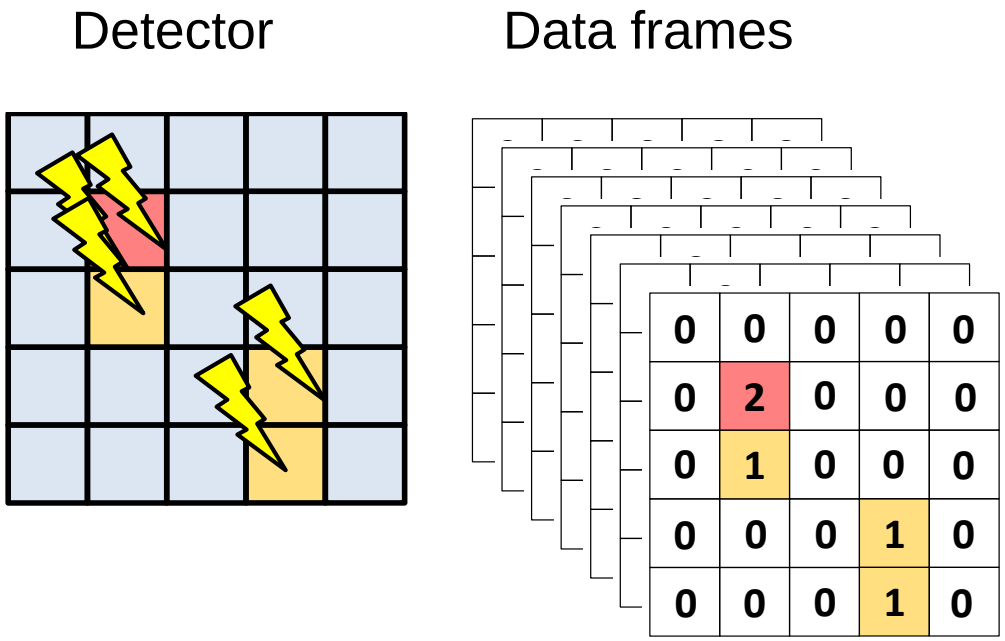
Pixel (1,1)
Energy ~15 keV
Time 525 ns

Pixel (3,3)
Energy ~10 keV
Time 765 ns

Hit counting mode with frame readout

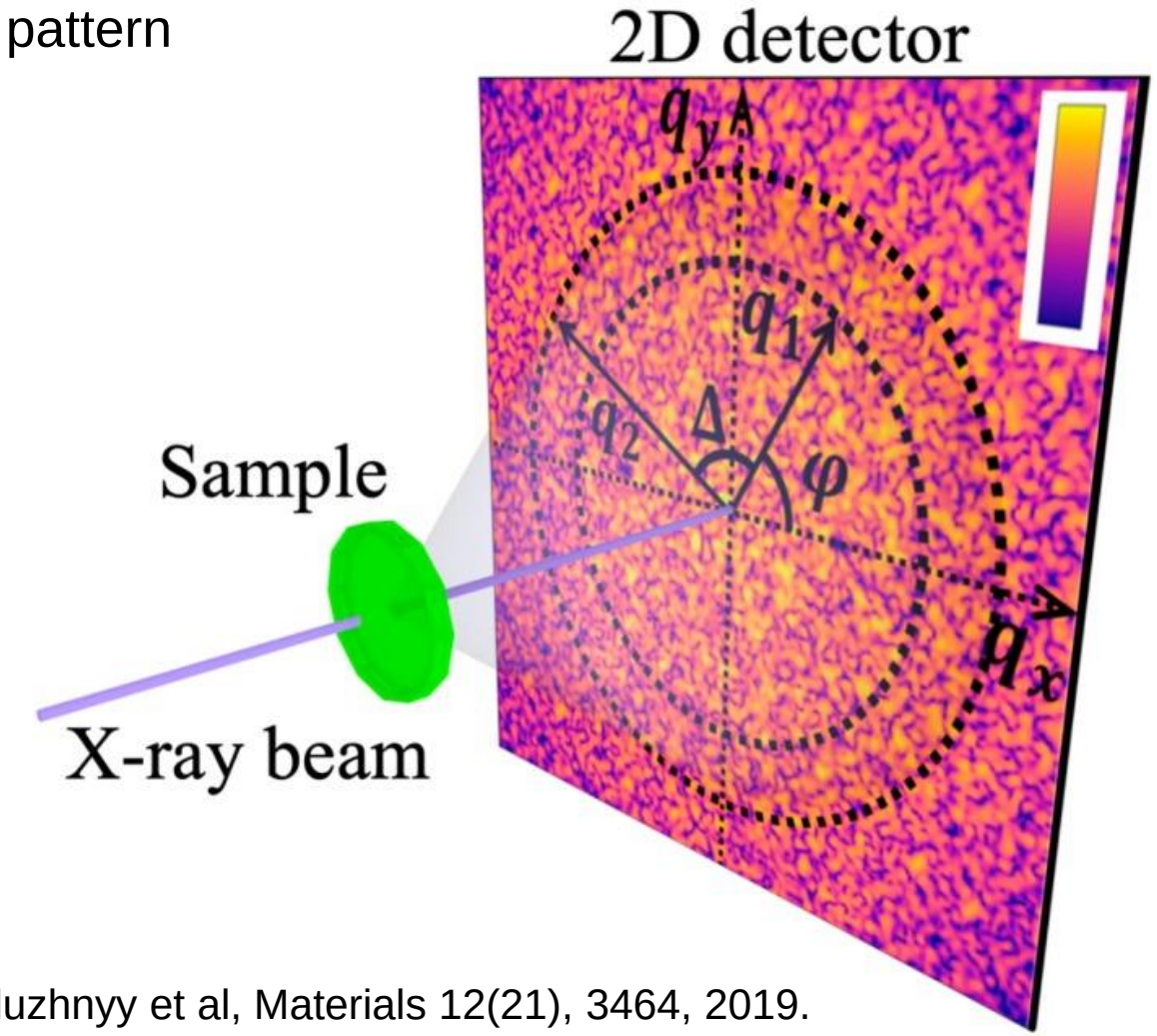
- Single threshold
- Count rate capability – **2 million counts/pix/s** at 10% pileup (10 times higher than Medipix3)
- Up to **80 kHz** frame rate (20 times higher than Medipix3)





Using both readout modes at one synchrotron beamline

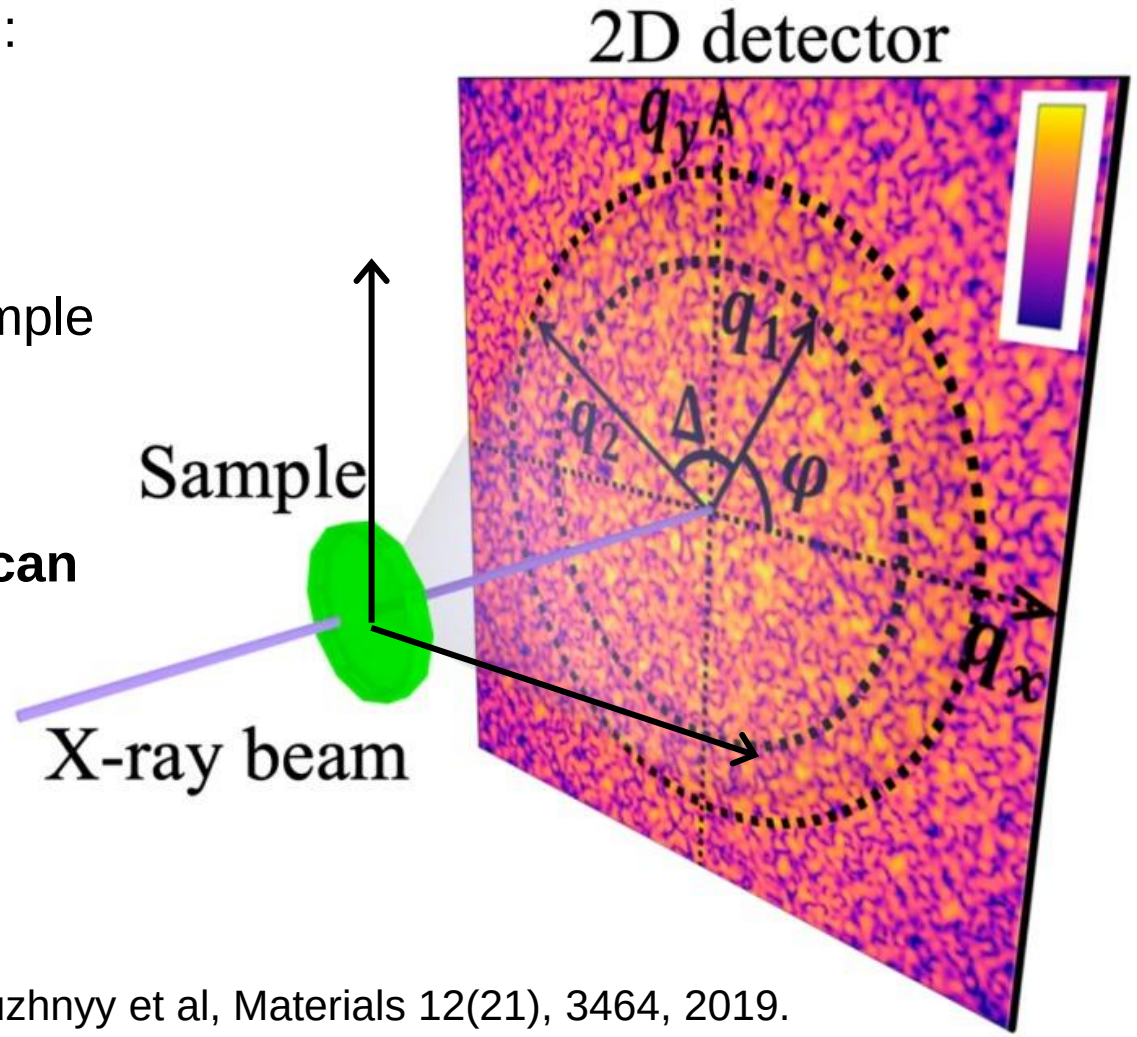
- Diffraction with coherent X-rays produces speckle pattern from non-crystalline object
  - Encodes positions of atoms



I. Zaluzhnyy et al, Materials 12(21), 3464, 2019.
doi: 10.3390/ma12213464

Using both readout modes at one synchrotron beamline

- Large static sample (e.g. nanostructured materials):
  - *Hit counting mode*
  - Take images while moving sample
  - Determine nanoscale structure across large sample



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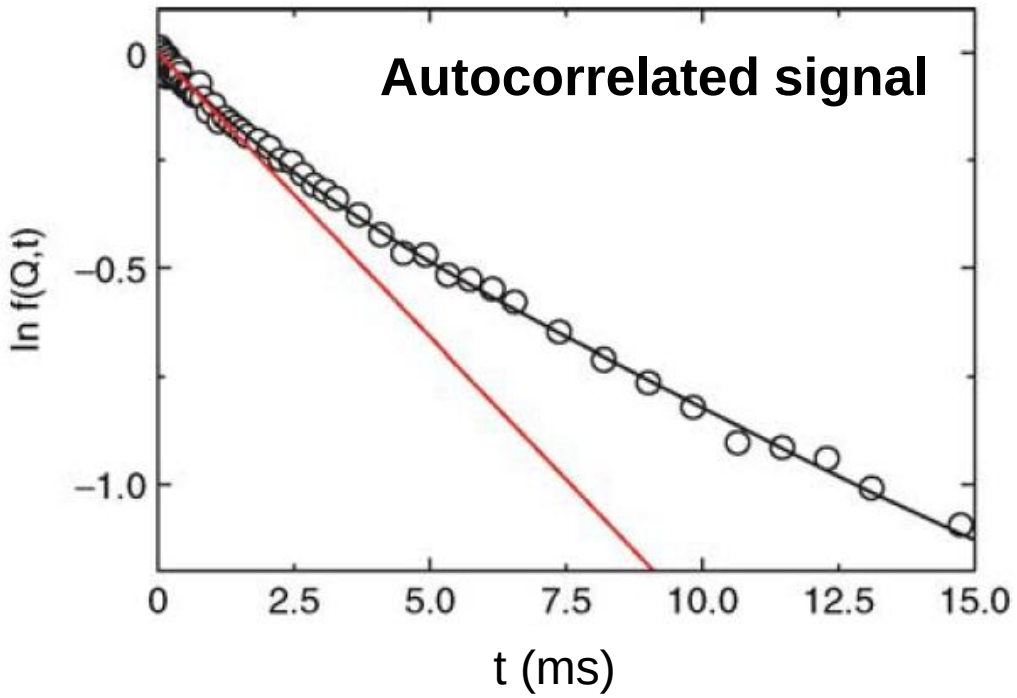
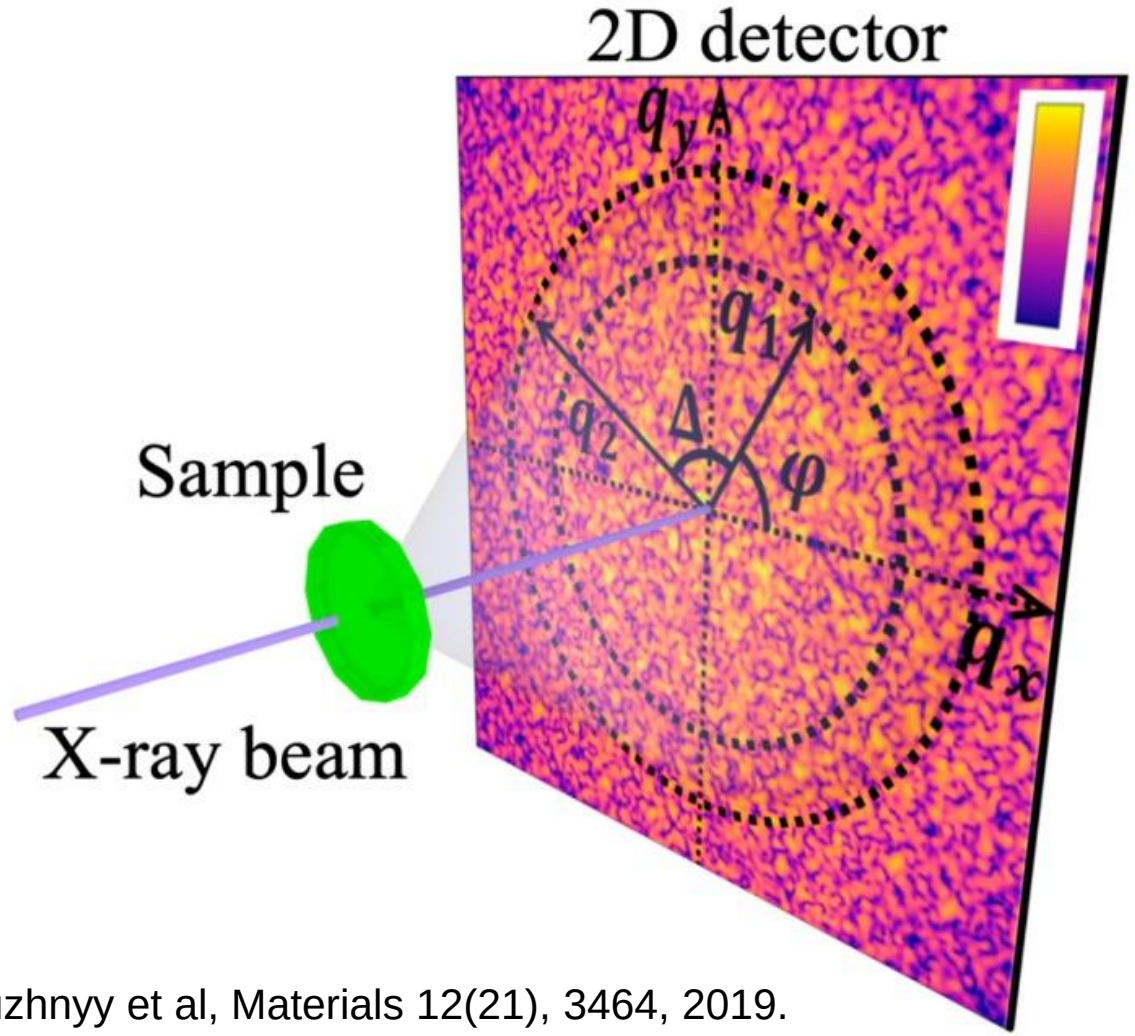
Using both readout modes at one synchrotron beamline

- Dynamic sample (e.g. proteins in solution):
  - *Timestamping mode*
  - Speckle pattern fluctuates over time
  - Deduce dynamics from correlations in signal





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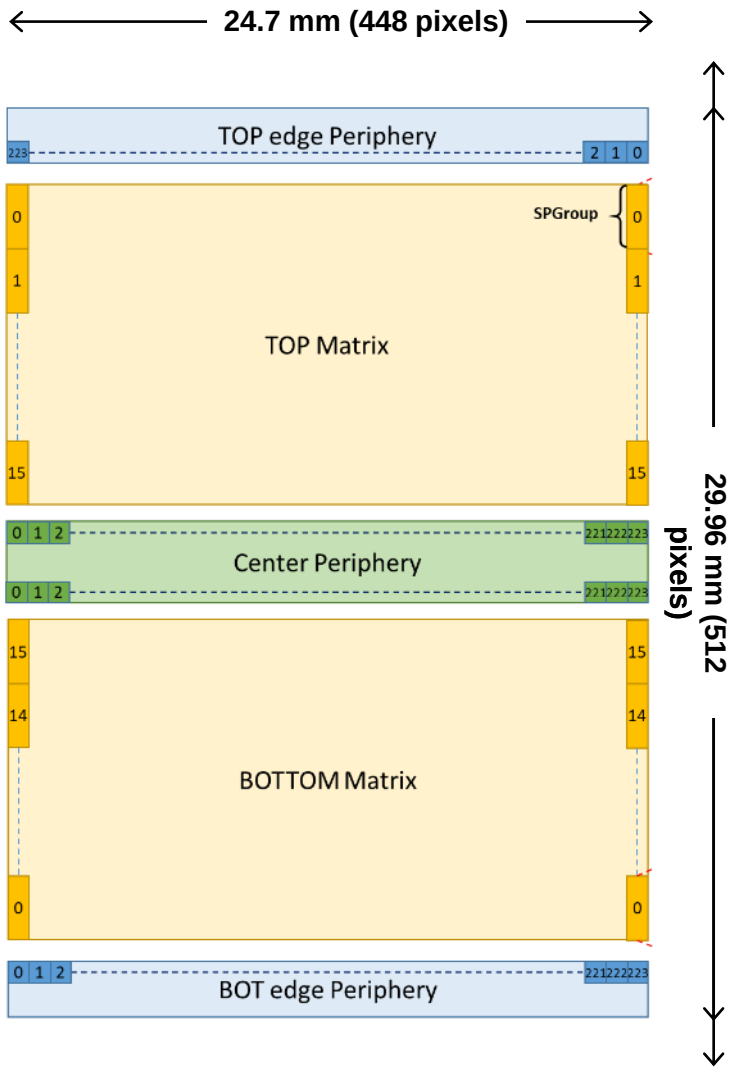
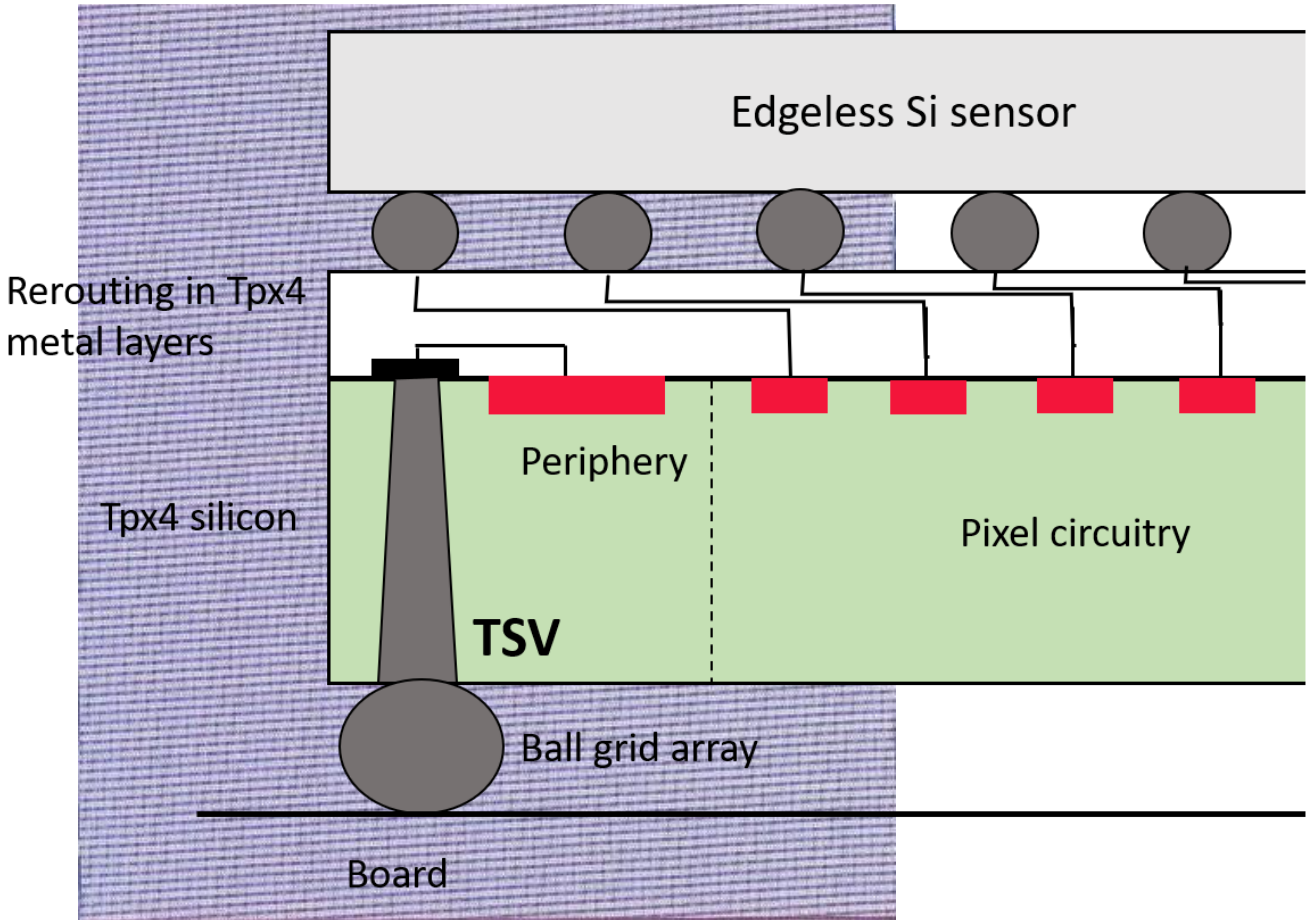
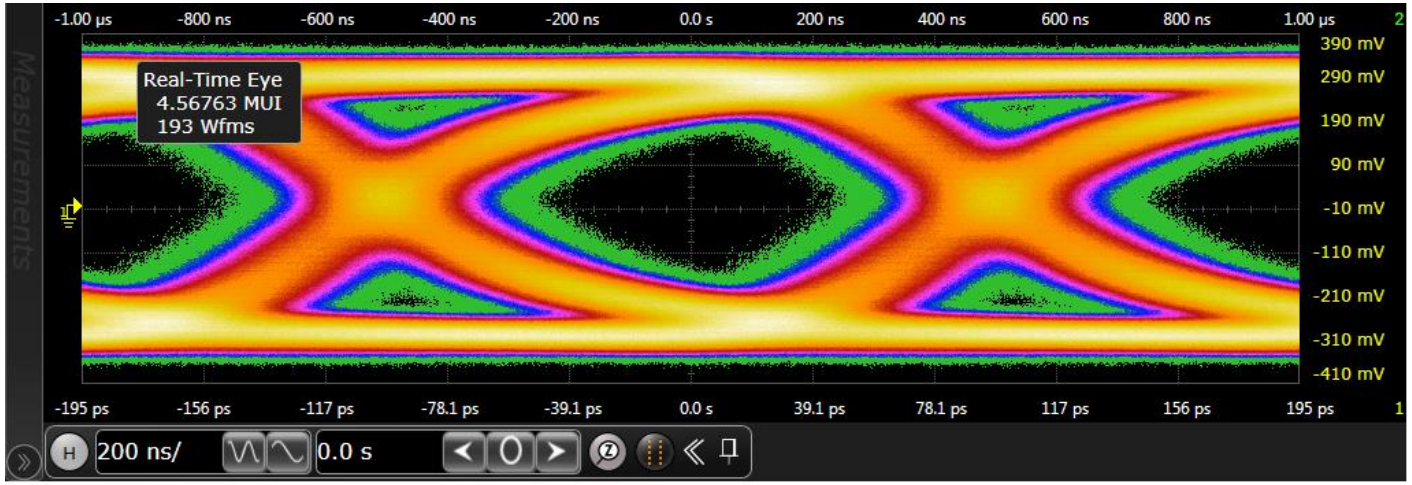
4-side buttable design with Through Silicon Vias





High-speed readout

- High-speed transmitter from Nikhef (successor of transmitter used in Velopix)
- 16 transmitters running up to 10.24 Gbit/s
  - Can be configured to 5.12, 2.56, 1.28… GBit/s

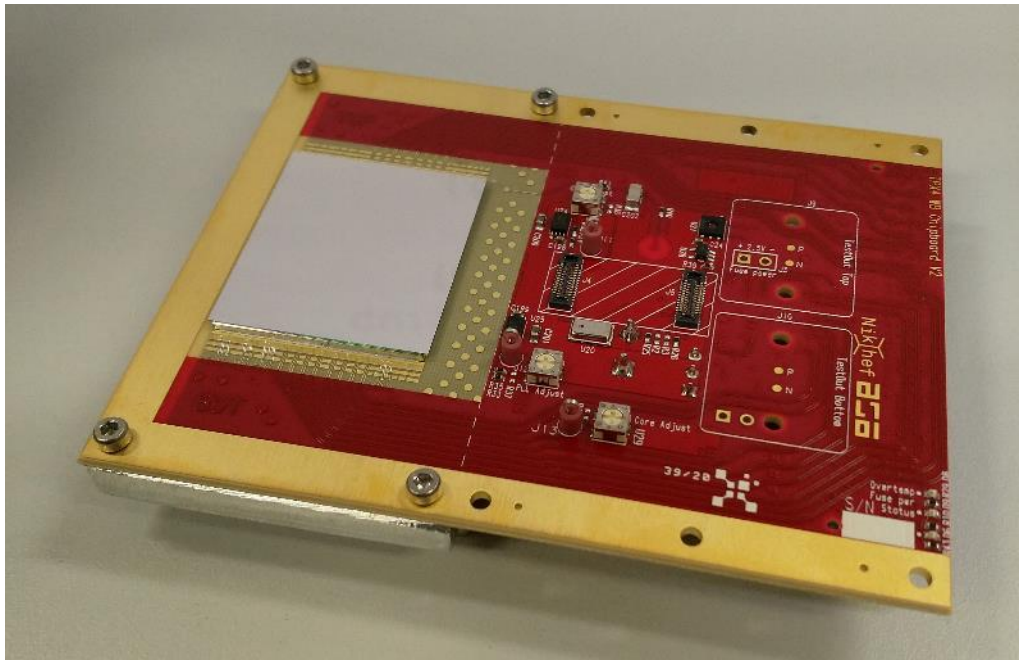


"Eye diagram" with transmitter at 5.12 Gbit/s

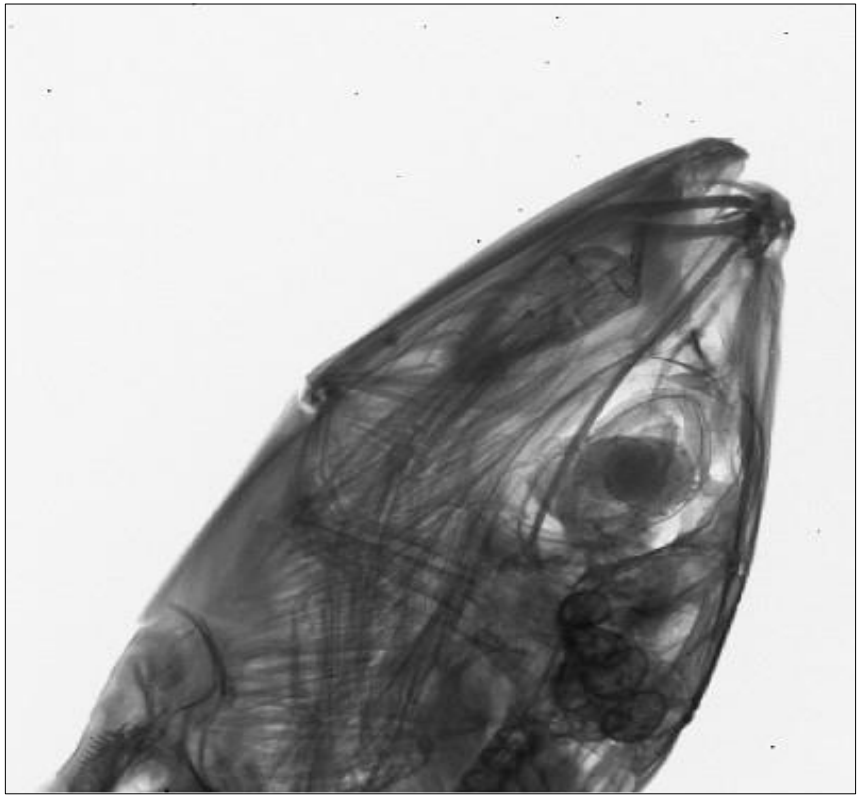
Test results from CERN

- Tested with Si sensor and Nikhef „Spidr4“ readout

Timepix4v1 with 1 448x512 sensor



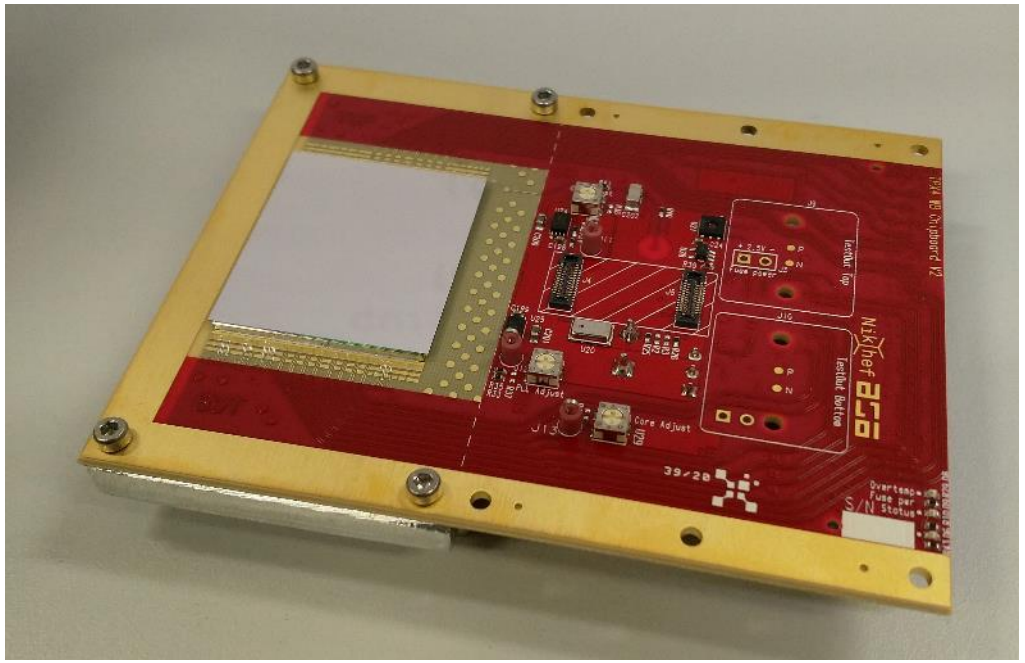
X-ray image from frame mode

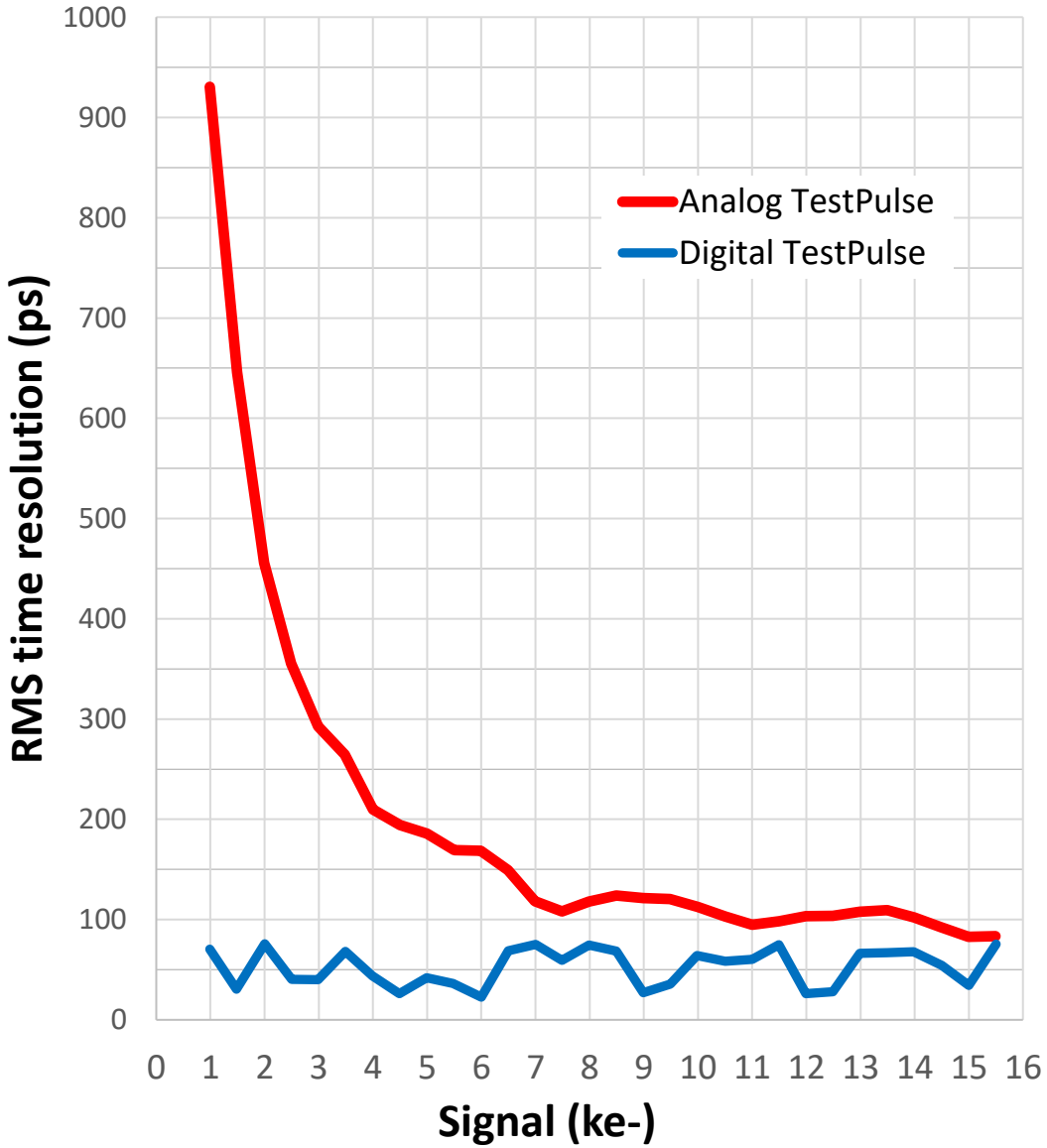


Test results from CERN

- Tested with Si sensor and Nikhef „Spidr4“ readout
- Most functionality works well, time resolution meets specs (~ 150 ps RMS)

Timepix4v1 with 1 448x512 sensor

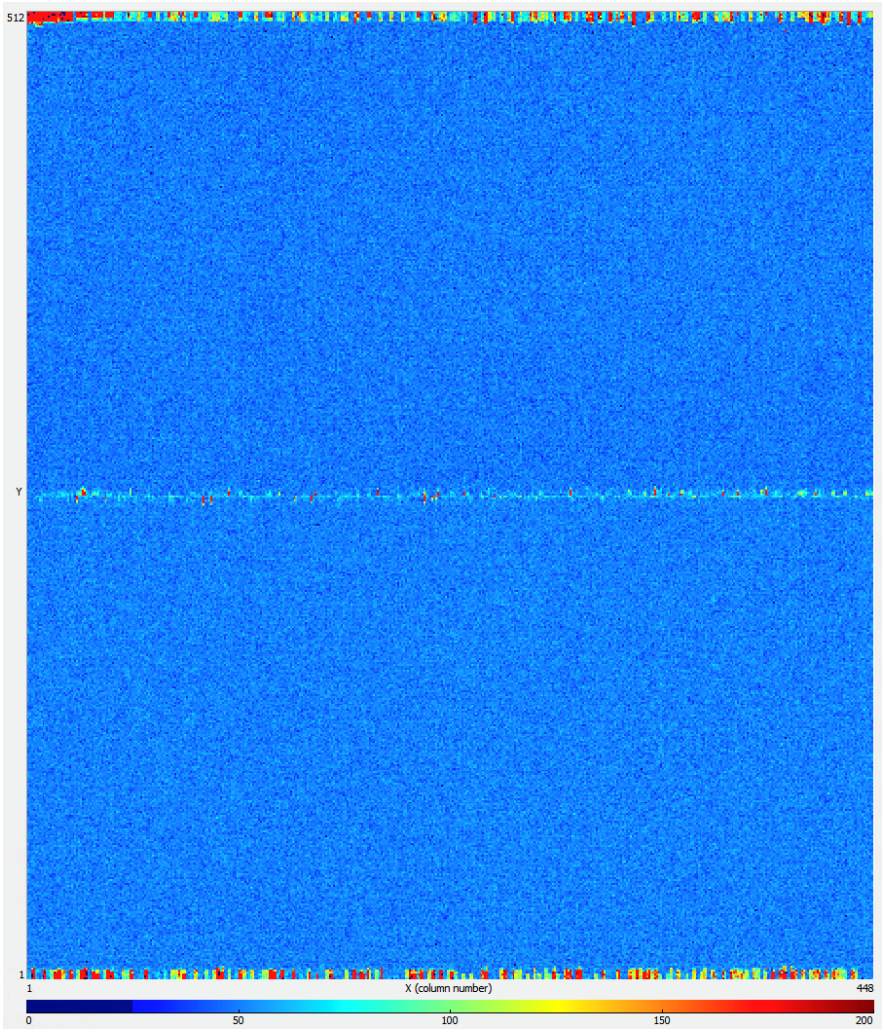




Chip revisions

- Timepix4v0 (Apr 2020)
  - Noisy pixels over “periphery” due to interference
  - 640 MHz Voltage controlled oscillators have too high frequency
    - High-speed readout requires special operating conditions
- Timepix4v1 revision (Oct 2020)
  - Shielding improves noisy pixel behaviour
- Timepix4v2 revision (expected back from foundry soon)
  - VCO behaviour fixed
    - Revised VCO design has been tested in MPW

Timepix4v0 pixel noise



200

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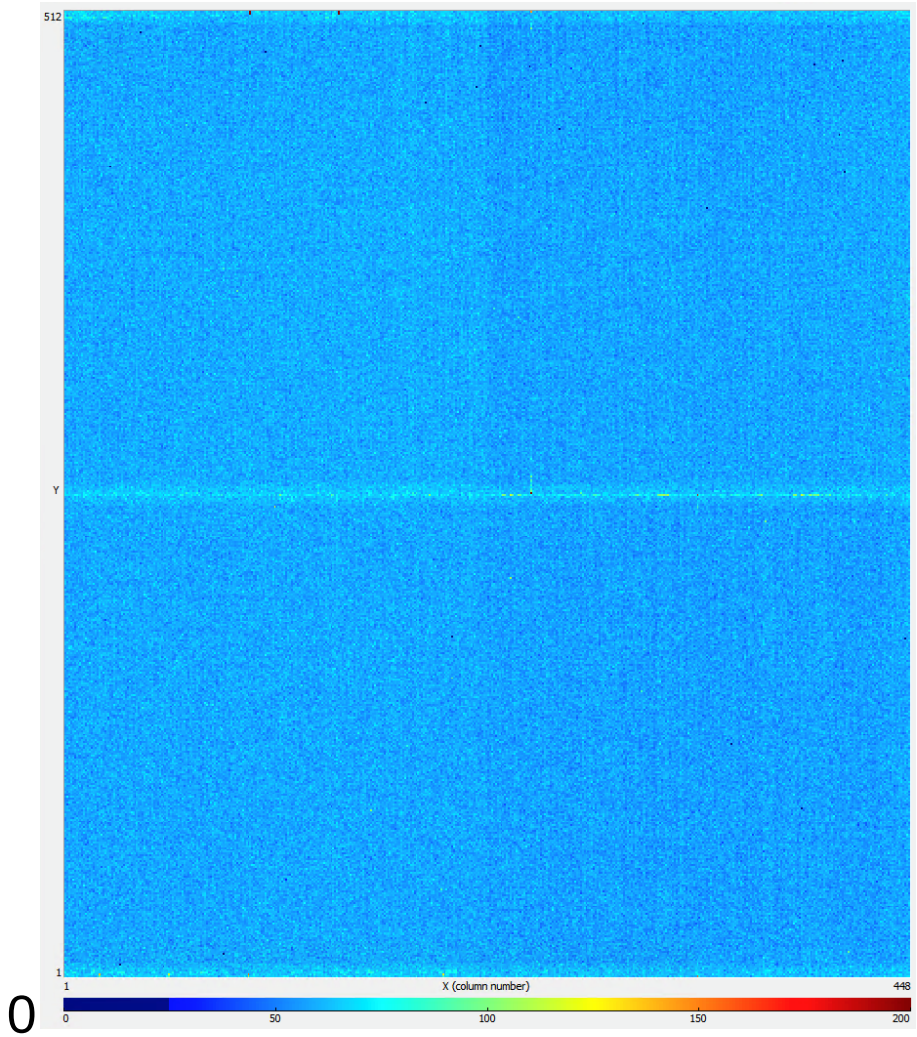
Timepix4v1(changed metal layer)



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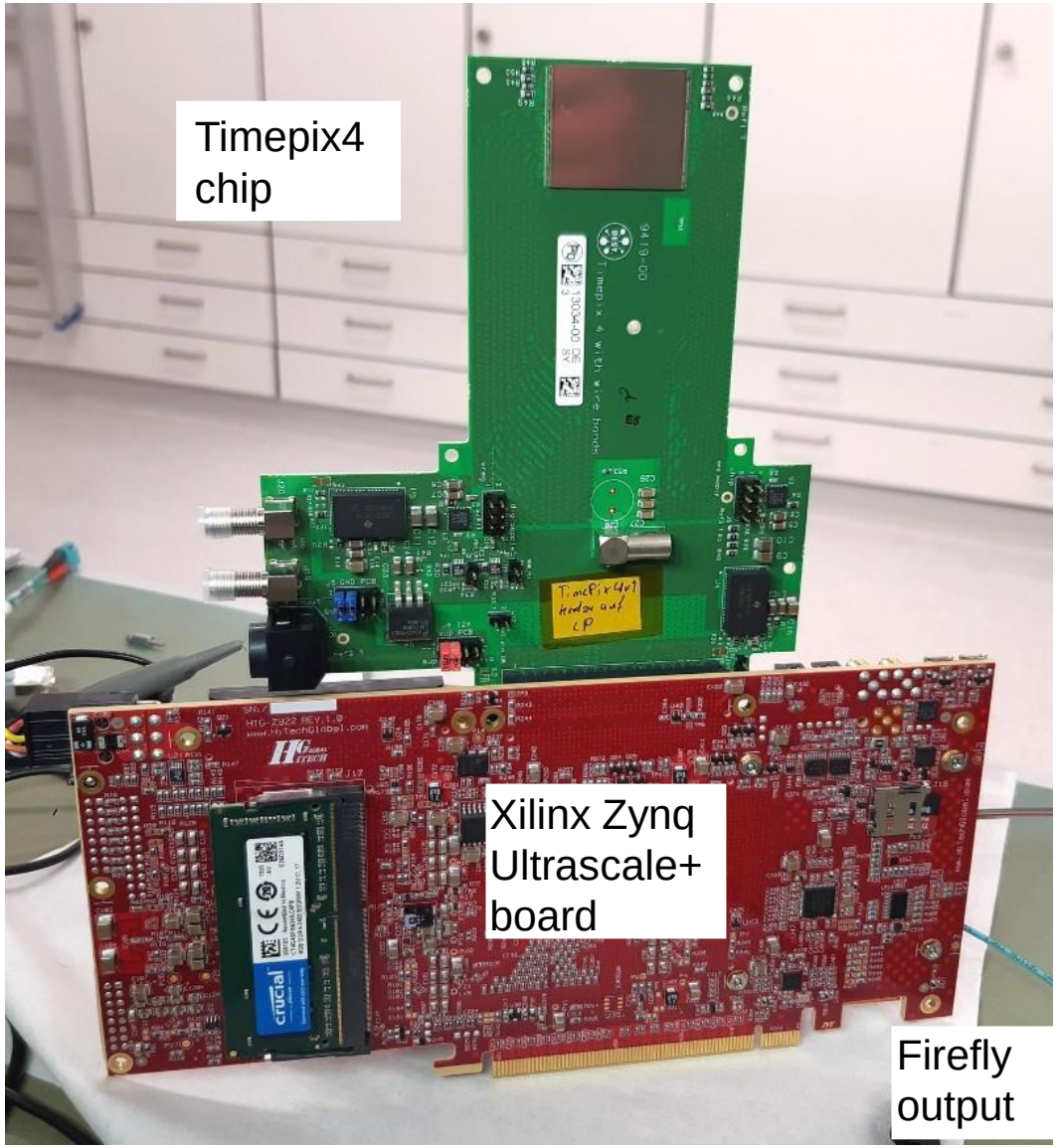
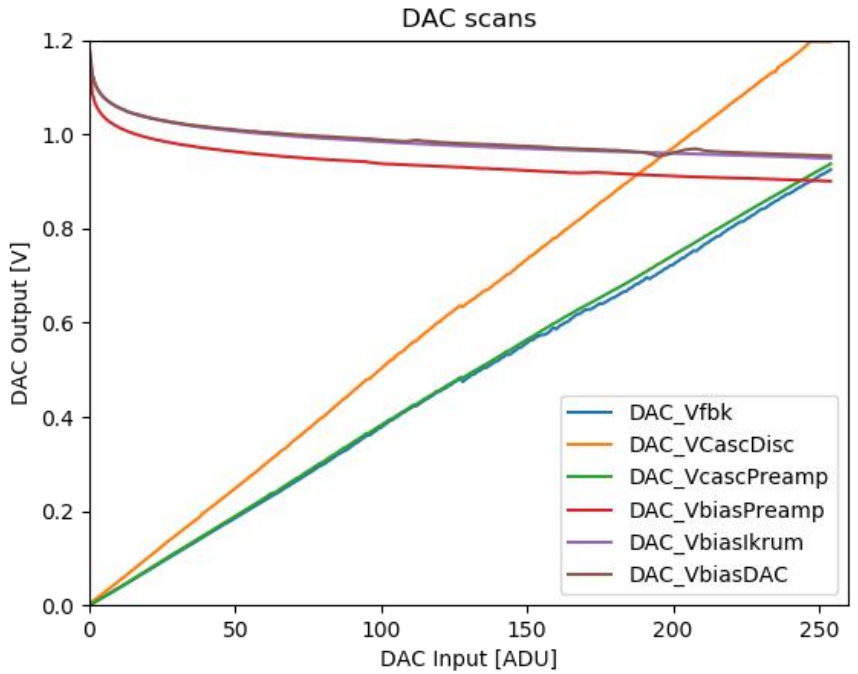
DESY single chip prototype

- Single-chip Timepix4 board connected to off-the-shelf Xilinx board
  - Zynq Ultrascale+ with FPGA fabric and 4-core CPU
- Parallel readout of 16 high-speed links from chip
  - Using specialized transceivers on Zynq
- Daughterboard offering 2 x 100 GBE links over “Firefly” optical cable



Testing single-chip board

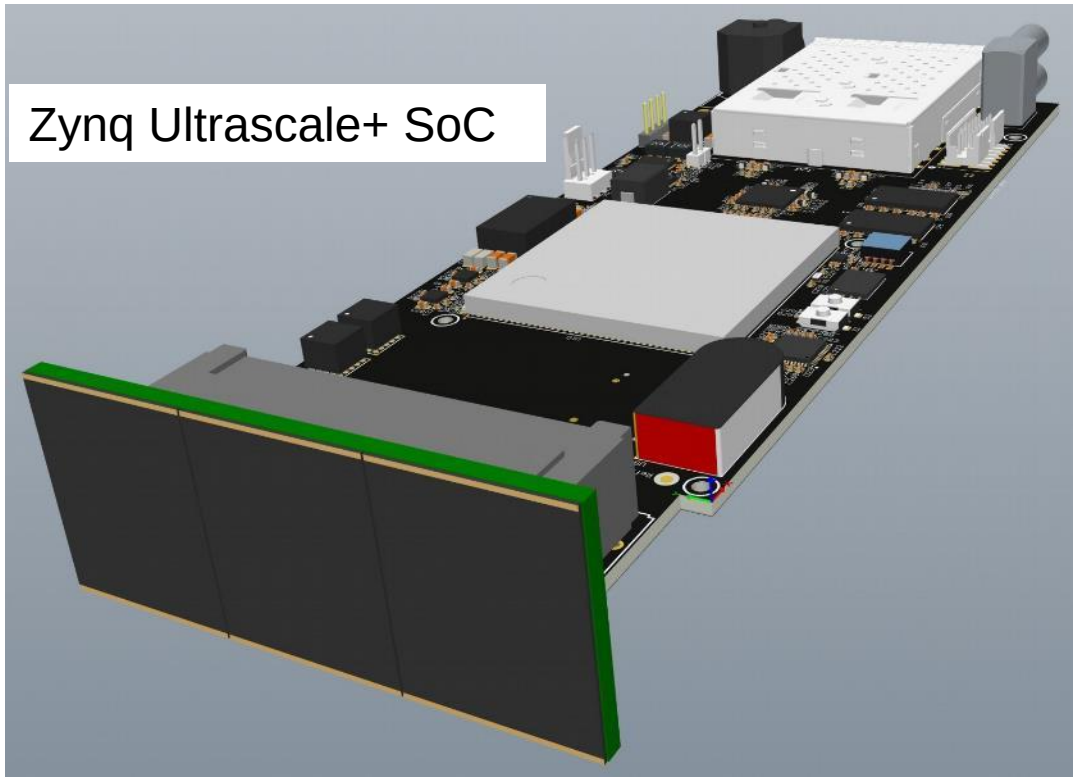
- Control and monitoring of the chip through control interface
  - Problems with image taking, related to board powering
- Data transfer tested from Xilinx board to PC using UDP
  - ~70 Gbit/s rate demonstrated using Mellanox accelerator library
  - 2 x 40 Gbit links are sufficient for reading 16 transceivers at 5 Gbit/s
- Next steps:
  - Revise chipboard design to improve powering
  - Test high-speed transceivers using revised Timepix4v2 chip



Multi-chip, multi-module systems

- Many X-ray experiments require a large continuous detector
- Tileable building block: 3-chip module
- Readout board with Zynq Ultrascale+ SoC
  - 3 x 100 GBE readout
- Ultimate goal – TSVs to eliminate wire bonds
  - Medipix4 collaboration already arranged TSV run with Fraunhofer IZM

3 x 100 GBE cages



3-chip detector head
1344 x 512 pixels

Conclusions

- Timepix4 offers both improved time stamping and hit counting modes
- Timepix4‘s versatility makes it appealing for synchrotron applications
- Most features of the chip work as expected, and Timepix4v2 is expected soon
- Development of readout systems is underway, with large tiled systems planned

> Thanks for listening